

# NCS1002

## Constant Voltage / Constant Current Secondary-Side Controller

### Description

The NCS1002 is a highly integrated solution for Switching Mode Power Supply (SMPS) applications requiring a dual control loop to perform Constant Voltage (CV) and Constant Current (CC) regulation. The NCS1002 integrates a 2.5 V voltage reference and two precision op amps. The voltage reference, along with Op Amp 1, is the core of the voltage control-loop. Op Amp 2 is an independent, uncommitted amplifier specifically designed for the current control. Key external components needed to complete the two control loops are: (a) A resistor divider that senses the output of the power supply (battery charger) and fixes the voltage regulation set point at the specified value. (b) A sense resistor that feeds the current sensing circuit with a voltage proportional to the DC output current. This resistor determines the current regulation set point and must be adequately rated in terms of power dissipation. The NCS1002 comes in a small 8-pin SOIC package and is ideal for space-shrunk applications such as battery chargers.

### Features

- Low Input Offset Voltage: 0.5 mV, Typ
- Input Common-Mode Range includes Ground
- Low Quiescent Current: 300  $\mu$ A per Op Amp at  $V_{CC} = 5$  V
- Large Output Voltage Swing
- Wide Power Supply Range: 3 V to 32 V
- High ESD Protection: 2 kV
- These are Pb-Free Devices

### Typical Applications

- Battery Chargers
- Switch Mode Power Supplies



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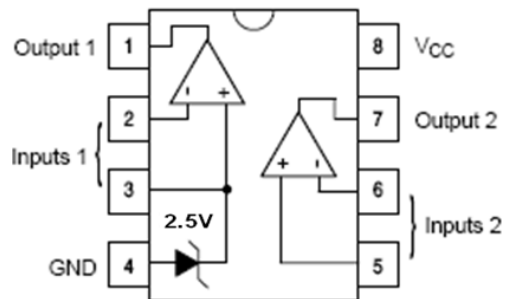
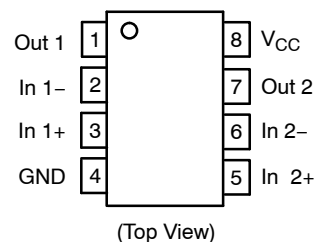
### MARKING DIAGRAMS



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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## MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage ( $V_{CC}$ to GND)	$V_{CC}$	36	V
Differential Input Voltage	$V_{id}$	36	V
Input Voltage	$V_i$	-0.3 to +36	V
ESD Protection Voltage at Pin Human Body Model	$V_{ESD}$	2000	V
Maximum Junction Temperature	$T_J$	150	°C
Specification Temperature Range ( $T_{min}$ to $T_{max}$ )	$T_A$	-40 to +105	°C
Operating Free-Air Temperature Range	$T_{oper}$	-55 to +125	°C
Storage Temperature Range	$T_{stg}$	-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## THERMAL CHARACTERISTICS

Parameter	Symbol	Rating	Unit
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	175	°C/W

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## ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
$I_{CC}$	Total Supply Current, excluding current in the Voltage Reference $V_{CC} = 5$ V, no load; $-40 \leq T_A \leq +105^\circ\text{C}$			0.3	0.4	mA
$I_{CC}$	Total Supply Current, excluding Current in the Voltage Reference $V_{CC} = 30$ V, no load; $-40 \leq T_A \leq +105^\circ\text{C}$				0.75	mA

### OP AMP 1 (OP AMP WITH NONINVERTING INPUT CONNECTED TO THE INTERNAL $V_{ref}$ ) ( $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ unless otherwise noted)

$V_{IO}$	Input Offset Voltage	$T_A = 25^\circ\text{C}$			2.0	mV
		$-40 \leq T_A \leq +105^\circ\text{C}$			3.0	mV
$DV_{IO}$	Input Offset Voltage Drift ( $-40 \leq T_A \leq +105^\circ\text{C}$ )			7.0		$\mu\text{V}/^\circ\text{C}$
$I_{IB}$	Input Bias Current (Inverting Input Only) $T_A = 25^\circ\text{C}$			20		nA
AVD	Large Signal Voltage Gain ( $V_{CC} = 15$ V, $R_L = 2$ k $\Omega$ , $V_{ICM} = 0$ V)			100		V/mV
PSRR	Power Supply Rejection ( $V_{CC} = 5.0$ V to 30 V, $V_{OUT} = 2$ V)		80	100		dB
$I_{SOURCE}$	Output Source Current ( $V_{CC} = 15$ V, $V_{OUT} = 2.0$ V, $V_{id} = 1$ V)		20	40		mA
$I_O$	Short Circuit to GND ( $V_{CC} = 15$ V)			40	60	mA
$I_{SINK}$	Output Current Sink ( $V_{id} = -1$ V)	$V_{CC} = +15$ V, $V_{OUT} = 0.2$ V (Note 1)	1	10		mA
		$V_{CC} = +15$ V, $V_{OUT} = 2$ V	10	20		mA
$V_{OH}$	Output Voltage Swing, High ( $V_{CC} = 30$ V)	$R_L = 2$ k $\Omega$ , $T_A = 25^\circ\text{C}$	26	27		V
		$-40 \leq T_A \leq +105^\circ\text{C}$	26			
		$R_L = 10$ k $\Omega$ , $T_A = 25^\circ\text{C}$	27	28		
		$-40 \leq T_A \leq +105^\circ\text{C}$	27			
$V_{OL}$	Output Voltage Swing, Low	$R_L = 10$ k $\Omega$ , $T_A = 25^\circ\text{C}$		5.0	50	mV
		$-40 \leq T_A \leq +105^\circ\text{C}$			50	
SR	Slew Rate ( $AV = +1$ , $V_i = 0.5$ V to 2 V, $V_{CC} = 15$ V, $R_L = 2$ k $\Omega$ , $C_L = 100$ pF)		0.2	0.4		V/ $\mu\text{s}$
GBP	Gain Bandwidth Product ( $V_{CC} = 30$ V, $AV = +1$ , (Note 1) $R_L = 2$ k $\Omega$ , $C_L = 100$ pF, $f = 100$ kHz, $V_{IN} = 10$ mV <sub>PP</sub> )		0.5	0.9		MHz
THD	Total Harmonic Distortion ( $f = 1$ kHz, $AV = 10$ , $R_L = 2$ k $\Omega$ , $V_{CC} = 30$ V, $V_{OUT} = 2$ V <sub>PP</sub> )			0.08		%

### OP AMP 2 (INDEPENDENT OP AMP) ( $V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$ unless otherwise noted)

$V_{IO}$	Input Offset Voltage	$T_A = 25^\circ\text{C}$		0.5	2.0	mV
		$-40 \leq T_A \leq +105^\circ\text{C}$			3.0	
$DV_{IO}$	Input Offset Voltage Drift ( $-40 \leq T_A \leq +105^\circ\text{C}$ )			7.0		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input Offset Current	$T_A = 25^\circ\text{C}$		2.0	75	nA
		$-40 \leq T_A \leq +105^\circ\text{C}$			150	
$I_{IB}$	Input Bias Current	$T_A = 25^\circ\text{C}$		20	150	nA
		$-40 \leq T_A \leq +105^\circ\text{C}$			200	
AVD	Large Signal Voltage Gain ( $V_{CC} = 15$ V, $R_L = 2$ k $\Omega$ , $V_{OUT} = 1.4$ V to 11.4 V)	$T_A = 25^\circ\text{C}$	50	100		V/mV
		$-40 \leq T_A \leq +105^\circ\text{C}$	25			
PSRR	Power Supply Rejection ( $V_{CC} = 5$ V to 30 V)		65	100		dB

1. Guaranteed by design and/or characterization.

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## ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
<b>OP AMP 2 (INDEPENDENT OP AMP) (continued)</b> ( $V_{CC} = 5.0\text{ V}$ , $T_A = 25^\circ\text{C}$ unless otherwise noted)						
$V_{ICM}$	Input Common Mode Voltage Range (Note 2) ( $V_{CC} = +30\text{ V}$ )	$T_A = 25^\circ\text{C}$	0		$V_{CC} - 1.5$	V
		$-40 \leq T_A \leq +105^\circ\text{C}$	0		$V_{CC} - 2.0$	
CMRR	Common Mode Rejection Ratio (Note 4)	0 to $V_{CC} - 1.7\text{ V}$ , $T_A = 25^\circ\text{C}$	70	85		dB
		0 to $V_{CC} - 2.2\text{ V}$ $-40 \leq T_A \leq +105^\circ\text{C}$	60			
$I_{SOURCE}$	Output Current Source ( $V_{CC} = 15\text{ V}$ , $V_{OUT} = 2\text{ V}$ , $V_{ID} = +1\text{ V}$ )		20	40		mA
$I_O$	Short-Circuit to GND ( $V_{CC} = 15\text{ V}$ )			40	60	mA
$I_{SINK}$	Output Current Sink ( $V_{ID} = -1\text{ V}$ )	$V_{CC} = +15\text{ V}$ , $V_{OUT} = 0.2\text{ V}$	1	10		mA
		$V_{CC} = +15\text{ V}$ , $V_{OUT} = 2\text{ V}$	10	20		mA
$V_{OH}$	Output Voltage Swing, High ( $V_{CC} = 30\text{ V}$ )	$R_L = 2\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	26	27		V
		$-40 \leq T_A \leq +105^\circ\text{C}$	26			
		$R_L = 10\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	27	28		
		$-40 \leq T_A \leq +105^\circ\text{C}$	27			
$V_{OL}$	Output Voltage Swing, Low	$R_L = 10\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$		5.0	50	mV
		$-40 \leq T_A \leq +105^\circ\text{C}$			50	
SR	Slew Rate ( $AV = +1$ , $V_i = 0.5\text{ V}$ to $3\text{ V}$ , $V_{CC} = 15\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ )		0.2	0.4		V/ $\mu\text{s}$
GBP	Gain Bandwidth Product ( $V_{CC} = 30\text{ V}$ , $AV = +1$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$ , $V_{IN} = 10\text{ mV}_{PP}$ ) (Note 4)		0.5	0.9		MHz
THD	Total Harmonic Distortion ( $f = 1\text{ kHz}$ , $AV = 10$ , $R_L = 2\text{ k}\Omega$ , $V_{CC} = 30\text{ V}$ , $V_{OUT} = 2\text{ V}_{PP}$ )			0.08		%
$e_{noise}$	Equivalent Input Noise Voltage ( $f = 1\text{ kHz}$ , $R_S = 100\ \Omega$ , $V_{CC} = 30\text{ V}$ )			50		nV/ $\sqrt{\text{Hz}}$

## VOLTAGE REFERENCE

$I_K$	Cathode Current		1 to 100			mA
$V_{ref}$	Reference Voltage ( $I_K = 1\text{ mA}$ )	$T_A = 25^\circ\text{C}$	2.49	2.5	2.51	V
		$-40 \leq T_A \leq +105^\circ\text{C}$	2.48	2.5	2.52	
$\Delta V_{ref}$	Reference Deviation over Temperature ( $V_{KA} = V_{ref}$ , $I_K = 10\text{ mA}$ , $-40 \leq T_A \leq +105^\circ\text{C}$ ) (Note 4)			7.0	30	mV
$I_{min}$	Minimum Cathode Current for Regulation ( $V_{KA} \geq 2.45\text{ V}_i$ )			40	75	$\mu\text{A}$
$ Z_{KA} $	Dynamic Impedance (Note 3) ( $V_{KA} = V_{ref}$ , $I_K = 1\text{ mA}$ to $100\text{ mA}$ , $f < 1\text{ kHz}$ )			0.2	0.5	$\Omega$

- The input common-mode voltage of either input signal should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode range is  $V_{CC} - 1.5\text{ V}$ . Both inputs can go to  $V_{CC} + 0.3\text{ V}$  without damage.
- The Dynamic Impedance is defined as  $|Z_{KA}| = \Delta V_{KA} / \Delta I_K$ .
- Guaranteed by design and/or characterization.

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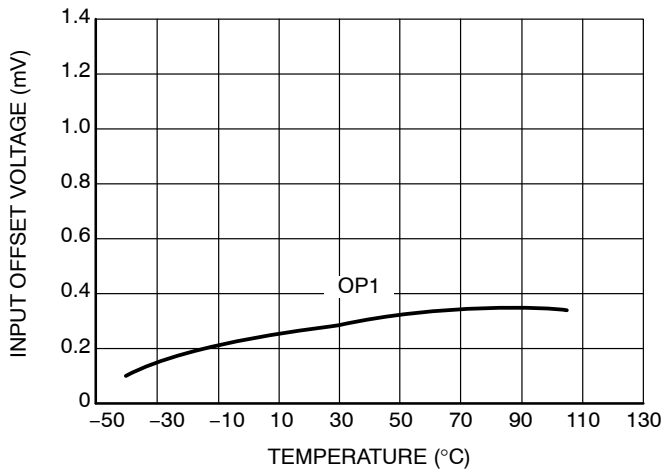


Figure 1. Input Offset Voltage vs. Temperature

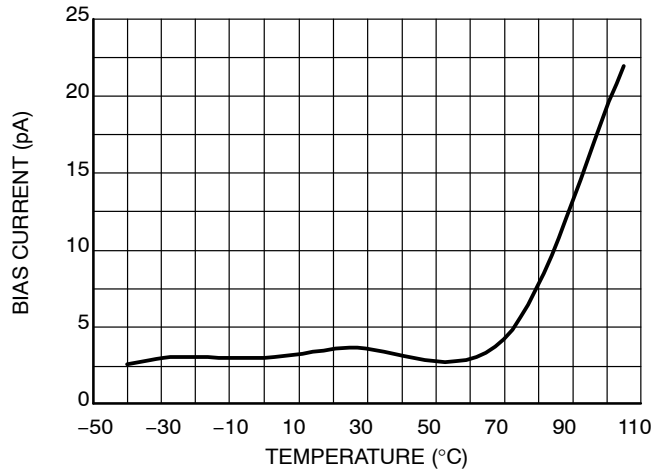


Figure 2. IB vs. Temperature

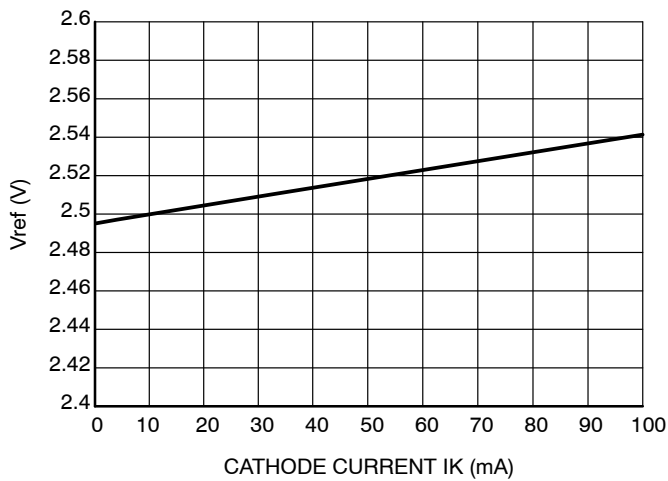


Figure 3. Vref as a Function of IK

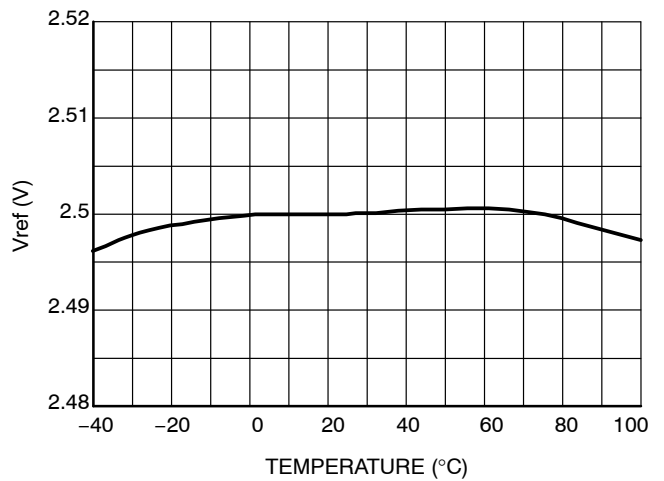


Figure 4. Vref Over Temperature

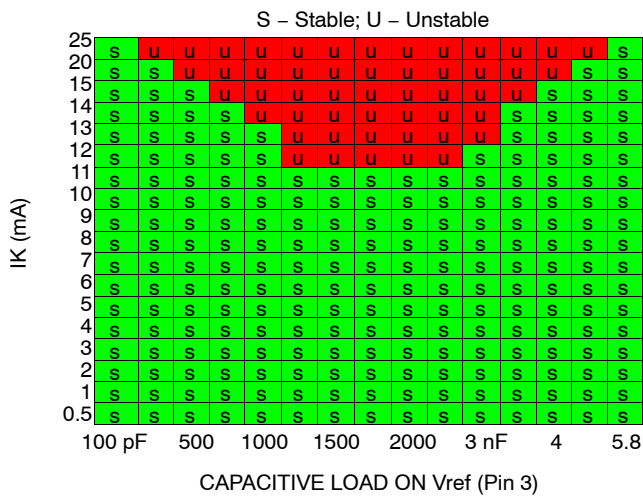


Figure 5. Region of Reference Stability vs. Capacitive Load (Pin 3)

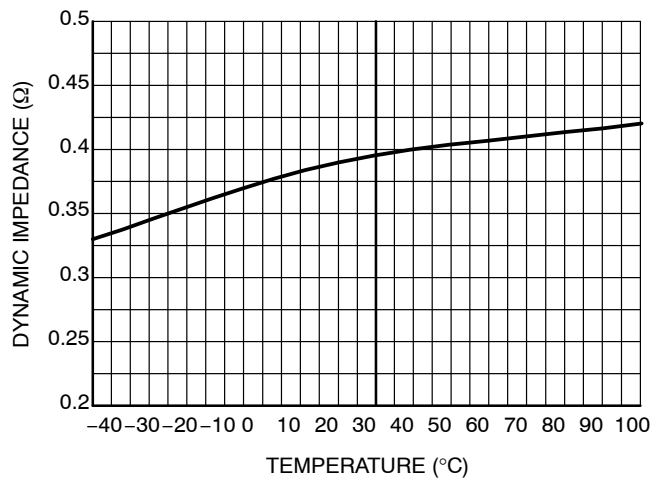


Figure 6. Ref Dynamic Impedance vs. Temperature

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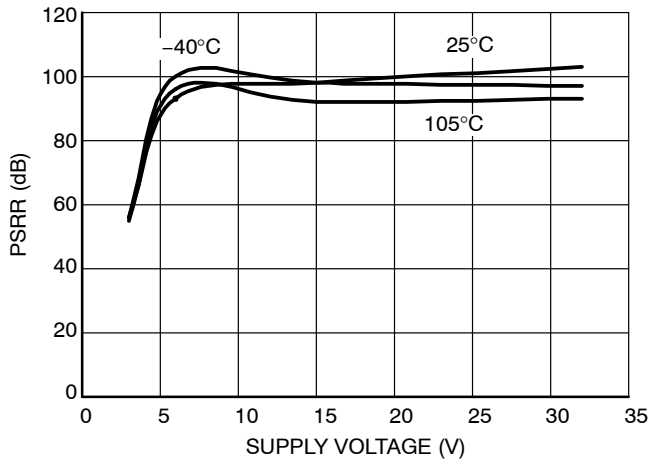


Figure 7. NCS1002 PSRR vs. Supply Voltage

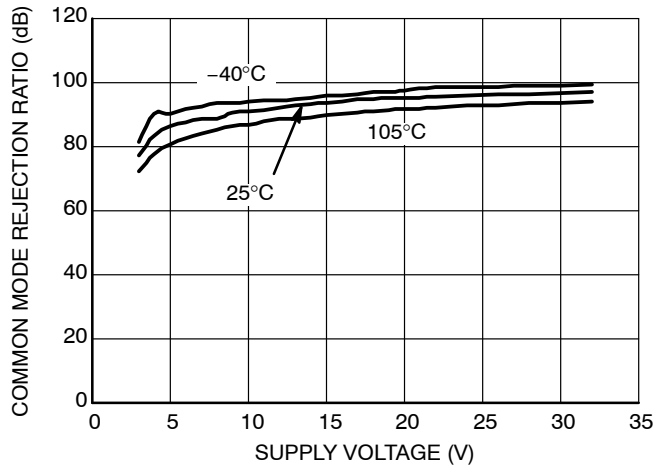


Figure 8. NCS1002 CMRR vs. Supply Voltage

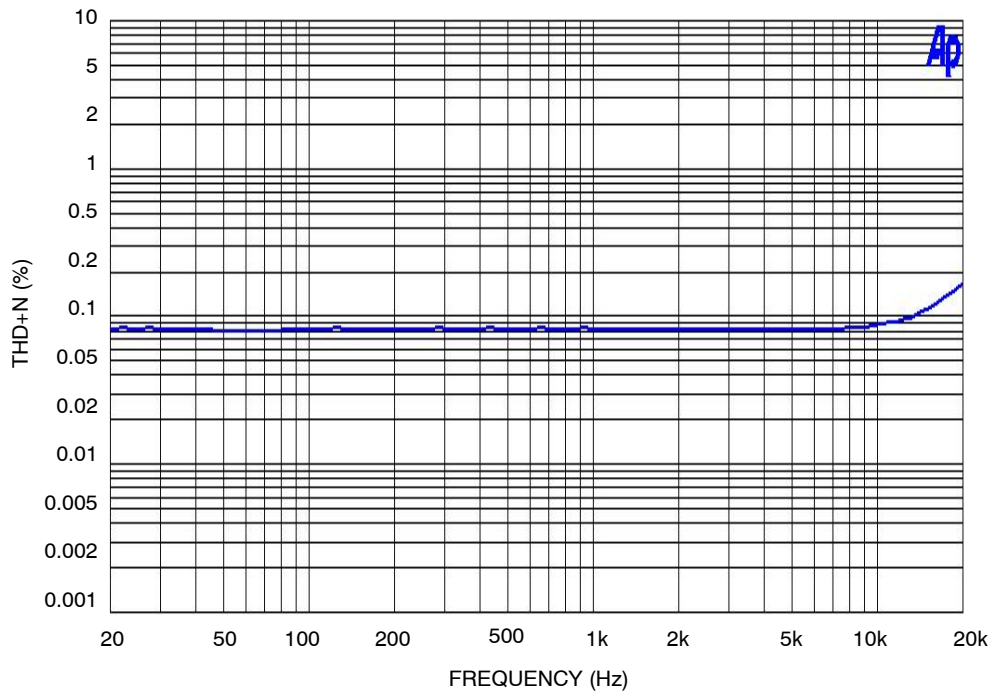


Figure 9. THD+N

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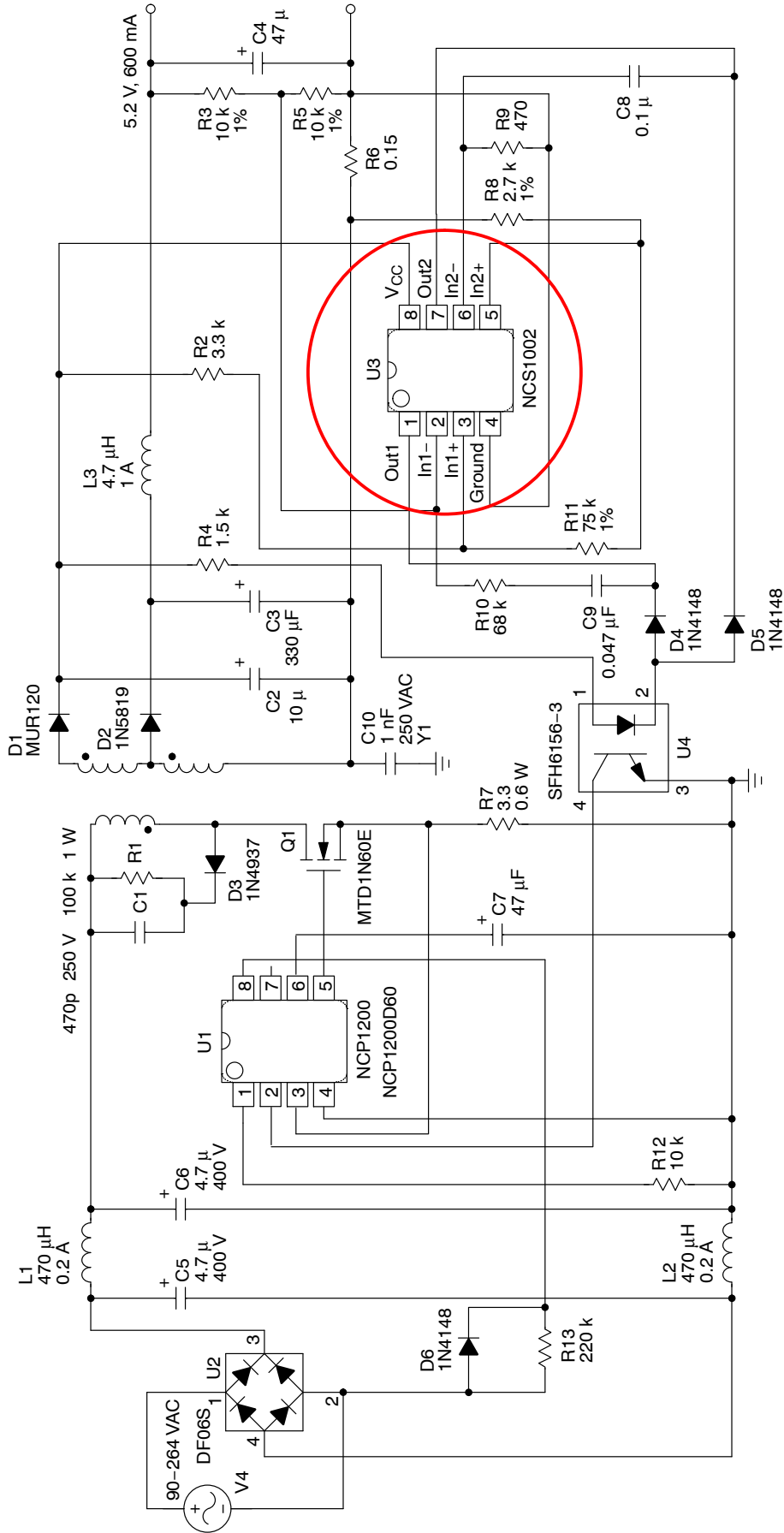


Figure 1. AC Adapter Application

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## ORDERING INFORMATION

Device	Package	Shipping†
NCS1002DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

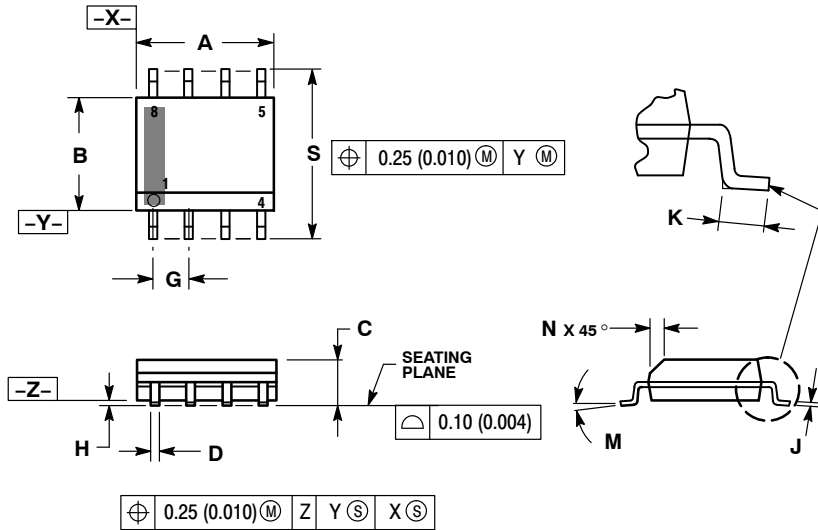
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AJ

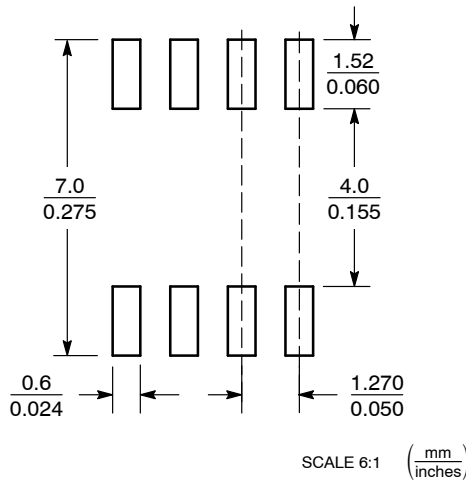


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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