WLED Driver for Notebooks with PWM Interface and Auto Phase Shift

Check for Samples: TPS61187

FEATURES

- **4.5 V to 24 V Input Voltage**
- **38 V Maximum Output Voltage**
- **Integrated 2 A 40 V MOSFET**
- **300 kHz to 1 MHz Programmable Switching Frequency**
- **Adaptive Boost Output to WLED Voltages**
- **Wide PWM Dimming Frequency Range**
  - **100 Hz to 50 KHz for Direct PWM Mode**
  - **100 Hz to 22 KHz for Frequency Programmable Mode**
- **100:1 Dimming Ratio at 20 kHz**
- **10000:1 Dimming Ratio at 200 Hz (Direct PWM mode)**
- **Small External Components**
- **Integrated Loop Compensation**
- **Six Current Sinks of 30 mA Max**
- **1.5% (Typ) Current Matching**
- **PWM Brightness Interface Control**
- **PWM Phase Shift Mode Brightness Dimming Method or Direct PWM Dimming Method**
- **4 kV HBM ESD Protection**
- **Programmable Over Voltage Threshold**
- **Built-in WLED Open/Short Protection**
- **Thermal Shutdown**
- **20 Lead 4mm × 4mm × 0.8 mm TQFN Package**

APPLICATIONS

- **Notebook LCD Display Backlight**

DESCRIPTION

The TPS61187 IC provides a highly integrated WLED driver solution for notebook LCD backlight. This device has a built-in high efficiency boost regulator with integrated 2.0A /40V power MOSFET. The six current sink regulators provide high precision current regulation and matching. In total, the device can support up to 60 WLEDs. In addition, the boost output automatically adjusts its voltage to the WLED forward voltage to optimize efficiency.

The TPS61187 supports the auto phase shift dimming method and direct PWM dimming method. During phase shift PWM dimming, the WLED current is turned on/off at the duty cycle controlled by the input PWM signal and each channel is shifted according to the frequency determined by an integrated pulse width modulation (PWM) signal. The frequency of this signal is resistor programmable, while the duty cycle is controlled directly from an external PWM signal input to the PWM pin. During direct PWM dimming, the WLED current is turned on/off synchronized with the input PWM signal.

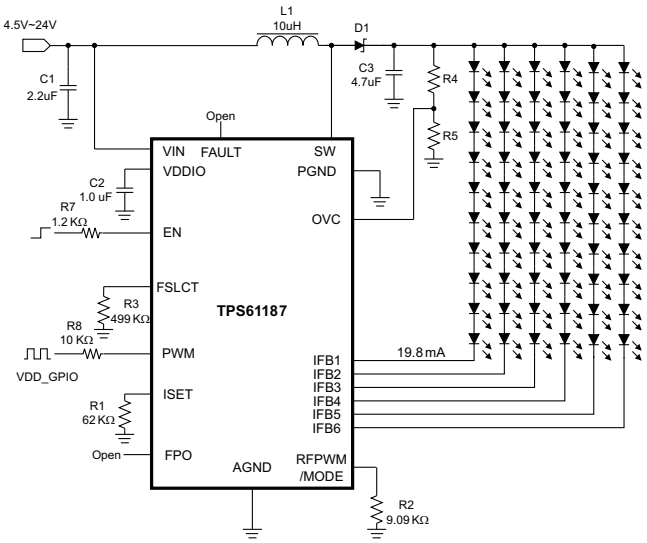


Figure 1. Typical Application – Phase Shift PWM Mode

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE INFORMATION(1)

PACKAGE	PACKAGE MARKING
TPS61187RTJ	TPS61187

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE		UNIT
		MIN	MAX	
Voltage range (2)	VIN, FAULT	–0.3	24	V
	FPO	–0.3	7	V
	SW	–0.3	40	V
	EN, PWM, IFB1 to IFB4	–0.3	20	V
	VDDIO	–0.3	3.7	V
	All other pins	–0.3	3.6	V
HBM ESD rating			4	kV
MM ESD rating			200	V
CDM ESD rating			1.5	kV
Continuous power dissipation		See Thermal Information Table		
Operating junction temperature range		–40	150	°C
Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over ooperating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	4.5		24	V
V_{OUT}	Output voltage range	VIN		38	V
L1	Inductor, 600 kHz ~ 1 MHz switching frequency	10		22	µH
L1	Inductor, 300 kHz ~ 600 kHz swtching frequency	22		47	µH
C_I	Input capacitor	1			µF
C_O	Output capacitor	1.0	4.7	10	µF
F_{PWM_O}	IFBx PWM dimming frequency - frequency programmable mode	0.1		22(1)	KHz
F_{PWM_O}	IFBx PWM dimming frequency - direct PWM mode	0.1		50	KHz
F_{PWM_I}	PWM input signal frequency	0.1		22	KHz
F_{BOOST}	Boost regulator switching frequency	300		1000	KHz
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) 5 µs min pulse on time.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS61187 RTJ 20	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	39.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	34.0	
θ_{JB}	Junction-to-board thermal resistance	9.9	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	9.5	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, PWM/EN = high, IFB current = 20mA, IFB voltage = 500mV, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		4.5		24	V
I_{q_VIN}	Operating quiescent current into Vin	Device enable, switching 1MHz and no load, V_{IN} = 24 V			4.0	mA
VDDIO	VDDIO pin output voltage	Iload = 5 mA	3.0	3.3	3.6	V
I_{SD}	Shutdown current	V_{IN} = 12 V , EN = low			11	µA
		V_{IN} = 24 V, EN = low			16	
V_{IN_UVLO}	V_{IN} under-voltage lockout threshold	V_{IN} ramp down			3.50	V
		V_{IN} ramp up			3.75	
V_{IN_Hys}	V_{IN} under-voltage lockout hysterisis			250		mV
PWM						
V_H	EN Logic high threshold	EN	2.1			V
V_L	EN Logic low threshold	EN			0.8	
V_H	PWM Logic high threshold	PWM	2.1			
V_L	PWM Logic low threshold	PWM			0.8	
R_{PD}	Pull down resistor on PWM and EN		400	800	1600	kΩ
CURRENT REGULATION						
V_{ISET}	ISET pin voltage		1.204	1.229	1.253	V
K_{ISET}	Current multiplier			980		
I_{FB}	Current accuracy	I_{ISET} = 20 µA, 0°C to 70°C	–2%		2%	
		I_{ISET} = 20 µA, –40°C to 85°C	–2.3%		2.3%	
K_m	$(I_{max}–I_{min}) / I_{AVG}$	I_{ISET} = 20 µA		1.3%		
I_{leak}	IFB pin leakage current	IFB voltage = 15 V, each pin		2	5	µA
		IFB voltage = 5 V, each pin		1	2	
I_{IFB_max}	Current sink max output current	IFB = 350 mV	30			mA
f_{dim}	PWM dimming frequency	R_{FPWM} = 9.09 kΩ		20		kHz
BOOST OUTPUT REGULATION						
V_{IFB_L}	Output voltage up threshold	Measured on $V_{IFB(min)}$		350		mV
V_{IFB_H}	Ouput voltage down threshold	Measured on $V_{IFB(min)}$		650		mV
POWER SWITCH						
R_{PWM_SW}	PWM FET on-resistance	V_{IN} = 12 V		0.25	0.35	Ω
I_{LN_NFET}	PWM FET leakage current	V_{SW} = 40 V, T_A = 25°C			2	µA

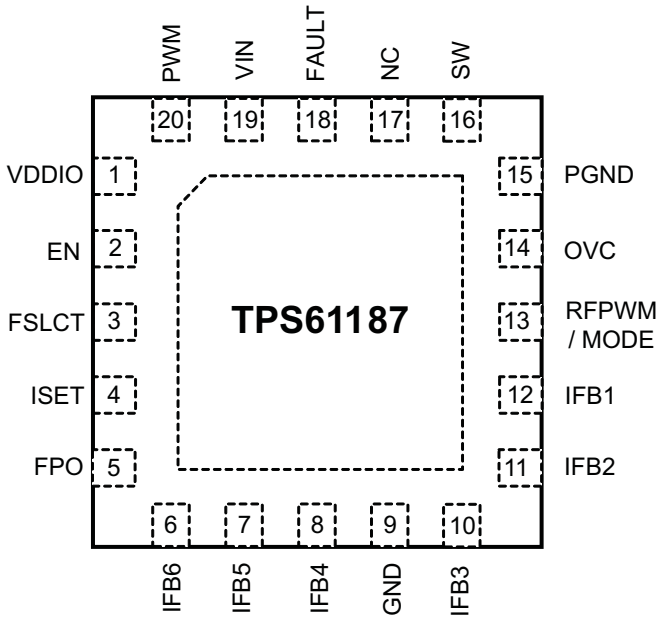
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 12V, PWM/EN = high, IFB current = 20mA, IFB voltage = 500mV, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_S	Oscillator frequency	R_{FSW} = 499 kΩ	0.8	1.0	1.2	MHz
D_{max}	Maximum duty cycle	IFB = 0		94%		
OC, SC, OVP AND SS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	2.0		3.0	A
V_{CLAMP_TH}	Ouput voltage clamp program threshold		1.90	1.95	2.00	V
V_{OVP_IFB}	IFB overvoltage threshold	Measured on the IFBx pin, IFB on	12	13.5	15	V
FPO, FAULT						
V_{FPO_L}	FPO Logic low voltage	$I_{\_SOURCE}$ = 0.5 mA			0.4	V
V_{FAULT_HIGH}	Fault high voltage	Measured as $V_{IN} – V_{FAULT}$		0.1		V
V_{FAULT_LOW}	Fault low voltage	Measured as $V_{IN} – V_{FAULT}$, Sink, 10 µA	6	8	10	V
I_{FAULT}	Maximum sink current	$V_{IN} – V_{FAULT}$ = 0 V		20		µA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			150		°C
	Thermal shutdown hysteresis			15		

DEVICE INFORMATION

20 PIN 4mm × 4mm RTJ PACKAGE
TOP VIEW



PowerPAD information goes here.

PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
VDDIO	1	Internal pre_regulator. Connect a 1.0 µF ceramic capacitor to VDDIO.
EN	2	Enable
FSLCT	3	Switching frequency selection pin. Use a resistor to set the frequency between 300kHz to 1.0MHz
ISET	4	Full-scale LED current set pin. Connecting a resistor to the pin programs the current level.
FPO	5	Fault protection output to indicate fault conditions including OVP, OC, and OT
IFB1 to IFB6	6,7,8, 10,11,12	Regulated current sink input pins
GND	9,	Analog ground
RFPWM / MODE	13	Dimming frequency program pin with an external resistor / mode selection, see(1)
OVC	14	Over-voltage clamp pin / voltage feedback, see (1)
PGND	15	Power ground
SW	16	Drain connection of the internal power FET
NC	17	No connection
FAULT	18	Fault pin to drive external ISO FET
VIN	19	Supply input pin
PWM	20	PWM signal input pin

(1) See Application Information section for details.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

TITLE	DESCRIPTION	FIGURE
Efficiency vs Load current by output voltage	V_{IN} = 12 V, V_{OUT} = 28 V, 32 V, 36 V, L = 10 µH	Figure 2
Efficiency vs Load current by input voltage	V_{OUT} = 32 V , V_{IN} = 8 V, 12 V, 24 V, L = 10 µH	Figure 3
Efficiency vs PWM duty	V_{OUT} = 32 V , V_{IN} = 8 V, 12 V, 24 V, F_{DIM} = 200 Hz, L = 10 µH, R_{ISET} = 62 kΩ	Figure 4
Dimming linearity	V_{OUT} = 32 V, V_{IN} = 8 V, 12 V, 24 V, F_{DIM} = 20 KHz, L = 10 µH, R_{ISET} = 62 kΩ	Figure 5
Dimming linearity	V_{OUT} = 32 V, V_{IN} = 8 V, 12 V, 24 V, F_{DIM} = 200 Hz, L = 10 µH, R_{ISET} = 62 kΩ	Figure 6
Boost switching frequency	V_{IN} = 12 V, V_{OUT} = 33.8 V, L = 10 µH, R_{ISET} = 62 kΩ	Figure 7
Phase shift dimming frequency	V_{IN} = 12 V, V_{OUT} = 33.8 V, L = 10 µH, R_{ISET} = 62 kΩ	Figure 8
Switch waveform	V_{IN} = 8 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 100%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 9
Switch waveform	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 100%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 10
Phase shift PWM dimming F_{DIM} = 200Hz, duty = 50%	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 45%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 11
Phase shift PWM dimming F_{DIM} = 20KHz, duty = 50%	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 51%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 12
Output ripple of Phase shift PWM dimming	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 50%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 13
Output ripple of Phase shift PWM dimming	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 70%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 14
Start up waveform	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 100%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 15
Start up waveform	V_{IN} = 12 V, V_{OUT} = 33.8 V, F_{DIM} = 20 kHz, Duty = 50%, L = 10 µH, R_{ISET} = 62 kΩ	Figure 16

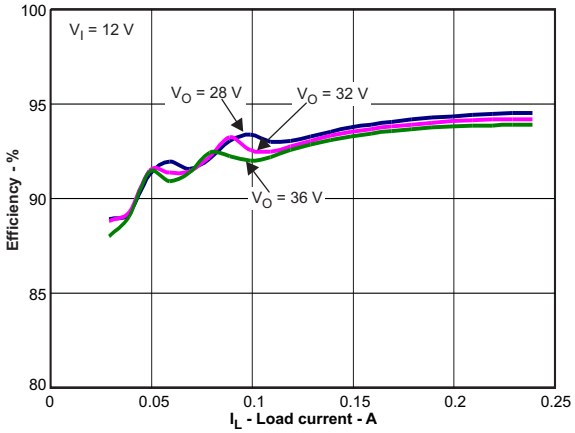


Figure 2. Efficiency

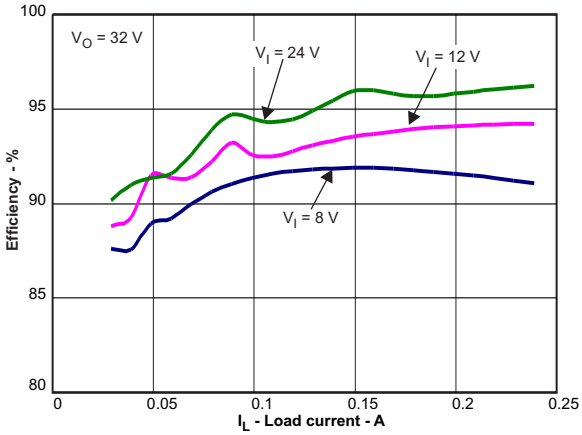


Figure 3. Efficiency

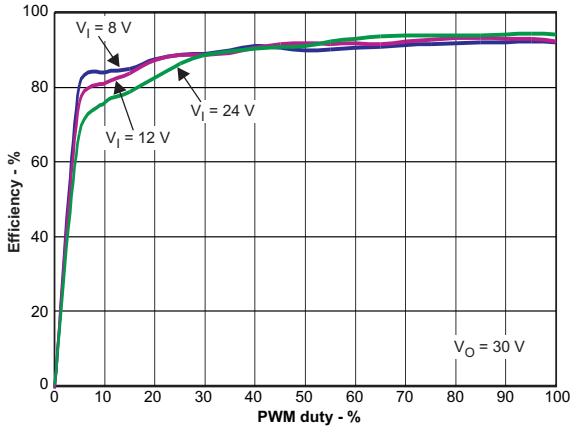


Figure 4. Efficiency

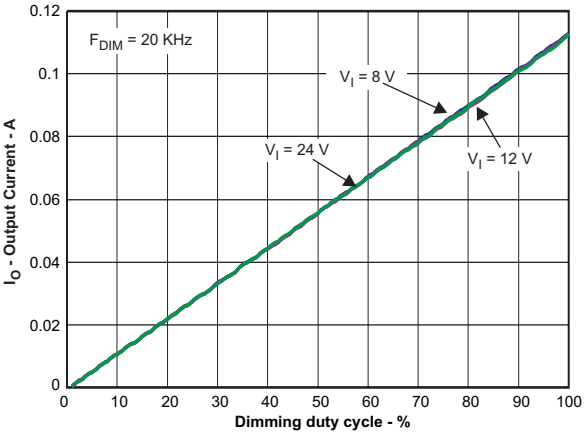


Figure 5. Output Current

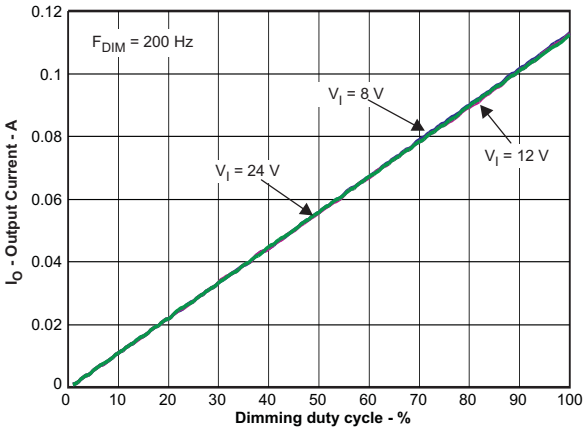


Figure 6. Output Current

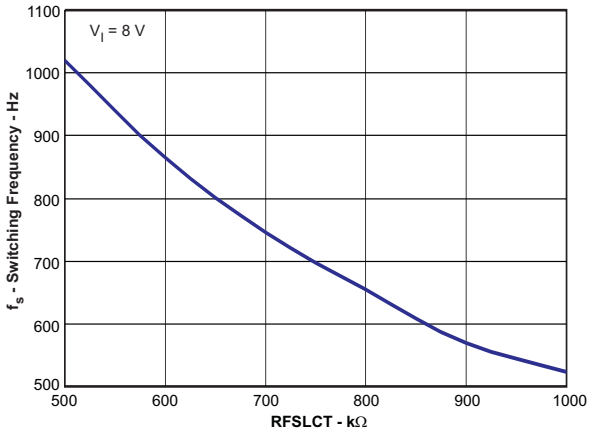


Figure 7. Switching Frequency

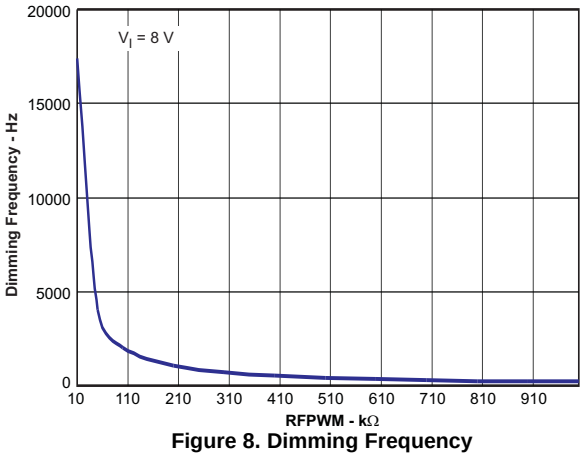


Figure 8. Dimming Frequency

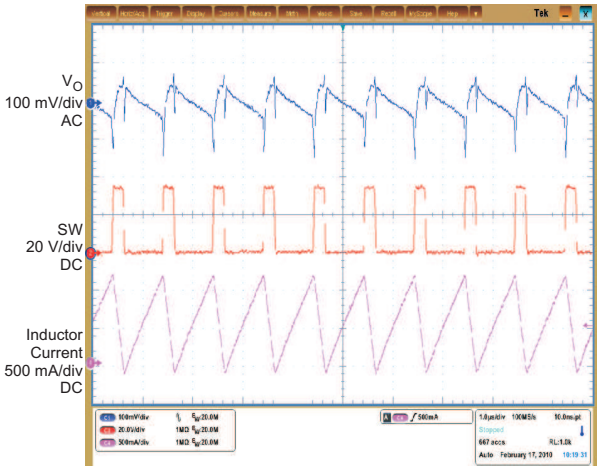


Figure 9. Switch Waveform

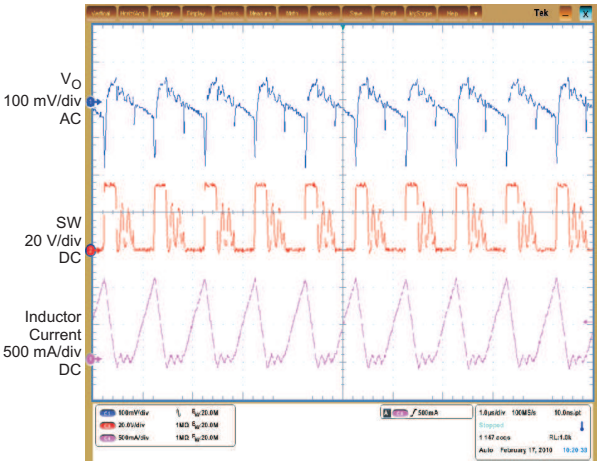


Figure 10. Switch Waveform

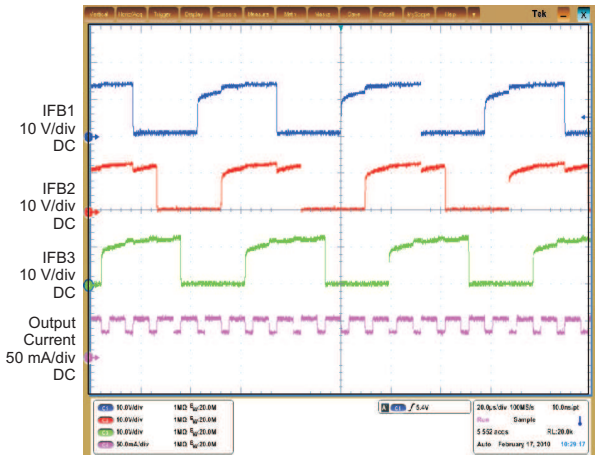


Figure 11. Phase Shift Waveform

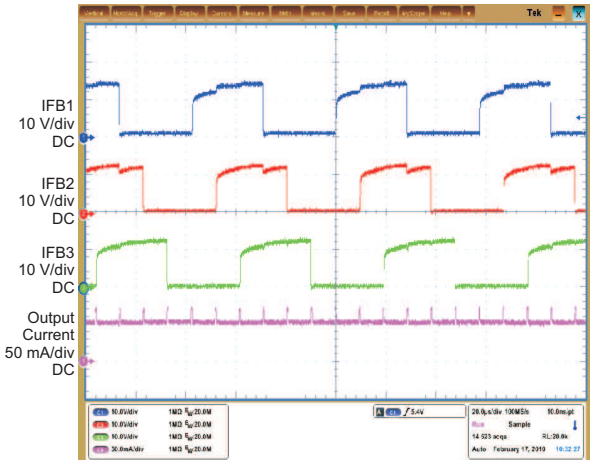


Figure 12. Phase Shift Waveform

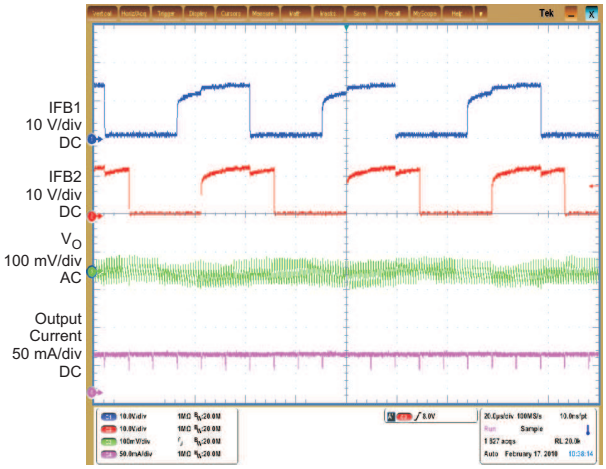


Figure 13. Output Ripple Waveform

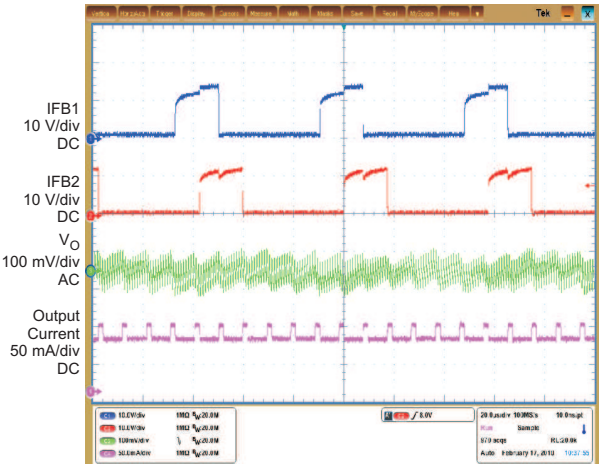


Figure 14. Output Ripple Waveform

Figure 15. Start Up Waveform

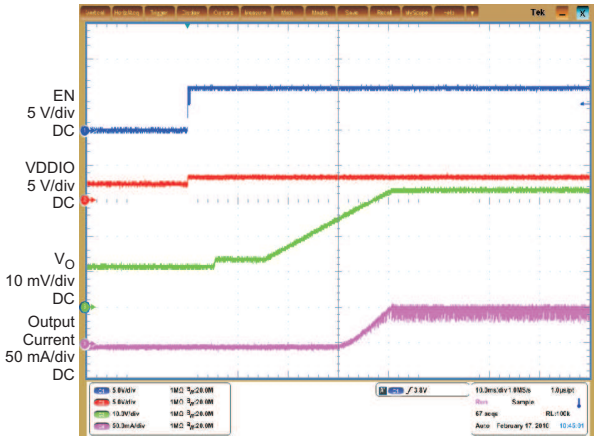
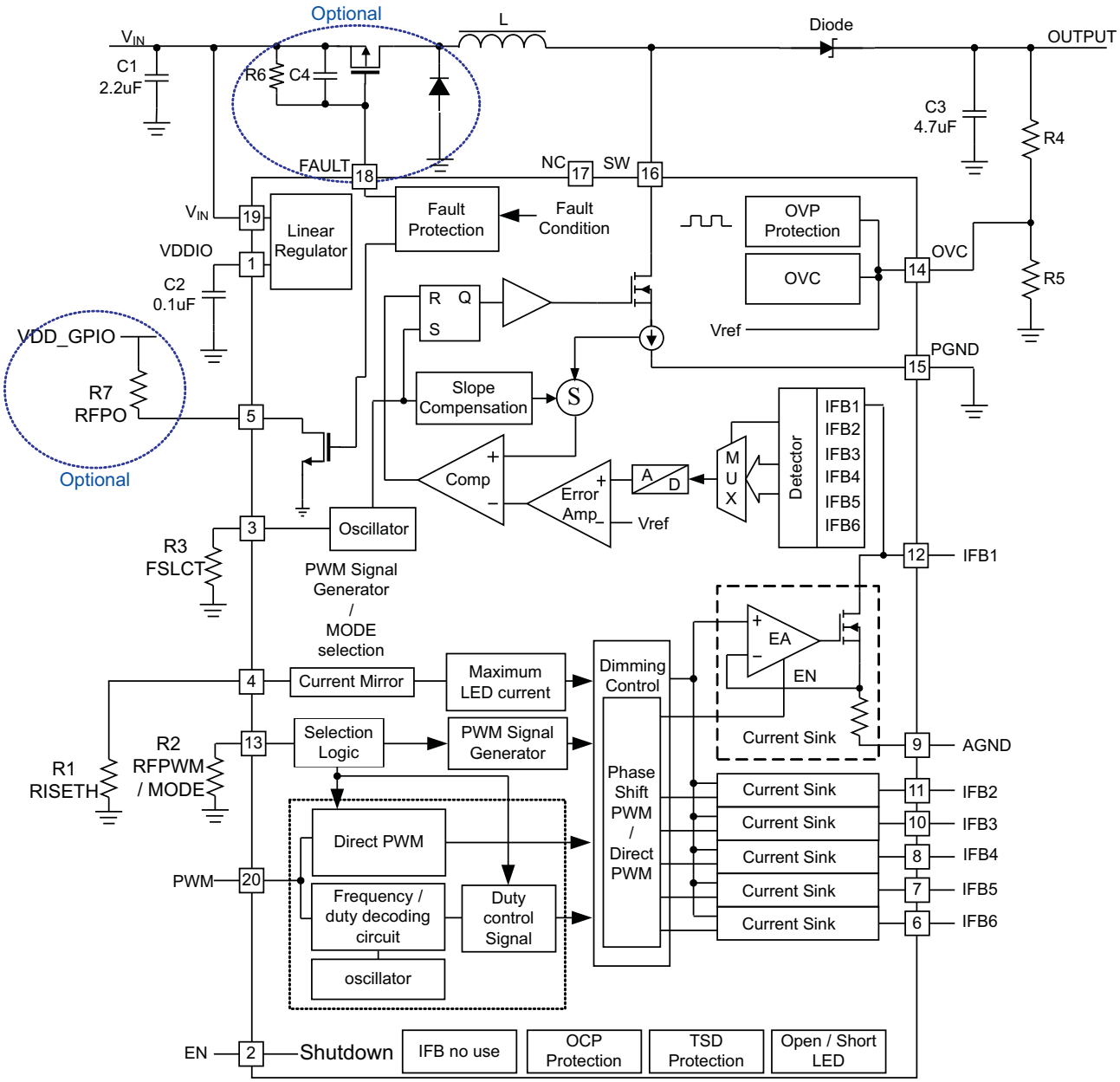


Figure 16. Start Up Waveform

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

NORMAL OPERATION

The TPS61187 is a high efficiency, high output voltage white LED driver for notebook panel backlighting applications. The advantages of white LEDs compared to CCFL backlights are higher power efficiency and lower profile design. Due to the large number of white LEDs required to provide backlighting for medium to large display panels, the LEDs must be arranged in parallel strings of several LEDs in series. Therefore, the backlight driver for battery powered systems is almost always a boost regulator with multiple current sink regulators. Having more white LEDs in series reduces the number of parallel strings and therefore improves overall current matching. However, the efficiency of the boost regulator declines due to the need for high output voltage. Also, there must be enough white LEDs in series to ensure the output voltage stays above the input voltage range.

The TPS61187 IC has integrated all of the key function blocks to power and control up to 60 white LEDs. The device includes a 40 V / 2 A boost regulator, six 30 mA current sink regulators, and a protection circuit for over-current, over-voltage, Open LED, Short LED, and output short circuit failures.

The TPS61187 integrates auto phase shifted PWM dimming methods with the PWM interface to reduce the output ripple voltage and audible noise. An optional direct PWM mode is user selectable through the MODE selection function.

SUPPLY VOLTAGE

The TPS61187 IC has a built-in linear regulator to supply the IC analog and logic circuit. The VDDIO pin, output of the regulator, is connected to a 1 µF bypass capacitor for the regulator to be controlled in a stable loop. VDDIO does not have high current sourcing capability for external use but it can be tied to the EN pin for start up.

BOOST REGULATOR AND PROGRAMMABLE SWITCH FREQUENCY (FSCLT)

The fixed-frequency PWM boost converter uses current-mode control and has integrated loop compensation. The internal compensation ensures stable output over the full input and output voltage ranges assuming the recommended inductance and output capacitance values shown in the Typical Application – Phase Shift PWM Mode figure are used. The output voltage of the boost regulator is automatically set by the IC to minimize voltage drop across the IFB pins. The IC regulates the lowest IFB pin to 350 mV, and consistently adjusts the boost output voltage to account for any changes in LED forward voltages. If the input voltage is higher than the sum of the white LED forward voltage drops (e.g., at low duty cycles), the boost converter is not able to regulate the output due to its minimum duty cycle limitation. In this case, increase the number of WLEDs in series or include series ballast resistors in order to provide enough headroom for the converter to boost the output voltage. Since the TPS61187 integrates a 2.0A/40V power MOSFET, the boost converter can provide up to a 38 V output voltage.

The TPS61187 switching frequency can be programmed between 300 kHz to 1.0MHz by the resistor value on the FSLCT pin according to Equation 1:

$$F_{SW} = \frac{5 \times 10^{11}}{R_{FSLCT}} \quad (1)$$

Where: R_{FSLCT} = FSCLT pin resistor

See Figure 7 for boost converter switching frequency adjustment resistor R_{FSLCT} selection.

The adjustable switching frequency feature provides the user with the flexibility of choosing a faster switching frequency, and therefore, an inductor with smaller inductance and footprint or slower switching frequency, and therefore, potentially higher efficiency due to lower switching losses. Use Equation 1 or refer to Table 1 to select the correct value:

Table 1. R_{FSLCT} Recommendations

R_{FLCT}	F_{SW}
833K	600 KHz
625K	800 KHz
499K	1 MHz

LED CURRENT SINKS

The six current sink regulators embedded in the TPS61187 can be collectively configured to provide up to a maximum of 30 mA each. These six specialized current sinks are accurate to within ±2% max for currents at 20 mA, with a string-to-string difference of ±1.5% typical.

The IFB current must be programmed to the highest WLED current expected using the ISETH pin resistor and Equation 2.

$$I_{FB} = \frac{V_{ISETH}}{R_{ISETH}} \times K_{ISET} \quad (2)$$

Where:

K_{ISET} = 980 (current multiple)
V_{ISETH} = 1.229V (ISETH pin voltage)
R_{ISETH} = ISETH pin resistor

ENABLE AND STARTUP

The internal regulator which provides VDDIO wakes up as soon as V_{IN} is applied even when EN is low. This allows the IC to start when EN is tied to the VDDIO pin. VDDIO does not come to full regulation until EN is high. The TPS61187 checks the status of all current feedback channels and shuts down any unused feedback channels. It is recommended to short the unused channels to ground for faster startup.

After the device is enabled, if the PWM pin is left floating, the output voltage of the TPS61187 regulates to the minimum output voltage. Once the IC detects a voltage on the PWM pin, the TPS61187 begins to regulate the IFB pin current, as pre-set per the ISETH pin resistor, according to the duty cycle of the signal on the PWM pin. The boost converter output voltage rises to the appropriate level to accommodate the sum of the white LED string with the highest forward voltage drops plus the headroom of the current sink at that current.

Pulling the EN pin low shuts down the IC, resulting in the IC consuming less than 11 µA in shutdown mode.

IFB PIN UNUSED

The TPS61187 has open/short string detection. For an unused IFB string, simply short it to ground or leave it open. Shorting unused IFB pins to ground for faster startup is recommended.

BRIGHTNESS DIMMING CONTROL

The TPS61187 has auto phase shifted PWM dimming control with the PWM control interface.

The internal decoder block detects duty information from the input PWM signal, saves it in an eight bit register and delivers it to the output PWM dimming control circuit. The output PWM dimming control circuit turns on/off six output current sinks at the PWM frequency set by RFPWM and the duty cycle from the decoder block.

The TPS61187 also has direct PWM dimming control with the PWM control interface. In direct PWM mode, each current sink turns on/off at the same frequency and duty cycle as the input PWM signal. See the *Mode Selection* section for dimming mode selection.

When in phase shifted PWM mode, it is recommended to insert a series resistor of 10kΩ to 20kΩ value close to PWMIN pin. This resistor together with an internal capacitor forms a low pass R-C filter with 30ns to 60ns time constant. This prevents possible high frequency noises being coupled into the input PWM signal and causing interference to the internal duty cycle decoding circuit. However, it is not necessary for direct PWM mode since the duty cycle decoding circuit is disabled during the direct PWM mode.

ADJUSTBLE PWM DIMMING FREQUENCY AND MODE SELECTION (R_FPWM / MODE)

The TPS61187 can operate in auto phase shift mode or direct PWM mode. Tying the RFPWM/MODE pin to VDDIO forces the IC to operate in direct PWM mode. A resistor between the RFPWM/MODE pin and ground sets the IC into auto phase shift mode and the value of the resistor determines the PWM dimming frequency. Use Equation 3 or refer to Table 2 to select the correct value:

$$F_{DIM} = \frac{1.818 \times 10^8}{R_{FPWM}} \quad (3)$$

Where: R_{FPWM} = RFPWM pin resistor

Table 2. R_{FPWM} Recommendations

R_{FPWM}	F_{DIM}
866 kΩ	210 Hz
432 kΩ	420 Hz
174 kΩ	1.05 kHz
9.09 kΩ	20 kHz

MODE SELECTION – PHASE SHIFT PWM OR DIRECT PWM DIMMING

The phase shift PWM dimming method or direct PWM dimming method can be selected through the RFPWM pin. By attaching an external resistor to the RFPWM pin, the default phase shift PWM mode can be selected. To select direct PWM mode, the RFPWM pin needs to be tied to the VDDIO pin. The RFPWM/MODE pin can be noise sensitive when R2 has high impedance. In this case, careful layout or a parallel bypassing capacitor improves noise sensitivity but the value of the parallel capacitor may not exceed 33 pF for oscillator stability.

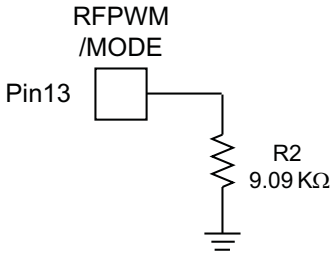


Figure 17. Phase Shift PWM Dimming Mode Selection

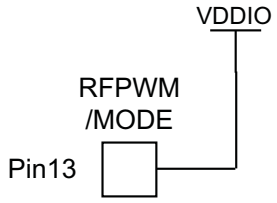


Figure 18. Direct PWM Dimming Mode Selection

PHASE SHIFT PWM DIMMING

In phase shift PWM mode, all current feedback channels are turned on and off at F_{DIM} frequency with a constant delay. However, the number of used channels and PWM dimming frequency determine the delay time between two neighboring channels per Equation 4.

$$T\_delay = \frac{1}{n \times F_{DIM}} \quad (4)$$

Where: n is the number of used channels

F_{DIM} is the PWM dimming frequency which is determined by the value of R_{FPWM} on the RFPWM pin. Figure 19 provides the detailed timing diagram of the phase shift PWM dimming mode.

In phase shift PWM mode, the internal decoder converts the duty cycle information from the applied PWM signal at the PWM pin into an 8-bit digital signal and stores it into a register. The integrated dimming control circuit reconstructs the PWM duty cycle per the register value and sends it to each of the current sinks. In order to avoid any flickering while the duty cycle information is reconstructed from the register, one LSB (1/256) of duty cycle hysteresis is included which results in 1/256 resolution when incrementing the applied signal's duty cycle but 2/256 resolution when decrementing the duty cycle.

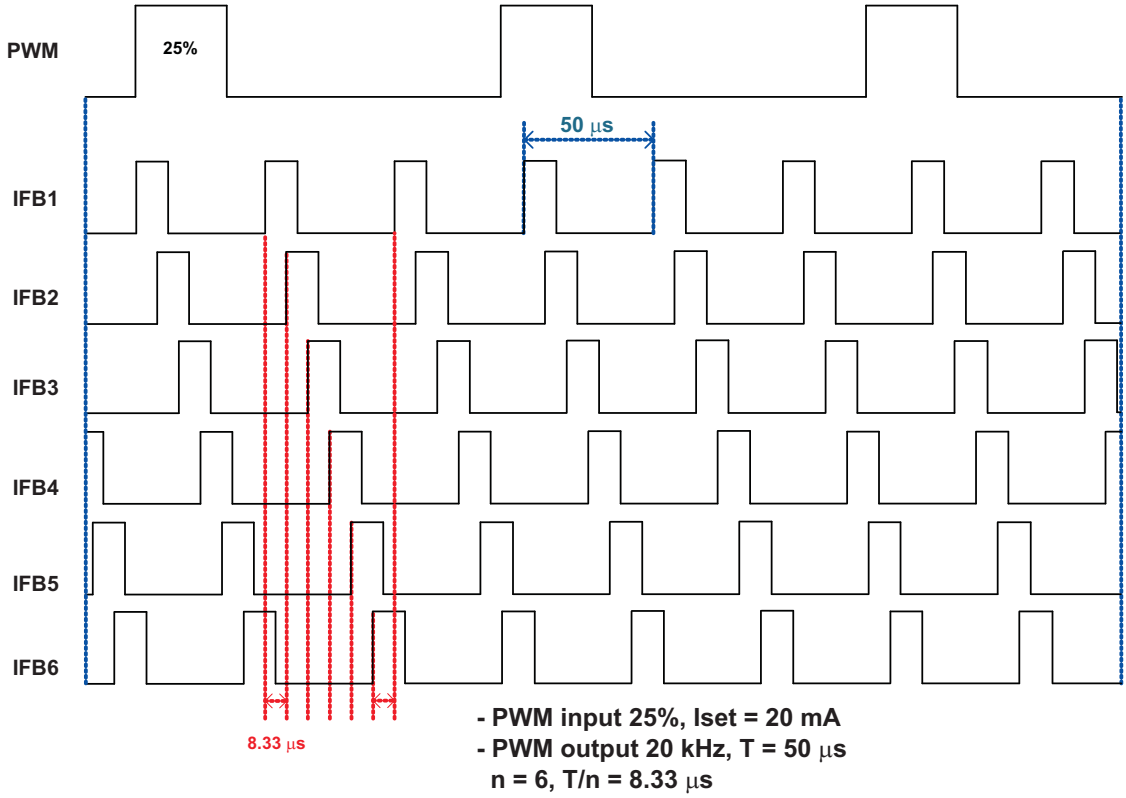


Figure 19. Phase Shift PWM Dimming Timing Diagram

DIRECT PWM DIMMING

In direct PWM mode, all current feedback channels are turned on and off and are synchronized with the input PWM signal.

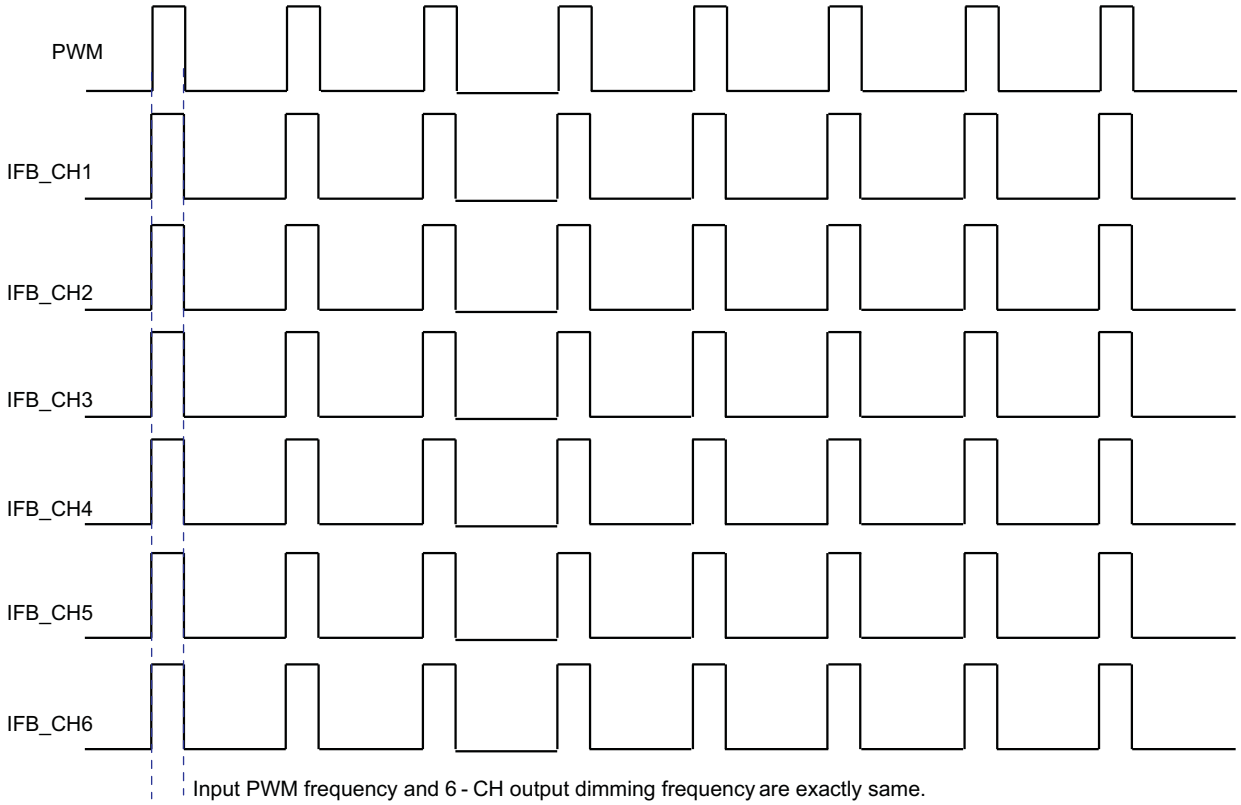


Figure 20. Direct PWM Dimming Timing Diagram

OVER VOLTAGE CLAMP / VOLTAGE FEEDBACK (OVC / FB)

The correct divider ratio is important for optimum operation of the TPS61187. Use the following guidelines to choose the divider value. It can be noise sensitive if R_{upper} and R_{down} have high impedance. Careful layout is required. Also, choose lower resistance values for R_{upper} and R_{down} when power dissipation allows.

Step1. Determine the maximum output voltage, V_O, for the system according to the number of series WLEDs.

Step2. Select an R_{upper} resistor value (1 MΩ for a typical application; a lower value such as 100 kΩ for a noisy environment).

Step3. Calculate R_{down} using Equation 5.

$$V_{OVP} = \left(\frac{R_{upper}}{R_{down}} + 1 \right) \times V_{OV\_TH} \quad (5)$$

Where: V_{OV_TH} = 1.95 V

When the IC detects that the OVC pin exceeds 1.95 V typical, indicating that the output voltage is over the set threshold point, the OVC circuitry clamps the output voltage to the set threshold.

CURRENT SINK OPEN PROTECTION

For the TPS61187, if one of the WLED strings is open, the IC automatically detects and disables that string. The IC detects the open WLED string by sensing no current in the corresponding IFB pin. As a result, the IC deactivates the open IFB pin and removes it from the voltage feedback loop. Subsequently, the output voltage drops and is regulated to the minimum voltage required for the connected WLED strings. The IFB current of the connected WLED strings remains in regulation.

If any IFB pin voltage exceeds the IFB over-voltage threshold (13.5 V typical), the IC turns off the corresponding current sink and removes this IFB pin from the regulation loop. The current regulation of the remaining IFB pins is not affected. This condition often occurs when there are several shorted WLEDs in one string. WLED mismatch typically does not create large voltage differences among WLED strings.

The IC only shuts down if it detects that all of the WLED strings are open. If an open string is reconnected again, a power-on reset (POR) or EN pin toggling is required to reactivate a previously deactivated string.

OVER CURRENT AND SHORT CIRCUIT PROTECTION

The TPS61187 has a pulse-by-pulse over-current limit of 2.0 A (min). The PWM switch turns off when the inductor current reaches this current threshold. The PWM switch remains off until the beginning of the next switching cycle. This protects the IC and external components during on overload conditions. When there is a sustained over-current condition, the IC turns off and requires a POR or EN pin toggling to restart. Under severe over-load and/or short circuit conditions, the boost output voltage can be pulled below the required regulated voltage to keep all of the white LEDs operating. Under this condition, the current flows directly from input to output through the inductor and schottky diode. To protect the TPS61187, the device shuts down immediately. The IC restarts after input POR or EN pin toggling.

THERMAL PROTECTION

When the junction temperature of the TPS61187 is over 150°C, the thermal protection circuit is triggered and shuts down the device immediately. Only a POR or EN pin toggling clears the protection and restarts the device.

APPLICATION INFORMATION

INDUCTOR SELECTION

Because selection of the inductor affects power supply steady state operation, transient behavior, and loop stability, the inductor is the most important component in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, dc resistance, and saturation current. The TPS61187 is designed to work with inductor values between 10 µH and 47 µH. A 10 µH inductor is typically available in a smaller or lower profile package, while a 47 µH inductor may produce higher efficiency due to a slower switching frequency and/or lower inductor ripple. If the boost output current is limited by the over-current protection of the IC, using a 10 µH inductor and the highest switching frequency maximizes controller output current capability.

Internal loop compensation for PWM control is optimized for the external component values, including typical tolerances, recommended in Table 3. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0 A value depending on how the inductor vendor defines saturation. In a boost regulator, the inductor dc current can be calculated with Equation 6.

$$I_{DC} = \frac{Vout \times Iout}{Vin \times \eta} \quad (6)$$

Where:

- Vout = boost output voltage
- Iout = boost output current
- Vin = boost input voltage
- η = power conversion efficiency, use 90% for TPS61187 applications

The inductor current peak-to-peak ripple can be calculated with Equation 7.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{Vout - Vin} + \frac{1}{Vin} \right) \times F_S} \quad (7)$$

Where:

- I_{PP} = inductor peak-to-peak ripple
- L = inductor value
- F_S = Switching frequency
- Vout = boost output voltage
- Vin = boost input voltage

Therefore, the peak current seen by the inductor is calculated with Equation 8.

$$I_P = I_{DC} + \frac{I_{PP}}{2} \quad (8)$$

Select an inductor with a saturation current over the calculated peak current. To calculate the worst case inductor peak current, use the minimum input voltage, maximum output voltage, and maximum load current.

Regulator efficiency is dependent on the resistance of its high current path and switching losses associated with the PWM switch and power diode. Although the TPS61187 IC has optimized the internal switch resistances, the overall efficiency is affected by the inductor dc resistance (DCR). Lower DCR improves efficiency. However, there is a trade off between DCR and inductor footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones. Table 3 lists the recommended inductors.

Table 3. Recommended Inductor for TPS61187

	L(µH)	DCR(mΩ)	Isat(A)	Size (L × W × H mm)
TOKO				
A915AY – 4R7M	4.7	38	1.87	5.2 × 5.2 × 3.0
A915AY – 100M	10	75	1.24	5.2 × 5.2 × 3.0
TDK				
SLF6028T – 4R7N1R6	4.7	38	1.87	5.2 × 5.2 × 3.0
SLF6028T – 4R7N1R6	10	75	1.24	5.2 × 5.2 × 3.0

OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet the requirement for output ripple and loop stability. This ripple voltage is related to the capacitance of the capacitor and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated with Equation 9:

$$Cout = \frac{(Vout - Vin) \times Iout}{Vout \times F_S \times Vripple} \quad (9)$$

Where:

Vripple = peak-to-peak output ripple. The additional part of the ripple caused by ESR is calculated using:
Vripple_ESR = Iout x RESR

Due to its low ESR, Vripple_ESR can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used. The controller output voltage also ripples due to the load transient that occurs during PWM dimming. The TPS61187 adopts a patented technology to limit this type of output ripple even with the minimum recommended output capacitance. In a typical application, the output ripple is less than 250 mV during PWM dimming with a 4.7 µF output capacitor. However, the output ripple decreases with higher output capacitances.

ISOLATION FET SELECTION

The TPS61187 provides a gate driver to an external P channel MOSFET which can be turned off during device shutdown or fault condition. This MOSFET can provide a true shutdown function and also protect the battery from output short circuit conditions. The source of the PMOS should be connected to the input, and a pull-up resistor is required between the source and gate of the FET to keep the FET off during IC shutdown. To turn on the isolation FET, the FAULT pin is pulled low and clamped at 8 V below the VBAT pin voltage. During device shutdown or fault condition, the isolation FET is turned off, and the input voltage is applied on the isolation MOSFET. During a short circuit condition, the catch diode (D2 in the typical application circuit) is forward biased when the isolation FET is turned off. The drain of the isolation FET swings below ground. The voltage across the isolation FET can be momentarily greater than the input voltage. Therefore, select a 30 V PMOS for a 24 V maximum input. The on resistance of the FET has a large impact on power conversion efficiency since the FET carries the input voltage. Select a MOSFET with $R_{ds(on)}$ less than 100 mΩ to limit the power losses.

LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in the Typical Application – Phase Shift PWM Mode figure, needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the input ripple seen by the IC. The input capacitor, C1 in the typical application circuit, should also be placed close to the inductor. C2 is the filter and noise decoupling capacitor for the internal linear regulator powering the internal digital circuits. It should be placed as close as possible between the VDDIO and AGND pins to prevent any noise insertion to the digital circuits. The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the pin to the inductor and schottky diode should be kept as short and wide as possible. It is also beneficial to have the ground of the output capacitor C3 close to the PGND pin since there is a large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point, for example on the thermal pad. The thermal pad needs to be soldered on to the PCB and connected to the GND pin of the IC. An additional thermal via can significantly improve power dissipation of the IC.

REVISION HISTORY

Changes from Original (June 2010) to Revision A **Page**

- Changed Typical Application graphic 1
- Changed cermaic capacitor value, attached to VDDIO, from 0.1 to 1.0 µF 5
- Changed bypass capacitor value in SUPPLY VOLTAGE section from 0.1 to 1.0 µF. 10
- Changed BRIGHTNESS DIMMING CONTROL section 11
- Deleted PWM BRIGHTNESS CONTROL INTERFACE section 12

Changes from Revision A (July 2010) to Revision B **Page**

- Changed in ABS MAX table, in row "All other pins", MAX col: from 3.6 to 3.7 2

Changes from Revision B (April 2011) to Revision C **Page**

- Changed From: TPS61187 To: TPS61187RTJ in the PACKAGE INFORMATION table 2
- Added a description paragraph and replaced Figure 19 in the PHASE SHIFT PWM DIMMING section 12

Changes from Revision C (September 2011) to Revision D **Page**

- Changed Figure 2 X axis unit from mA to A 6
- Changed Figure 3 X axis unit from mA to A 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS61187RTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS61187RTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

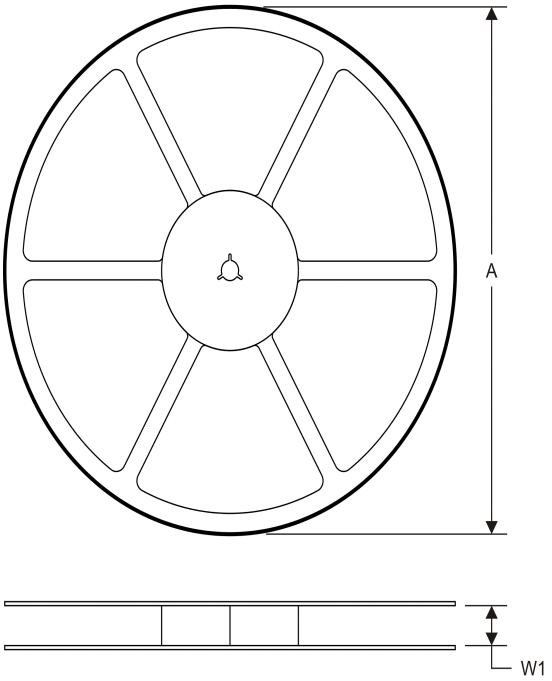
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

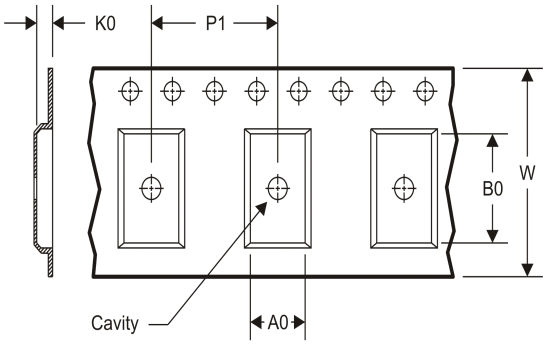
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



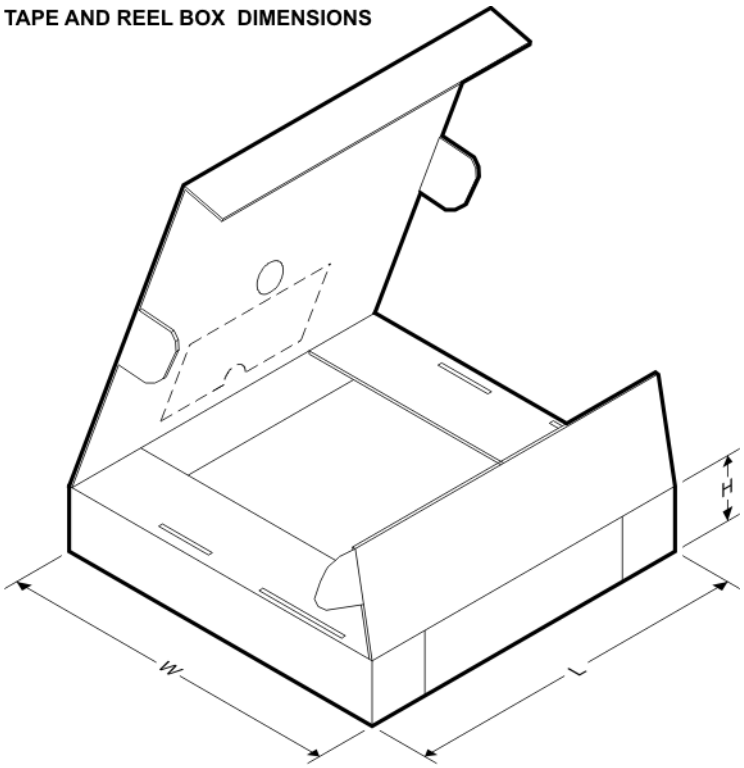
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61187RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS61187RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

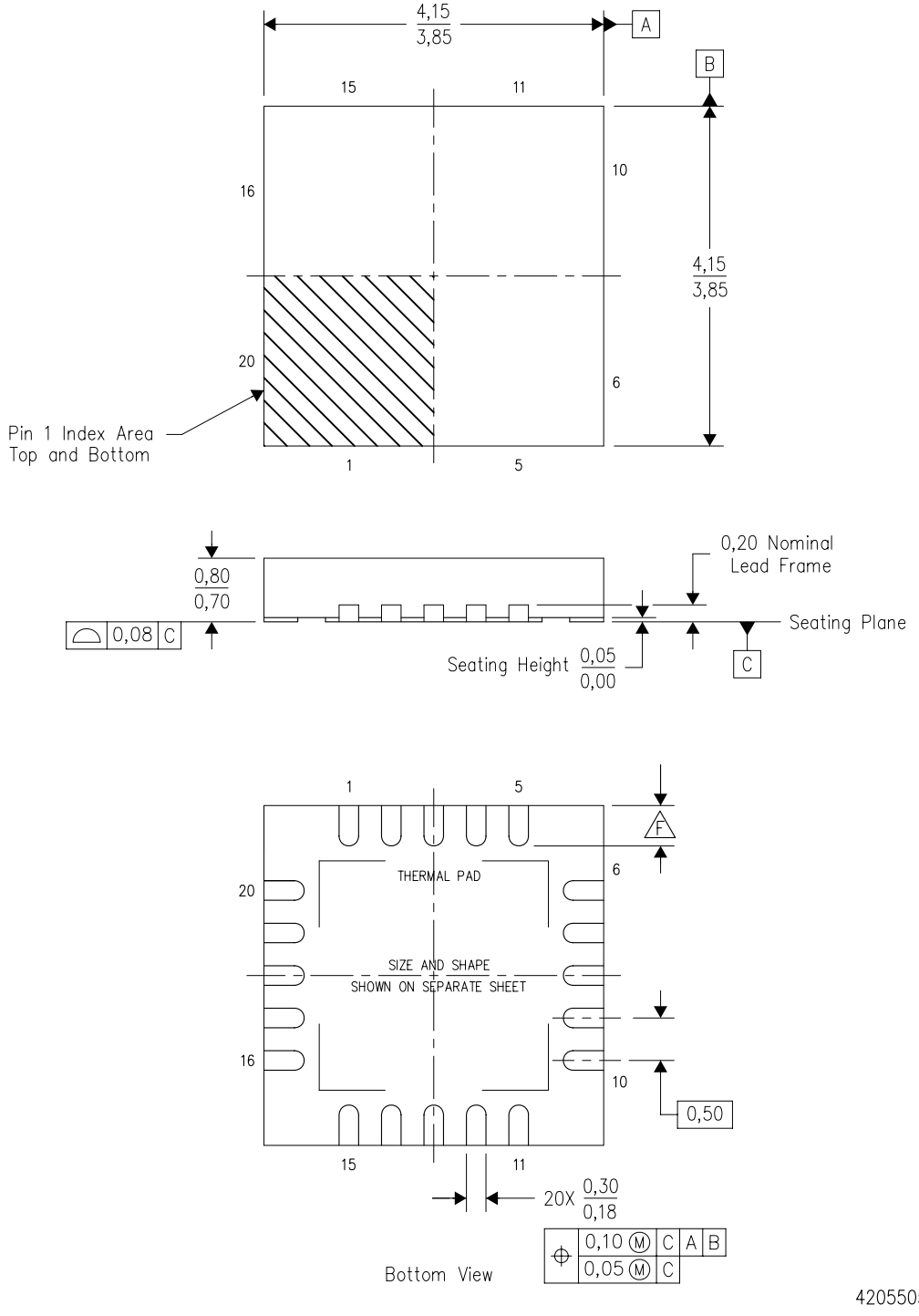
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61187RTJR	QFN	RTJ	20	3000	346.0	346.0	29.0
TPS61187RTJT	QFN	RTJ	20	250	210.0	185.0	35.0

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

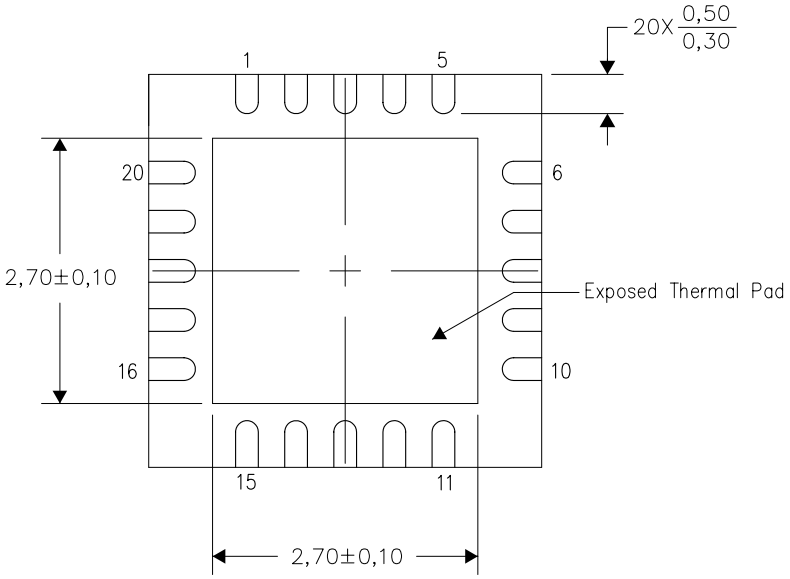
RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



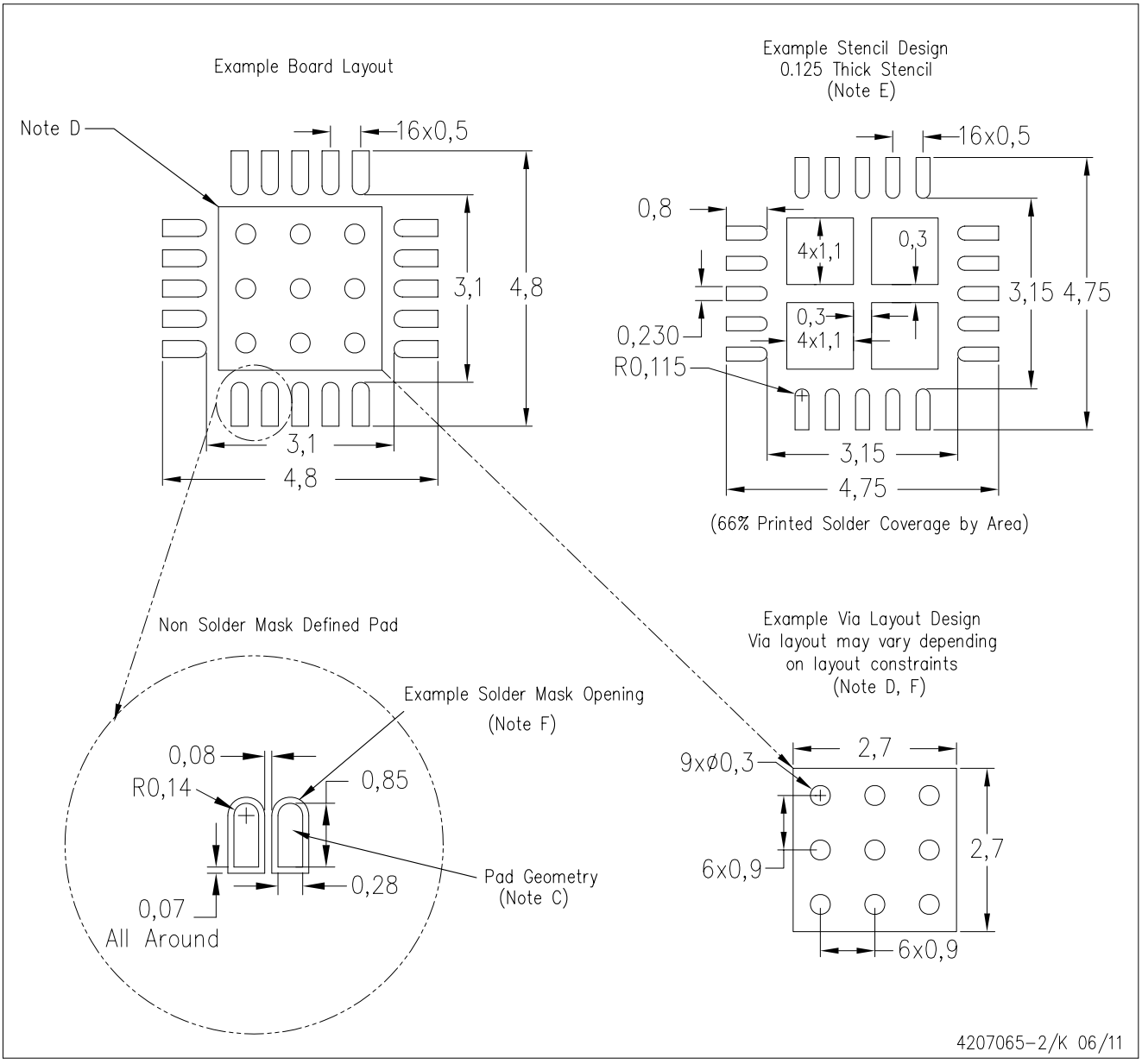
Bottom View

Exposed Thermal Pad Dimensions

4206256–2/Q 07/11

NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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