

4.5-V to 18-V, 3-A OUTPUT SYNCHRONOUS STEP DOWN SWITCHER WITH INTEGRATED FET (SWIFT™)

FEATURES

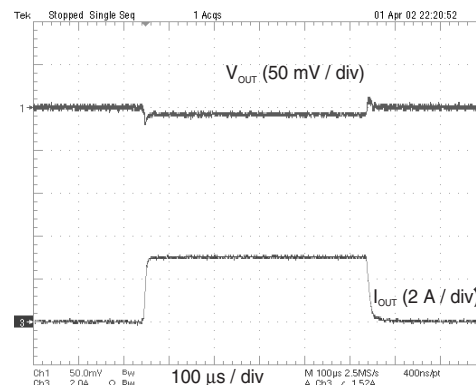
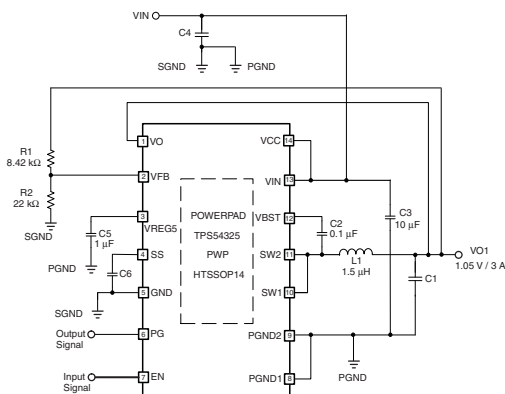
- **D-CAP2™ Mode Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **Wide V_{CC} Input Voltage Range: 4.5 V to 18 V**
- **Wide V_{IN} Input Voltage Range: 2.0 V to 18 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Highly Efficient Integrated FET's Optimized for Lower Duty Cycle Applications**
- 120 m Ω (High Side) and 70 m Ω (Low Side)
- **High Efficiency, less than 10 μ A at shutdown**
- **High Initial Bandgap Reference Accuracy**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **700-kHz Switching Frequency (f_{sw})**
- **Cycle By Cycle Over Current Limit**
- **Power Good Output**

APPLICATIONS

- **Wide Range of Applications for Low Voltage System**
 - Digital TV Power Supply
 - High Definition Blue-ray Disc™ Players
 - Networking Home Terminal
 - Digital Set Top Box (STB)

DESCRIPTION

The TPS54325 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54325 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54325 uses the D-CAP2™ mode control which provides a very fast transient response with no external components. The TPS54325 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V V_{CC} input, and from 2.0-V to 18-V V_{IN} input power supply voltage. The output voltage can be programmed between 0.76 V and 5.5 V. The device also features an adjustable slow start time and a power good function. The TPS54325 is available in the 14 pin HTSSOP package, and designed to operate from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SWIFT, D-CAP2, PowerPAD are trademarks of Texas Instruments.
Blue-ray Disc is a trademark of Blu-ray Disc.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾⁽³⁾	ORDERABLE PART NUMBER	TRANSPORT MEDIA, QUANTITY	ECO PLAN
–45°C to 85°C	PowerPAD™ (HTSSOP) – PWP	TPS54325PWP	Tube	Green (RoHS & no Sb/Br)
		TPS54325PWPR	Tape and Reel, 3000	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) All package options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGSover operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT	
V _I	Input voltage range	V _{IN} , V _{CC} , EN	–0.3 to 20	V
		V _{BST}	–0.3 to 26	V
		V _{BST} (vs SW1, SW2)	–0.3 to 6.5	V
		V _{FB} , V _O , SS, PG	–0.3 to 6.5	V
		SW1, SW2	–2 to 20	V
		SW1, SW2 (10 ns transient)	–3 to 20	V
V _O	Output voltage range	V _{REG5}	–0.3 to 6.5	V
		P _{GND1} , P _{GND2}	–0.3 to 0.3	V
V _{diff}	Voltage from GND to POWERPAD	–0.2 to 0.2	V	
ESD rating	Electrostatic discharge	Human Body Model (HBM)	2	kV
		Charged Device Model (CDM)	500	V
T _J	Operating junction temperature	–40 to 150	°C	
T _{stg}	Storage temperature	–55 to 150	°C	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS⁽¹⁾

(2 oz. trace and copper pad with solder)

PACKAGE	θ _{JA}	T _A = 25°C POWER RATING	T _A = 85°C POWER RATING
PWP	44.5°C/W	2.25 W	0.9 W

- (1) Rating based on JEDEC high thermal conductivity (High K) board with 2 x 2 arrays of thermal vias. See Texas Instruments application report (SLMA002) regarding thermal characteristic of the PowerPAD™ package.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply input voltage range	4.5	18	V
V _{IN}	Power input voltage range	2	18	V

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _I	Input voltage range	V _{BST}	-0.1	24	V
		V _{BST} (vs SW1, SW2)	-0.1	6	
		SS, PG	-0.1	6	
		EN	-0.1	18	
		V _O , V _{FB}	-0.1	5.5	
		SW1, SW2	-1.8	18	
		SW1, SW2 (10 ns transient)	-3	18	
		P _{GND1} , P _{GND2}	-0.1	0.1	
V _O	Output voltage range	V _{REG5}	-0.1	6	V
I _O	Output Current range	I _{VREG5}	0	10	mA
T _A	Operating free-air temperature		-40	85	°C
T _J	Operating junction temperature		-40	125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VCC}	Operating - non-switching supply current	V _{CC} current, T _A = 25°C, EN = 5 V, V _{FB} = 0.8 V		850	1300	μA
I _{VCCSDN}	Shutdown supply current	V _{CC} current, T _A = 25°C, EN = 0 V			10	μA
LOGIC THRESHOLD						
V _{ENH}	EN high-level input voltage	EN	2			V
V _{ENL}	EN low-level input voltage	EN			0.4	V
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V _{FBTH}	V _{FB} threshold voltage	T _A = 25°C, V _O = 1.05 V	757	765	773	mV
		T _A = 0°C to 85°C, V _O = 1.05 V ⁽¹⁾	753		777	
		T _A = -40°C to 85°C, V _O = 1.05 V ⁽¹⁾	751		779	
I _{VFB}	V _{FB} input current	V _{FB} = 0.8 V, T _A = 25°C		0	±0.1	μA
R _{Dischg}	V _O discharge resistance	EN = 0 V, V _O = 0.5 V, T _A = 25°C		50	100	Ω
V_{REG5} OUTPUT						
V _{VREG5}	V _{REG5} output voltage	T _A = 25°C, 6.0 V < V _{CC} < 18 V, 0 < I _{VREG5} < 5 mA	5.3	5.5	5.7	V
V _{LN5}	Line regulation	6.0 V < V _{CC} < 18 V, I _{VREG5} = 5 mA			20	mV
V _{LD5}	Load regulation	0 mA < I _{VREG5} < 5 mA			100	mV
I _{VREG5}	Output current	V _{CC} = 6 V, V _{REG5} = 4.0 V, T _A = 25°C		70		mA
MOSFET						
R _{dsonh}	High side switch resistance	25°C, V _{BST} - SW1, SW2 = 5.5 V		120		mΩ
R _{dsonl}	Low side switch resistance	25°C		70		mΩ
CURRENT LIMIT						
I _{ocl}	Current limit	T _A = -40°C to 85°C ⁽¹⁾	3.5	4.1		A
THERMAL SHUTDOWN						
T _{SDN}	Thermal shutdown threshold	Shutdown temperature ⁽¹⁾		150		°C
		Hysteresis ⁽¹⁾		25		
ON-TIME TIMER CONTROL						
T _{ON}	On time	V _{IN} = 12 V, V _O = 1.05 V		145		ns

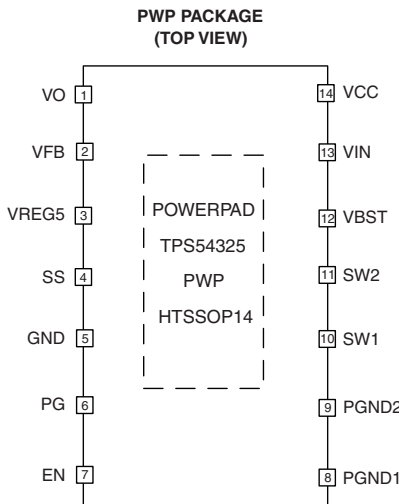
(1) Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T _{OFF(MIN)}	Minimum off time	T _A = 25°C, V _{FB} = 0.7 V		260		ns
SOFT START						
I _{SSC}	SS charge current	V _{SS} = 0 V	1.4	2.0	2.6	μA
I _{SSD}	SS discharge current	V _{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
V _{THPG}	PG threshold	V _{FB} rising (good)	85	90	95	%
		V _{FB} falling (fault)		85		
I _{PG}	PG sink current	PG = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V _{OVP}	Output OVP trip threshold	OVP detect	115	120	125	%
T _{OVPDEL}	Output OVP prop delay			5		μs
V _{UVP}	Output UVP trip threshold	UVP detect	65	70	75	%
		Hysteresis		10		
T _{UVPDEL}	Output UVP delay			0.25		ms
T _{UVPEN}	Output UVP enable delay	Relative to soft-start time		x 1.7		
UVLO						
V _{UVLO}	UVLO threshold	Wake up V _{REG5} voltage	3.45	3.70	3.95	V
		Hysteresis V _{REG5} voltage	0.15	0.25	0.35	

DEVICE INFORMATION



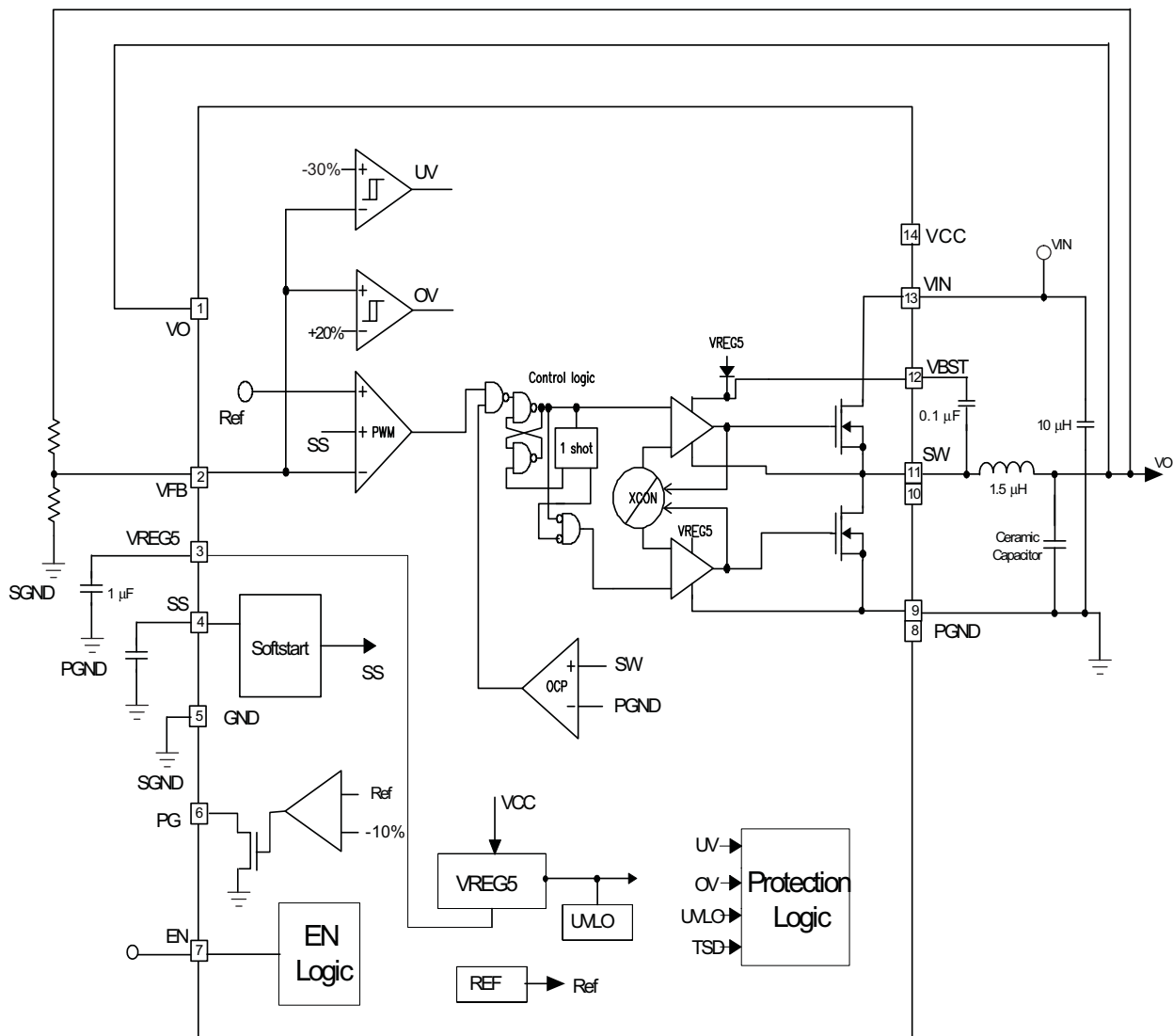
TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
VO	1	Connect to output of converter. This terminal is used for On-Time Adjustment.
VFB	2	Converter feedback input. Connect with feedback resistor divider.
VREG5	3	5.5 V power supply output. A capacitor (typical 1μF) should be connected to GND.
SS	4	Soft-start control. A external capacitor should be connected to GND.
GND	5	Signal ground pin
PG	6	Open drain power good output

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
EN	7	Enable control input
PGND1, PGND2	8, 9	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10, 11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators.
VBST	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN	13	Power input and connected to high side NFET drain
VCC	14	Supply input for 5 V internal linear regulator for the control circuitry
PowerPAD™	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND.

Functional Block Diagram



OVERVIEW

The TPS54325 is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54325 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot timer is set by the converter input voltage, V_{IN} , and the output voltage, V_O , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

PWM Frequency and Adaptive On-Time Control

TPS54325 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54325 runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is V_{OUT}/V_{IN} , the frequency is constant.

Soft Start and Pre-Biased Soft Start

The TPS54325 has an adjustable soft start. When the EN pin becomes high, 2.0- μ A current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in [Equation 1](#). VFB voltage is 0.765 V and SS pin source current is 2 μ A.

$$T_{ss}(ms) = \frac{C6(nF) \cdot V_{ref}}{I_{ss}(\mu A)} = \frac{C6(nF) \cdot 0.765}{2} \quad (1)$$

The TPS54325 contains a unique circuit to prevent current from being pulled from the output during startup in the condition the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage (V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by $(1-D)$, where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (V_O) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Power Good

The TPS54325 has power-good output. The power-good function is activated after soft start has finished. If the output voltage becomes within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. During start up, power good start after 1.7 times soft-start time to avoid a glitch of power-good signal. If the feedback voltage goes under 15% of the target value, the power good signal becomes low after 10 μ s internal delay.

Output Discharge Control

The TPS54325 discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The device discharges outputs using an internal 50- Ω MOSFET which is connected to V_O and PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

Current Protection

The TPS54325 has cycle-by-cycle over current limiting control. The inductor current is monitored during the OFF state and the controller keeps the OFF state when the inductor current is larger than the over current trip level. In order to provide both good accuracy and cost effective solution, the device supports temperature compensated internal MOSFET $R_{DS(on)}$ sensing.

The inductor current is monitored by the voltage between PGND pin and SW1/SW2 pin. In an over current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it will end up with crossing the under voltage protection threshold and shutdown.

Over/Under Voltage Protection

The TPS54325 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 μ s, the device latches off both internal top and bottom MOSFET. This function is enabled approximately 1.7 x soft-start time.

UVLO Protection

The TPS54325 has under voltage lock out protection (UVLO) that monitors the voltage of V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54325 is shut off. This is non-latch protection.

Thermal Shutdown

The TPS54325 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), the device is shut off. This is non-latch protection.

TYPICAL CHARACTERISTICS

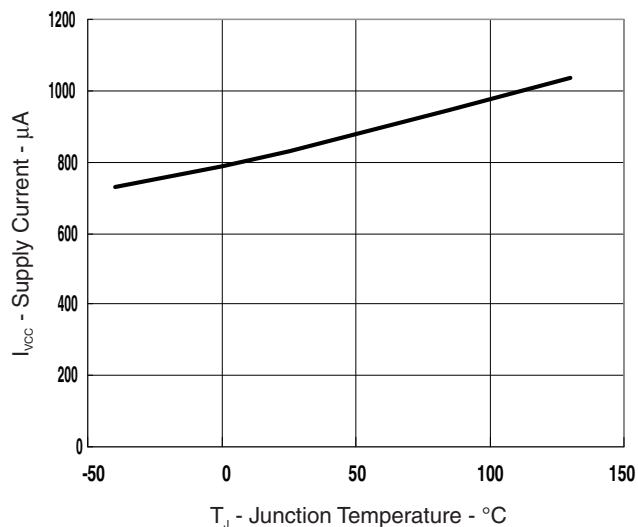


Figure 1. V_{CC} TEMPERATURE vs. JUNCTION TEMPERATURE

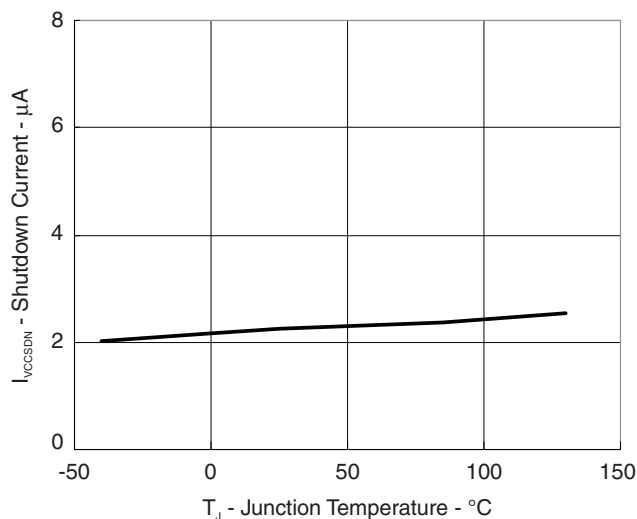


Figure 2. V_{CC} SHUTDOWN CURRENT vs. JUNCTION TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

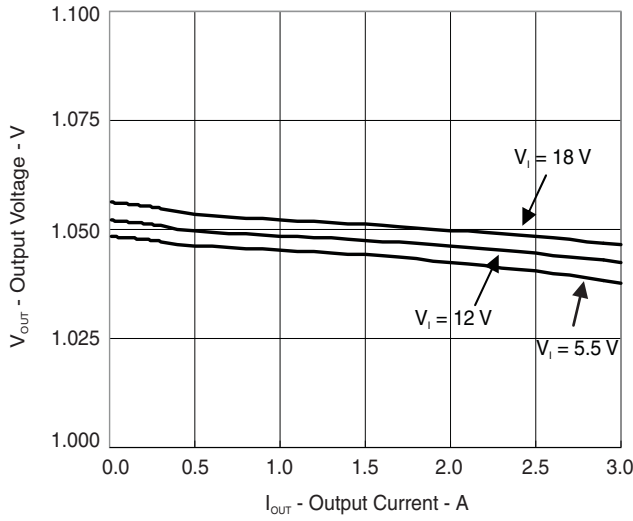


Figure 3. 1.05-V OUTPUT VOLTAGE vs. OUTPUT CURRENT

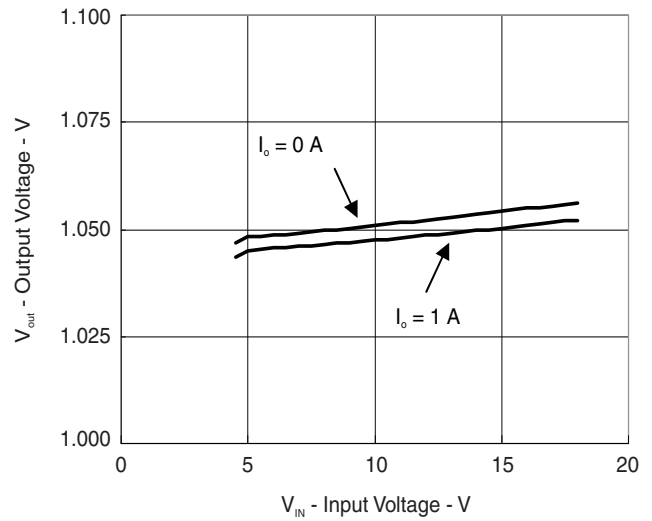


Figure 4. 1.05-V OUTPUT VOLTAGE vs. INPUT VOLTAGE

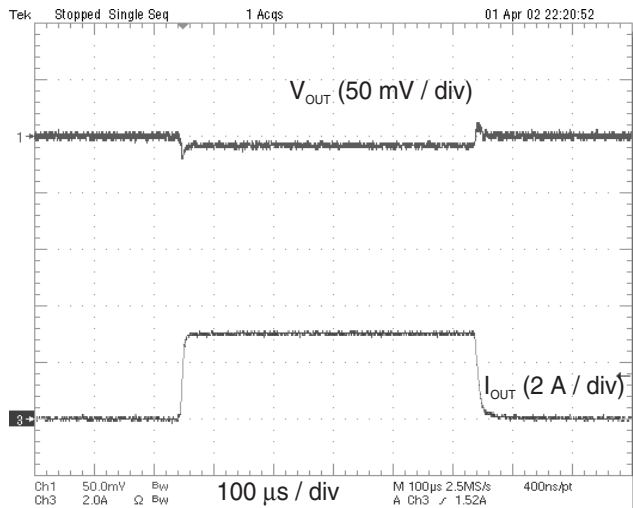


Figure 5. 1.05-V, 0-A TO 3-A LOAD TRANSIENT RESPONSE

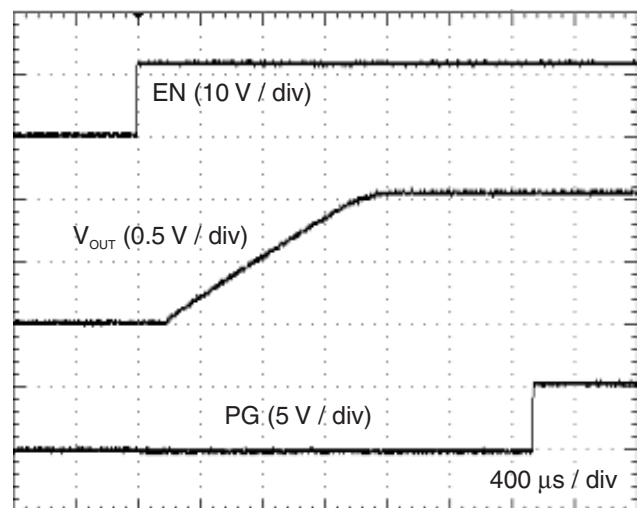


Figure 6. START-UP WAVE FORM

TYPICAL CHARACTERISTICS (continued)

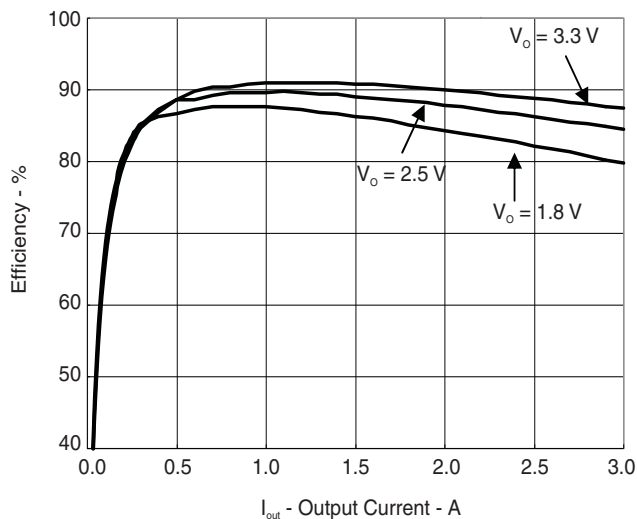


Figure 7. EFFICIENCY vs. OUTPUT CURRENT ($V_{IN} = 12\text{ V}$)

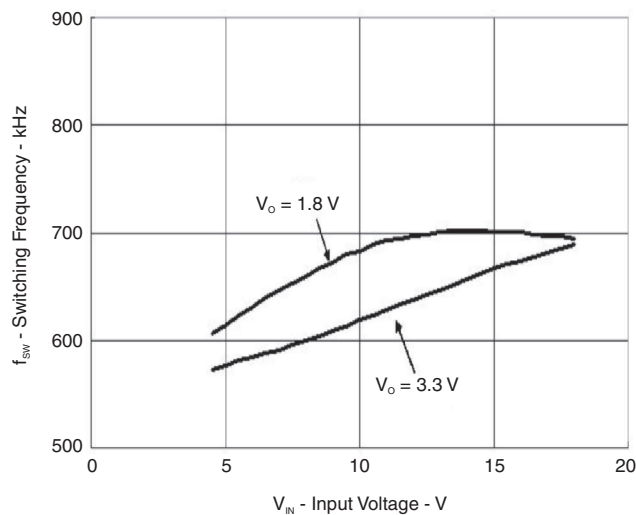


Figure 8. SWITCHING FREQUENCY vs. INPUT VOLTAGE ($I_O = 1\text{ A}$)

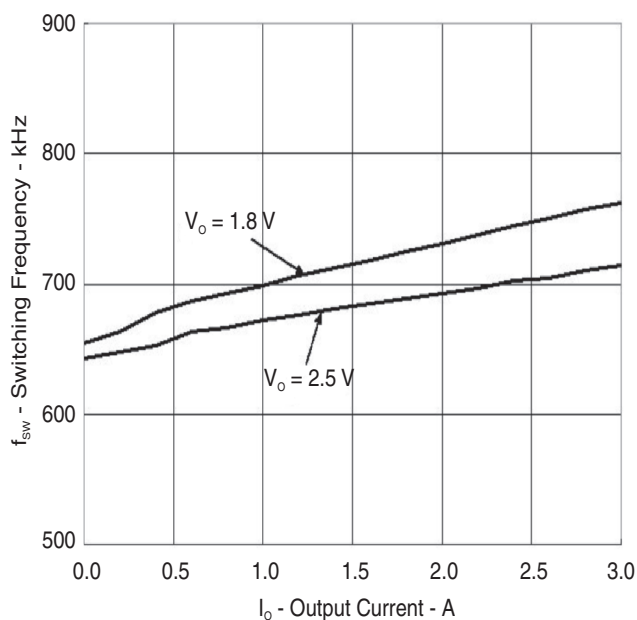


Figure 9. SWITCHING FREQUENCY vs. OUTPUT CURRENT

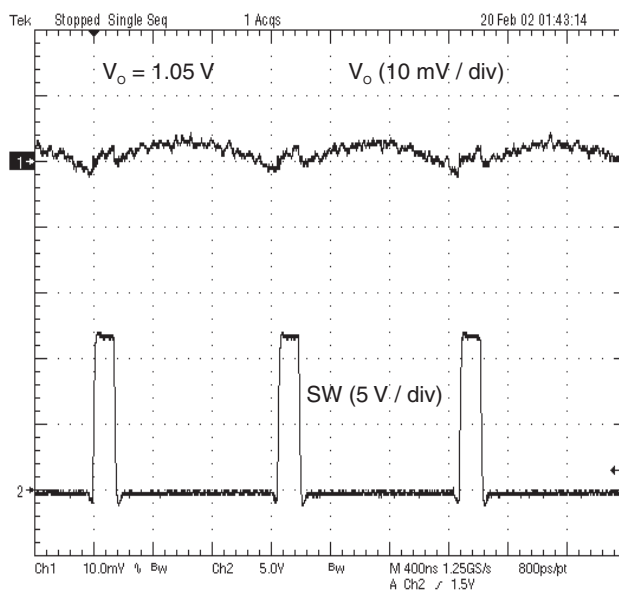


Figure 10. VOLTAGE RIPPLE AT OUTPUT

TYPICAL CHARACTERISTICS (continued)

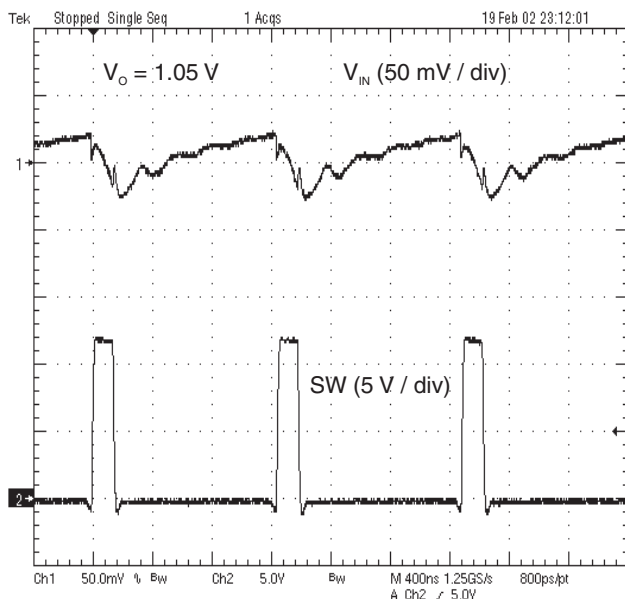


Figure 11. VOLTAGE RIPPLE AT INPUT

DESIGN GUIDE

Step By Step Design Procedure

To begin the design process, you must define these parameters for your application as follows:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

Output Inductor Selection

The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improves S/N ratio and contributes to stable operation. Smaller ripple currents result in lower output voltage ripple. When using low ESR output capacitors output ripple voltage is usually low, so larger ripple currents are acceptable. The coefficient K_{ind} represents the percentage of ripple current. The value of K_{ind} must not be greater than 0.4. Use 0.3 when using low ESR output capacitors. Equation 2 can be used to calculate L_1 . Use 700 kHz for f_{SW} . Make sure the chosen inductor is rated for the peak current of Equation 4 and the RMS current of Equation 5.

$$L_O = \frac{V_{OUT}}{V_{IN(max)}} \cdot \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \cdot f_{SW} \cdot K_{ind}} \quad (2)$$

$$\Delta p - p = \frac{V_{OUT}}{V_{IN(max)}} \cdot \frac{V_{IN(max)} - V_{OUT}}{L_O \cdot f_{SW}} \quad (3)$$

$$I_{lpeak} = I_O + \frac{\Delta p - p}{2} \quad (4)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} \Delta p - p^2} \quad (5)$$

Output Capacitor Selection

The capacitor value and ESR determines the amount of output voltage ripple. Recommended to use ceramic output capacitor. Using Equation 6 to Equation 8, an initial estimate for the capacitor value, ESR, and RMS current can be calculated. If the load transients are significant consider using the load step, instead of ripple current to calculate the maximum ESR. Minimum C_O should be over 20 μ F.

$$C_O > \frac{1}{8 \cdot f_{SW}} \cdot \frac{1}{\left(\frac{V_{O(ripple)}}{I_{(ripple)}} - R_{ESR} \right)} \quad (6)$$

$$R_{ESR} < \frac{V_{O(ripple)}}{I_{(ripple)}} \quad (7)$$

$$I_{CO(RMS)} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_O \cdot f_{SW}} \quad (8)$$

Input Capacitor Selection

The TPS54325 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μ F is recommended for the decoupling capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage. In case of separate V_{CC} and V_{IN} , then a ceramic capacitor over 10 μ F is recommended for the V_{IN} and also placing ceramic capacitor over 0.1 μ F for the V_{CC} is recommended.

Bootstrap Capacitor Selection

A 0.1- μ F ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

VREG5 Capacitor Selection

A 1- μ F ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using [Equation 9](#) and [Equation 10](#) to calculate V_{OUT} .

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

For output voltage from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \cdot \left(1 + \frac{R1}{R2}\right) \quad (9)$$

For output voltage over 2.5 V:

$$V_{OUT} = (0.763 + 0.0017 \cdot V_{OUT}) \cdot \left(1 + \frac{R1}{R2}\right) \quad (10)$$

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be connected to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. [SLMA002](#) and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. [SLMA004](#).

The exposed thermal pad dimensions for this package are shown in the following illustration.

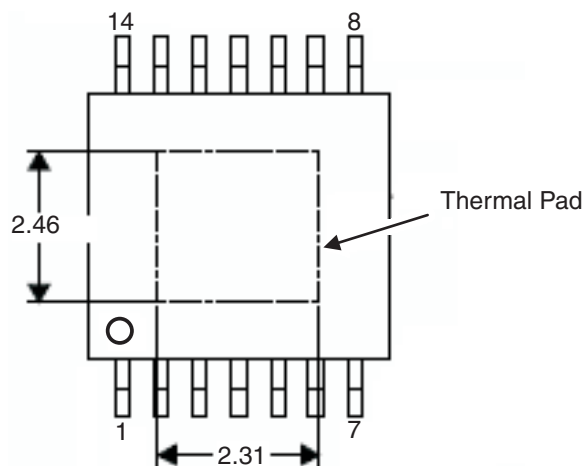


Figure 12. Thermal Pad Dimensions

LAYOUT CONSIDERATIONS

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. If VIN and VCC is shorted, VIN and VCC patterns need to be connected with broad pattern lines.
15. VIN Capacitor should be placed as near as possible to the device.

Revision History

The ambient temperature, T_A , for the current limit, I_{oc1} , was changed from 25°C to –40°C to 85°C and 3.5 A was added at min range.

$V_{IN} = 12$ V was specified for Figure 7. Efficiency vs. Output Current.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS54325PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS54325PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54325PWPR	HTSSOP	PWP	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



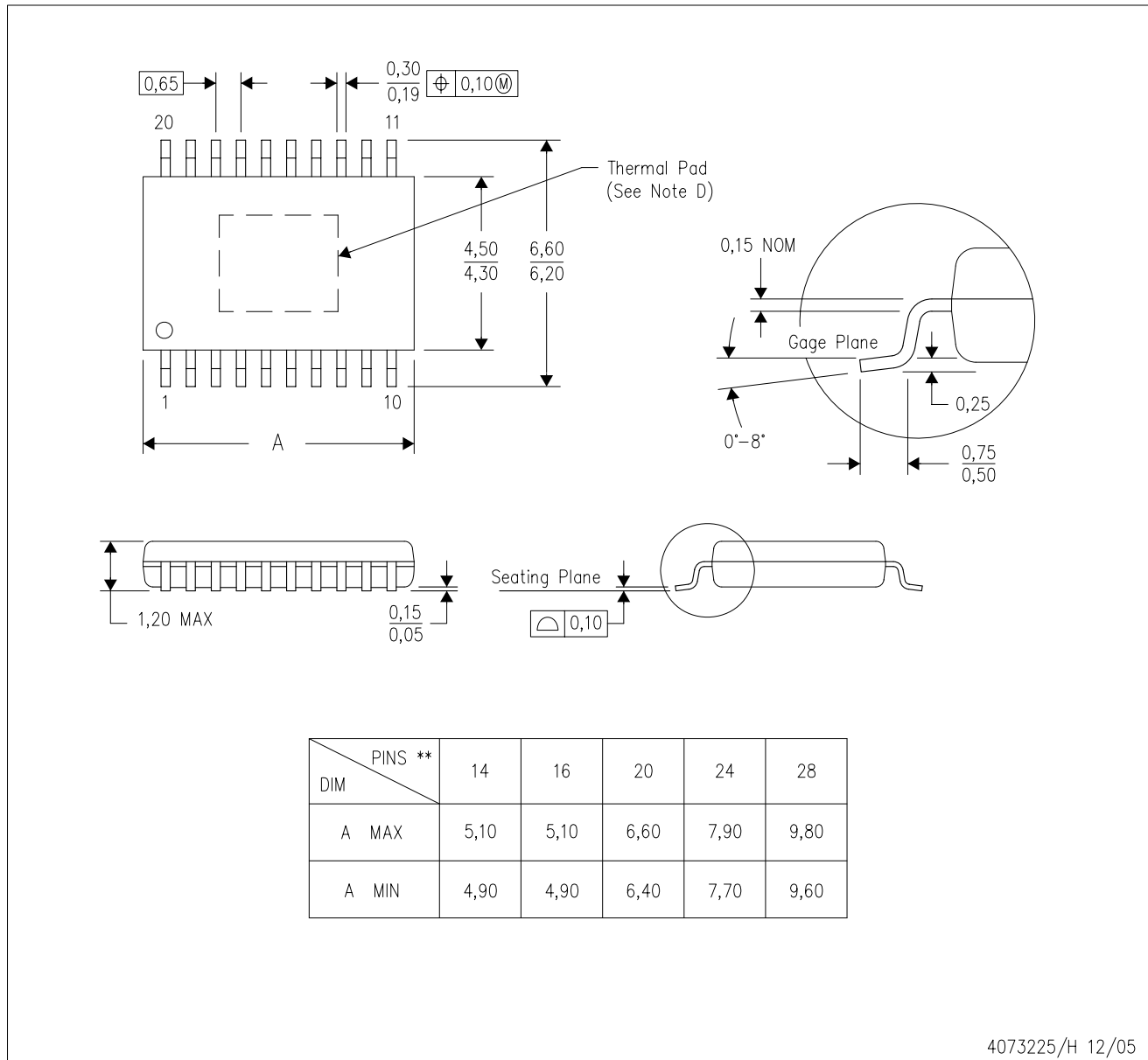
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54325PWPR	HTSSOP	PWP	14	2000	346.0	346.0	29.0

MECHANICAL DATA

PWP (R-PDSO-G**) 20 PIN SHOWN

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



4073225/H 12/05

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MO-153

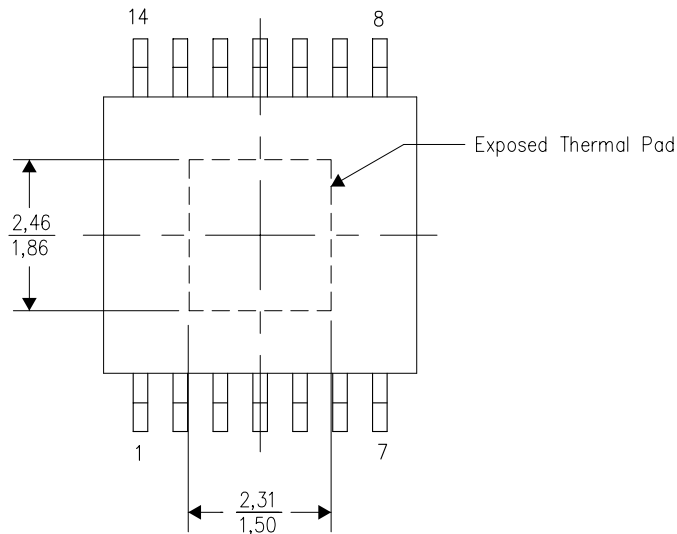
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

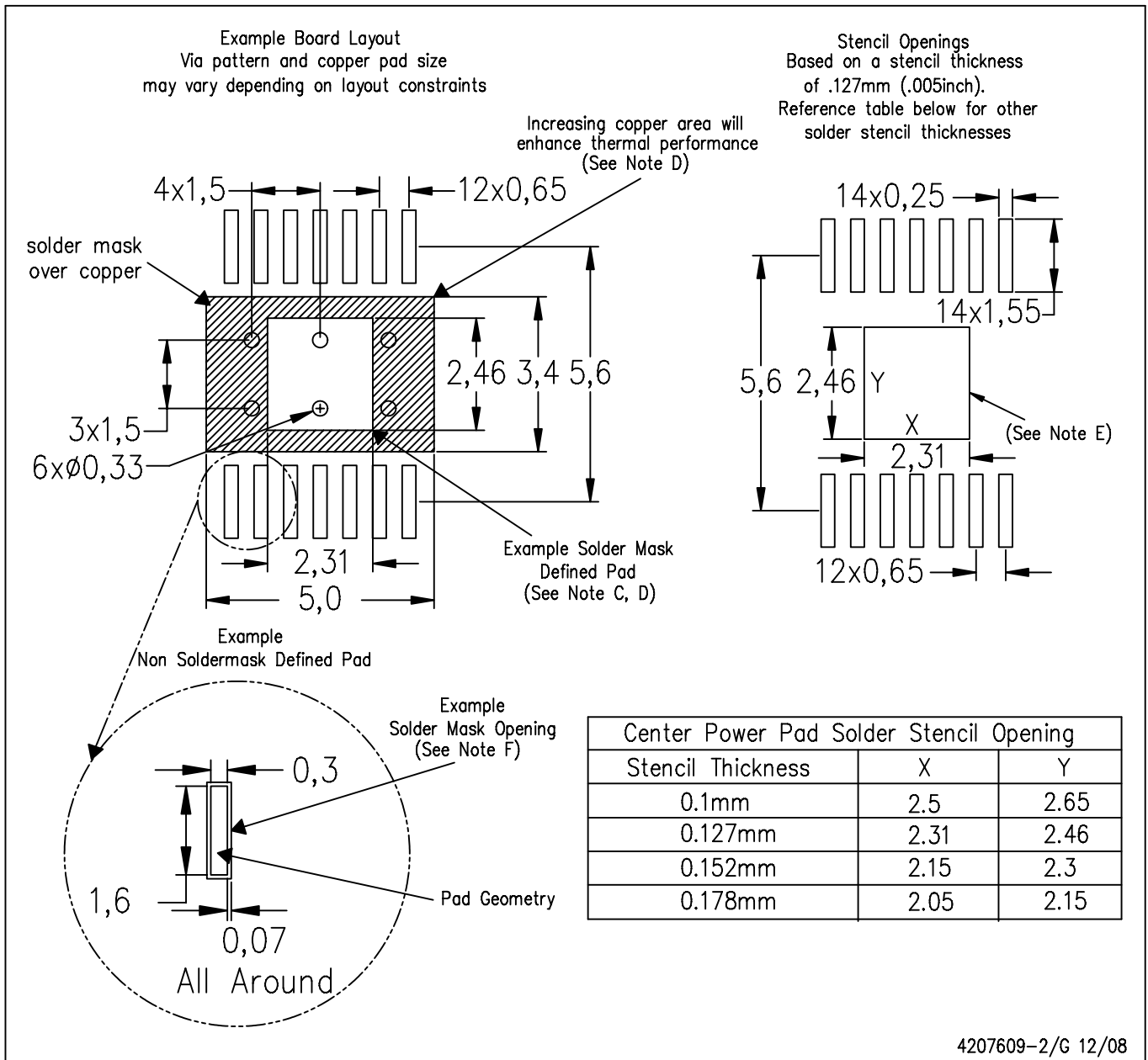


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R-PDSO-G14) PowerPAD™



4207609-2/G 12/08

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated