FEATURES

- **Two-Channel Bidirectional Buffers**
- **I^{2}C Bus and SMBus Compatible**
- **Active-High Repeater-Enable Input**
- **Open-Drain I^{2}C I/O**
- **5.5-V Tolerant I^{2}C I/O and Enable Input Support Mixed-Mode Signal Operation**
- **Lockup-Free Operation**
- **Accommodates Standard Mode and Fast Mode I^{2}C Devices and Multiple Masters**
- **Supports Arbitration and Clock Stretching Across the Repeater**
- **Powered-Off High-Impedance I^{2}C Pins**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

D, DCT, DGK, OR PW PACKAGE
(TOP VIEW)

```
        ┌──┬──┐
  NC  [ 1    8 ] V_CC
 SCL0 [ 2    7 ] SCL1
 SDA0 [ 3    6 ] SDA1
  GND [ 4    5 ] EN
        └─────┘
```
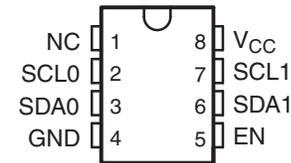
NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

This dual bidirectional I^{2}C buffer is operational at 2.3-V to 3.6-V V$_{CC}$.

The PCA9515A is a BiCMOS integrated circuit intended for I^{2}C bus and SMBus systems applications. The device contains two identical bidirectional open-drain buffer circuits that enable I^{2}C and similar bus systems to be extended without degradation of system performance. Both buffers specifically are designed to support the standard low-level-contention arbitration of the I^{2}C bus and support clock stretching.

The PCA9515A buffers both the serial data (SDA) and serial clock (SCL) signals on the I^{2}C bus, while retaining all the operating modes and features of the I^{2}C system. This enables two buses of 400-pF bus capacitance to be connected in an I^{2}C application.

The I^{2}C bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9515A enables the system designer to isolate two halves of a bus, accommodating more I^{2}C devices or longer trace lengths.

ORDERING INFORMATION

T$_A$	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[2]
−40°C to 85°C	SOIC – D	Tube of 75	PCA9515AD	PD515A
		Reel of 2500	PCA9515ADR	
		Reel of 250	PCA9515ADT	
	SSOP – DCT	Reel of 3000	PCA9515ADCTR	PREVIEW
		Reel of 250	PCA9515ADCTT	
	TSSOP – PW	Tube of 150	PCA9515APW	PD515A
		Reel of 2000	PCA9515APWR	
		Reel of 250	PCA9515APWT	
	VSSOP – DGK	Reel of 2500	PCA9515ADGKR	7B_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
    DGK: The actual top-side marking has one additional character that designates the assembly/test site.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The PCA9515A has an active-high enable (EN) input with an internal pullup, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It never should change state during an I²C operation, because disabling during a bus operation hangs the bus, and enabling part way through a bus cycle could confuse the I²C parts being enabled. The EN input should change state only when the global bus and the repeater port are in an idle state, to prevent system failures.

The PCA9515A also can be used to run two buses: one at 5-V interface levels and the other at 3.3-V interface levels, or one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated when the 400-kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz, because of the delays that are added by the repeater.

The output low levels for each internal buffer are approximately 0.5 V, but the input voltage of each internal buffer must be 70 mV or more below the output low level, when the output internally is driven low. This prevents a lockup condition from occurring when the input low condition is released.

Two or more PCA9515A devices cannot be used in series. The PCA9515A design does not allow this configuration. Because there is no direction pin, slightly different valid low-voltage levels are used to avoid lockup conditions between the input and the output of each repeater. A valid low applied at the input of a PCA9515A is propagated as a buffered low with a slightly higher value on the enabled outputs. When this buffered low is applied to another PCA9515A-type device in series, the second device does not recognize it as a valid low and does not propagate it as a buffered low again.

The device contains a power-up control circuit that sets an internal latch to prevent the output circuits from becoming active until V_{CC} is at a valid level (V_{CC} = 2.3 V).

As with the standard I²C system, pullup resistors are required to provide the logic high levels on the buffered bus. The PCA9515A has standard open-collector configuration of the I²C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with Standard Mode and Fast Mode I²C devices in addition to SMBus devices. Standard Mode I²C devices only specify 3 mA in a generic I²C system where Standard Mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.
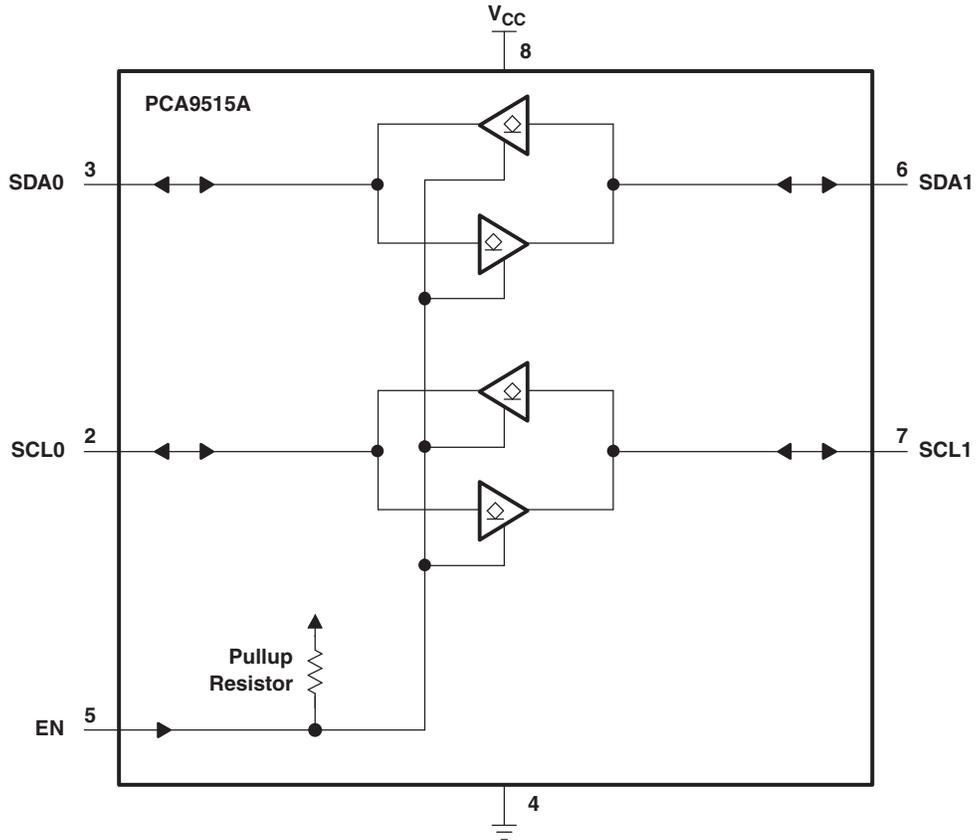
TERMINAL FUNCTIONS

NO.	NAME	DESCRIPTION
1	NC	No internal connection
2	SCL0	Serial clock bus 0
3	SDA0	Serial data bus 0
4	GND	Supply ground
5	EN	Active-high repeater enable input
6	SDA1	Serial data bus 1
7	SCL1	Serial clock bus 1
8	V_{CC}	Supply power

FUNCTION TABLE

INPUT EN	FUNCTION
L	Outputs disabled
H	SDA0 = SDA1, SCL0 = SCL1

LOGIC DIAGRAM (POSITIVE LOGIC)

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	7	V
V_I	Enable input voltage range[2]		−0.5	7	V
$V_{I/O}$	I²C bus voltage range[2]		−0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[3]	D package		97	°C/W
		DCT package		220	
		DGK package		172	
		PW package		149	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	SDA and SCL inputs	$0.7 \times V_{CC}$	5.5	V
		EN input	2	5.5	
V_{IL}[1]	Low-level input voltage	SDA and SCL inputs	−0.5	$0.3 \times V_{CC}$	V
		EN input	−0.5	0.8	
V_{ILc}[1]	SDA and SCL low-level input voltage contention		−0.5	0.4	V
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 3 V		6	
T_A	Operating free-air temperature		−40	85	°C

(1) V_{IL} specification is for the EN input and the first low level seen by the SDAx and SCLx lines. V_{ILc} is for the second and subsequent low levels seen by the SDAx and SCLx lines. V_{ILc} must be at least 70 mV below V_{OL}.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage		$I_I = -18$ mA	2.3 V to 3.6 V			−1.2	V
V_{OL}	Low-level output voltage	SDAx, SCLx	$I_{OL} = 20$ μA or 6 mA	2.3 V to 3.6 V	0.47	0.52	0.6	V
$V_{OL} - V_{ILc}$	Low-level input voltage below low-level output voltage	SDAx, SCLx	$I_I = 10$ μA	2.3 V to 3.6 V			70	mV
I_{CC}	Quiescent supply current		Both channels high, SDAx = SCLx = V_{CC}	2.7 V		0.5	3	mA
				3.6 V		0.5	3	
			Both channels low, SDA0 = SCL0 = GND and SDA1 = SCL1 = open; or SDA0 = SCL0 = open and SDA1 = SCL1 = GND	2.7 V		1	4	
				3.6 V		1	4	
			In contention, SDAx = SCLx = GND	2.7 V		1	4	
				3.6 V		1	4	
I_I	Input current	SDAx, SCLx	$V_I = 3.6$ V	2.3 V to 3.6 V			±1	μA
			$V_I = 0.2$ V				3	
		EN	$V_I = V_{CC}$				±1	
			$V_I = 0.2$ V			−10	−20	
I_{off}	Leakage current	SDAx, SCLx	$V_I = 3.6$ V	EN = L or H	0 V			0.5	μA
			$V_I = $ GND					0.5	
$I_{I(ramp)}$	Leakage current during power up	SDAx, SCLx	$V_I = 3.6$ V	EN = L or H	0 V to 2.3 V			1	μA
C_{in}	Input capacitance	EN	$V_I = 3$ V or GND		3.3 V		7	9	pF
		SDAx, SCLx		EN = H	3.3 V		7	9	

(1) All typical values are at nominal supply voltage (V_{CC} = 2.5 V or 3.3 V) and $T_A = 25°$C.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

|		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_{su}	Setup time, EN↑ before Start condition	100		100		ns
t_h	Hold time, EN↓ after Stop condition	130		100		ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V			V_{CC} = 3.3 V ± 0.3 V			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PZL}	Propagation delay time[2]	SDA0, SCL0 or SDA1, SCL1	SDA1, SCL1 or SDA0, SCL0	45	82	130	45	68	120	ns
t_{PLZ}				33	113	190	33	102	180	
t_{tHL}	Output transition time[2] (SDAx, SCLx)	80%	20%		57			58		ns
t_{tLH}		20%	80%		148			147		

(1) All typical values are at nominal supply voltage (V_{CC} = 2.5 V or 3.3 V) and $T_A = 25°$C.
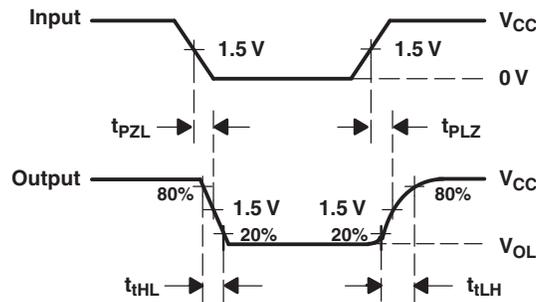(2) Different load resistance and capacitance alter the RC time constant, thereby changing the propagation delay and transition times.

PARAMETER MEASUREMENT INFORMATION
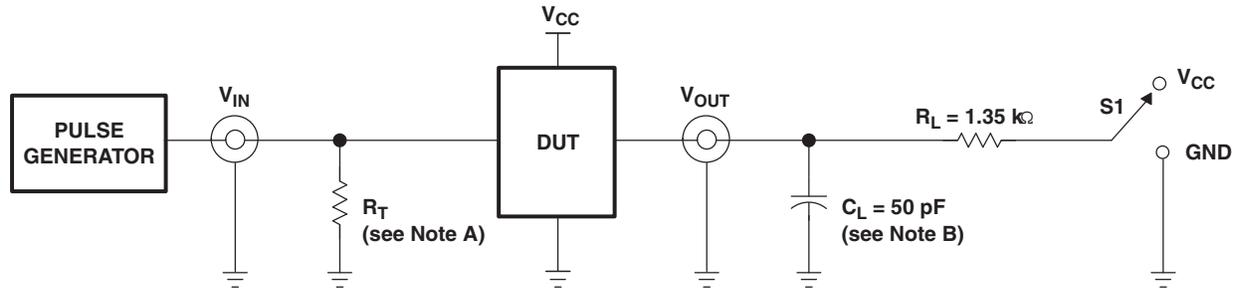
TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

A. R_T termination resistance should be equal to Z_{OUT} of pulse generators.

B. C_L includes probe and jig capacitance.

C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, slew rate $\geq$ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLH} and t_{PHL} are the same as t_{pd}.

F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

G. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 1. Test Circuit and Voltage Waveforms

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APPLICATION INFORMATION

A typical application is shown in Figure 2. In this example, the system master is running on a 3.3-V bus, while the slave is connected to a 5-V bus. Both buses run at 100 kHz, unless the slave bus is isolated, and then the master bus can run at 400 kHz. Master devices can be placed on either bus.
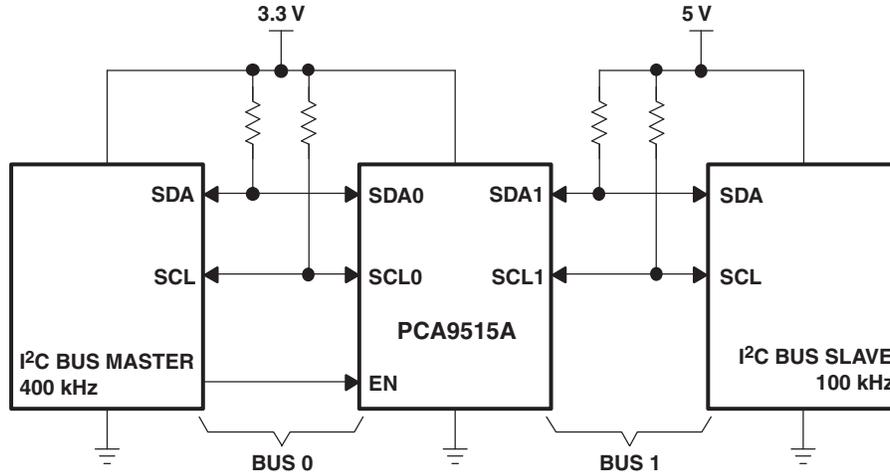

Figure 2. Typical Application

The PCA9515A is 5.5-V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

When one side of the PCA9515A is pulled low by a device on the I²C bus, a CMOS hysteresis-type input detects the falling edge and causes an internal driver on the other side to turn on, thus causing the other side also to go low. The side driven low by the PCA9515A typically is at $V_{OL} = 0.5$ V.

Figure 3 and Figure 4 show the waveforms that are seen in a typical application. If the bus master in Figure 2 writes to the slave through the PCA9515A, Bus 0 has the waveform shown in Figure 3. This looks like a normal I²C transmission until the falling edge of the eighth clock pulse. At that point, the master releases the data line (SDA) while the slave pulls it low through the PCA9515A. Because the V_{OL} of the PCA9515A typically is around 0.5 V, a step in the SDA is seen. After the master has transmitted the ninth clock pulse, the slave releases the data line.
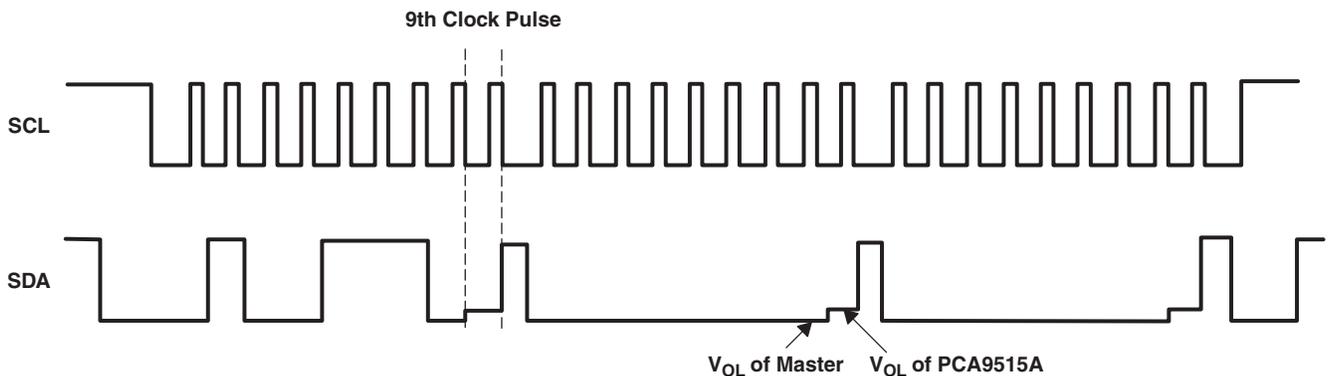

Figure 3. Bus 0 Waveforms
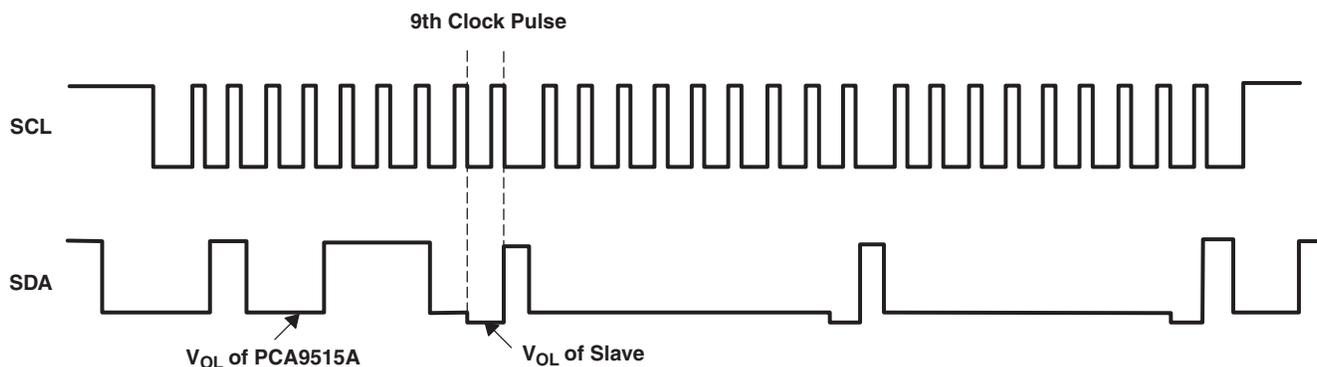
APPLICATION INFORMATION (continued)

Figure 4. Bus 1 Waveforms

On the Bus 1 side of the PCA9515A, the clock and data lines have a positive offset from ground equal to the V_{OL} of the PCA9515A. After the eighth clock pulse, the data line is pulled to the V_{OL} of the slave device, which is very close to ground in the example.

It is important to note that any arbitration or clock-stretching events on Bus 1 require that the V_{OL} of the devices on Bus 1 be 70 mV below the V_{OL} of the PCA9515A (see $V_{OL} - V_{ILc}$ in *Electrical Characteristics*) to be recognized by the PCA9515A and transmitted to Bus 0.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
PCA9515AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9515ADGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9515ADGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9515ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9515ADT	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9515APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9515APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9515APWT	ACTIVE	TSSOP	PW	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
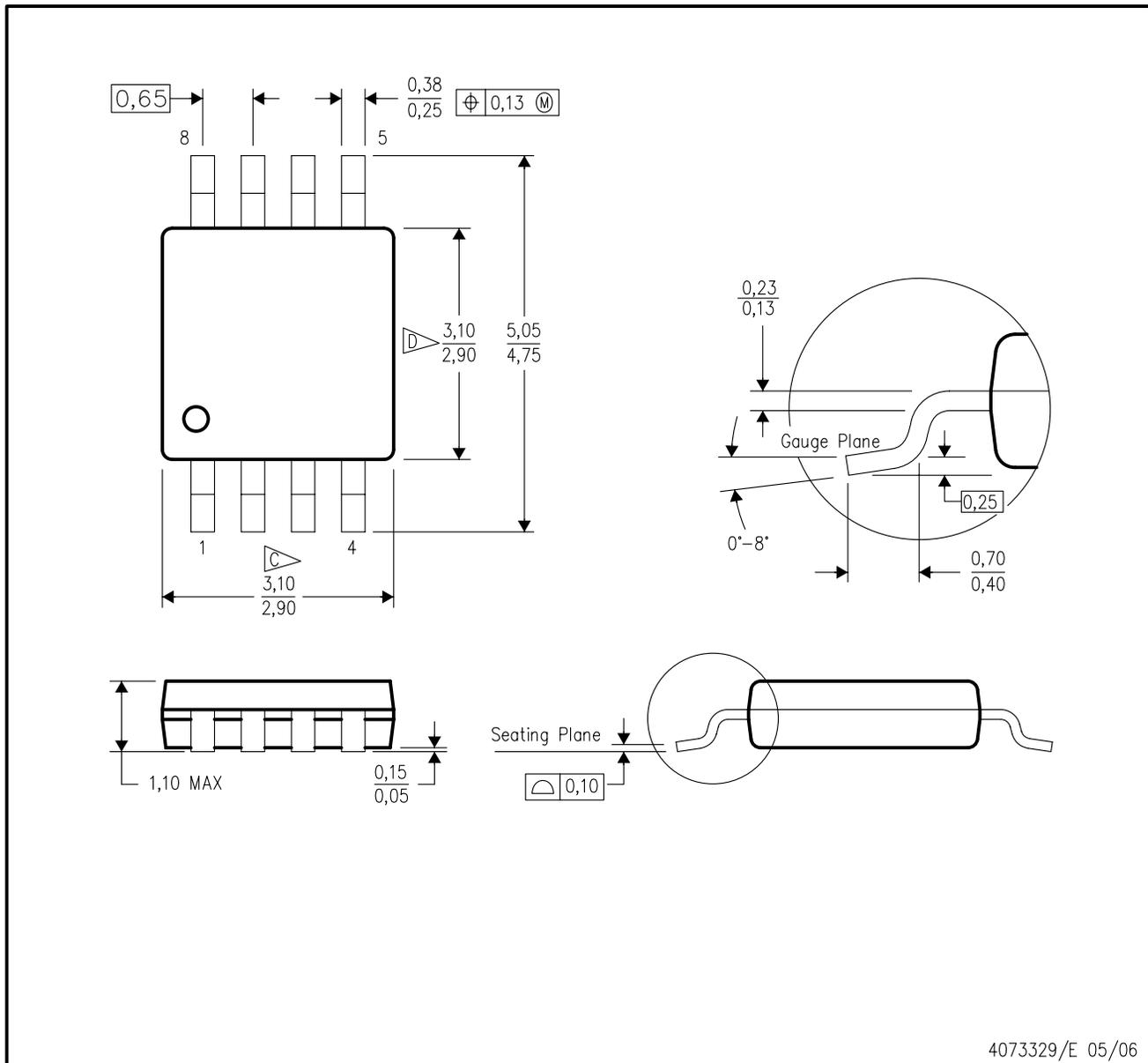
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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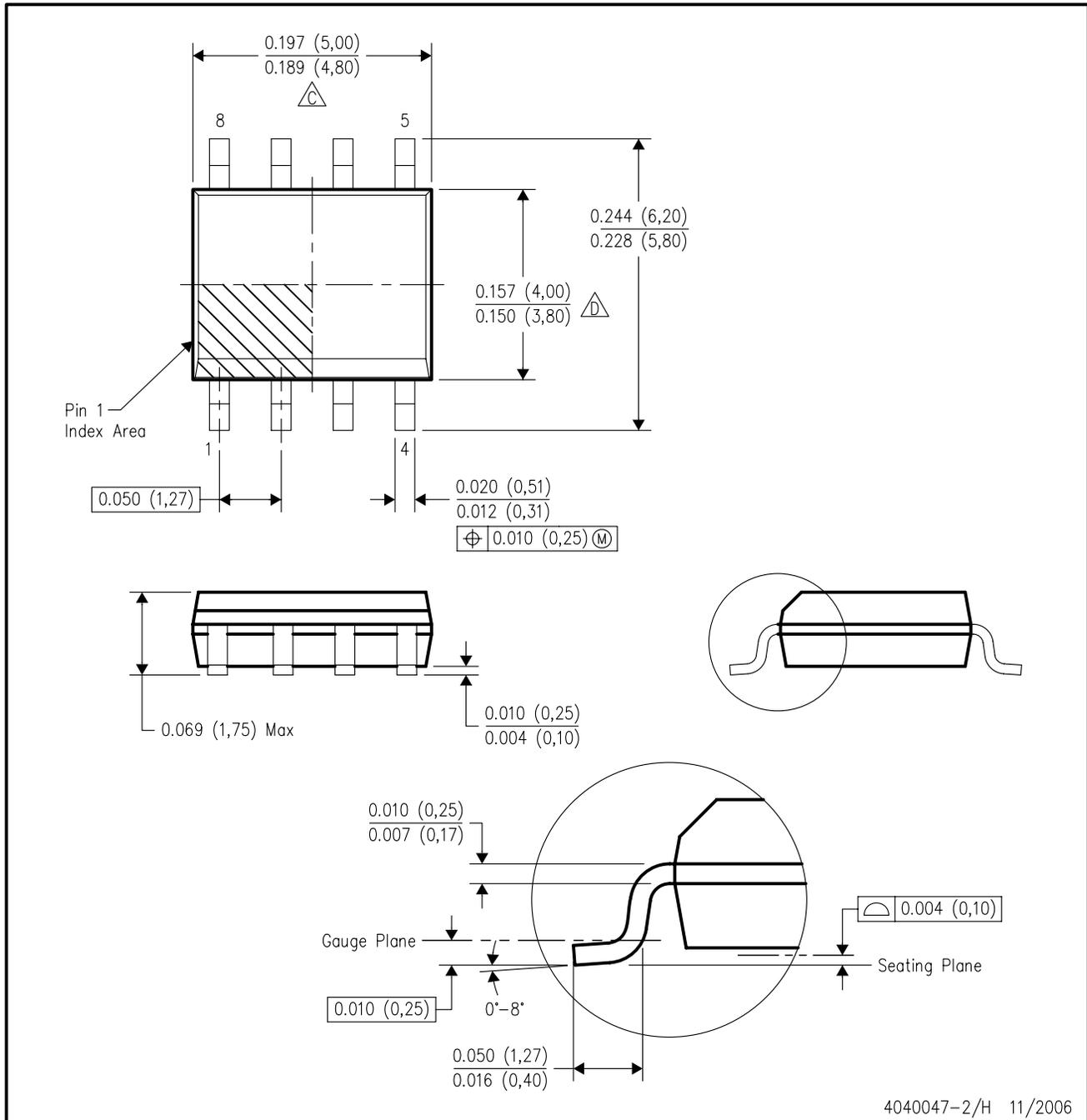
DGK (S−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE

0,65

8   5

0,38
0,25   ⊕ 0,13 Ⓜ

3,10
2,90

5,05
4,75

1   4
C
3,10
2,90

1,10 MAX

0,15
0,05

0,23
0,13

Gauge Plane

0°−8°

0,25

0,70
0,40

Seating Plane

0,10

4073329/E 05/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.15 per end.
         D   Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
         E.   Falls within JEDEC MO−187 variation AA, except interlead flash.

D (R−PDSO−G8)   **PLASTIC SMALL−OUTLINE PACKAGE**

0.197 (5,00)
0.189 (4,80)
C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
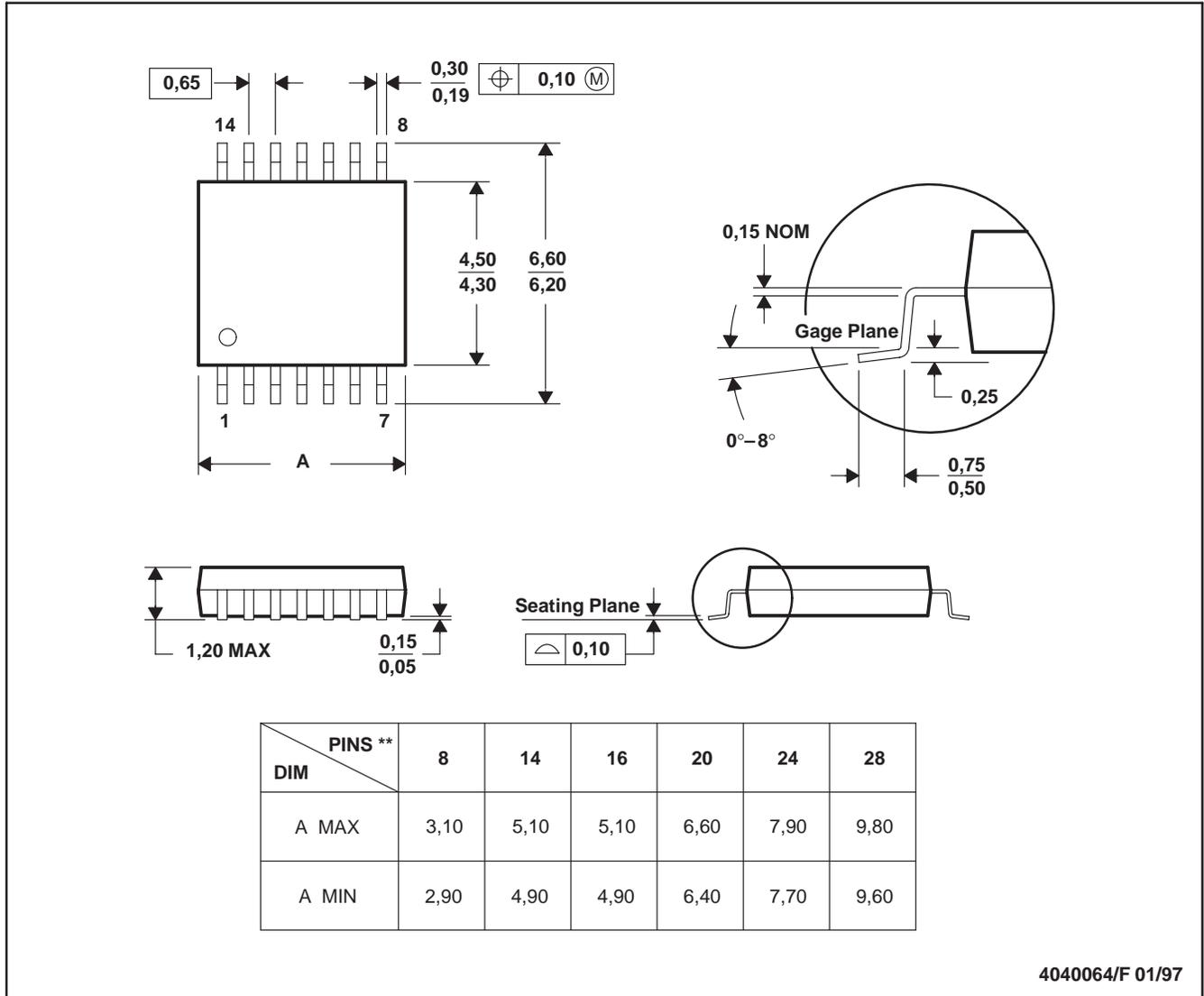0.016 (0,40)

4040047−2/H   11/2006

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
          D.   Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
          E.   Reference JEDEC MS−012 variation AA.

TEXAS INSTRUMENTS
www.ti.com

PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

0,65

$\dfrac{0,30}{0,19}$ ⊕ | 0,10 Ⓜ

14   8

$\dfrac{4,50}{4,30}$ $\dfrac{6,60}{6,20}$

1   7

A

0,15 NOM

Gage Plane

0,25

0°−8°

$\dfrac{0,75}{0,50}$

1,20 MAX $\dfrac{0,15}{0,05}$

Seating Plane

⌒ | 0,10

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  D. Falls within JEDEC MO-153

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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