Marvell Avastar 88W8797 Integrated 2x2 WLAN/Bluetooth/FM Single-Chip SoC

Supports High Throughput Data Rates for Next Generation WLAN Products

PRODUCT OVERVIEW

The Marvell® Avastar™ 88W8797 is a highly integrated 2x2 wireless local area network (WLAN) System-on-Chip (SoC), specifically designed to support high throughput data rates for next generation products and is part of the Marvell Avastar family of wireless devices. The SoC is designed for both simultaneous and independent operation of the following:

- 2x2 MIMO spatial streams supporting data rates up to MCS15 (300 Mbps)
- IEEE 802.11n/a/g/b payload data rates for Wireless Local Area Network (WLAN)
- Bluetooth 4.0 + HS (supports Low Energy (LE))
- FM transmit and receive (digital encoder/decoder FM radio with RDS/RBDS)

The device supports the 802.11i security standard through implementation of the Advanced Encryption Standard (AES)/ Counter Mode CBC-MAC Protocol (CCMP), Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP), Advanced Encryption Standard (AES)/Cipher-Based Message Authentication Code (CMAC), and WLAN Authentication and Privacy Infrastructure (WAPI) security mechanisms. The device also supports 802.11n Beamformer and Beamformee functions.

For video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported. The device also supports 802.11h Dynamic Frequency Selection (DFS) for detecting radar pulses when operating in the 5 GHz range.

The 88W8797 supports generic interfaces including SDIO 3.0, High-Speed Inter-Chip (HSIC), USB 2.0, high-speed UART, and PCM for connecting WLAN, Bluetooth, and FM to the host processor. For FM Tx/Rx, the device supports Inter-IC Sound (I2S) / analog stereo audio interfaces. An I2C-compatible interface is available to connect FM Tx/Rx to the host processor, as well. FM Tx/Rx can also share the host interface with Bluetooth.

The device is also equipped with a coexistence interface for external, co-located 2.4 GHz radios.

Available packaging includes a TFBGA option.

BLOCK DIAGRAM

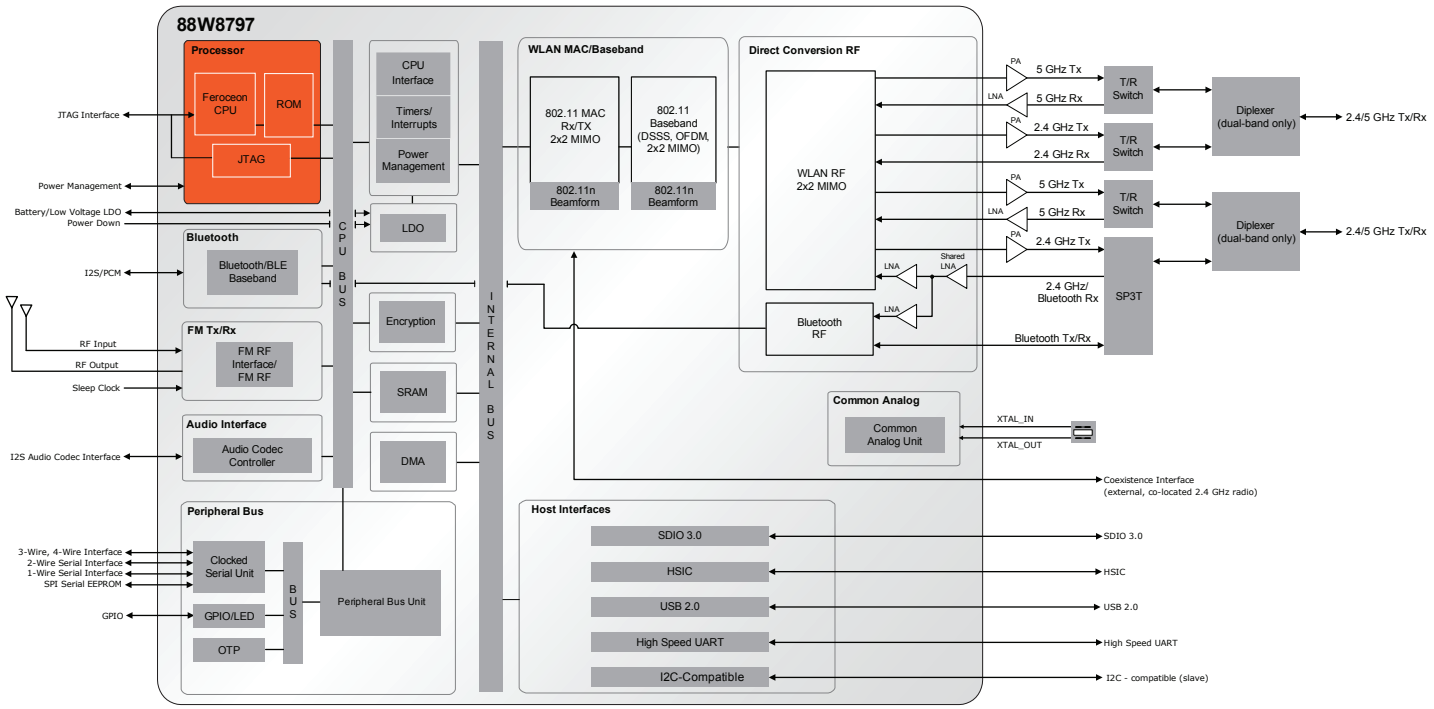

Fig 1. Avastar 88W8797 SoC Block Diagram

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SPECIFICATIONS

APPLICATIONS
- WLAN/Bluetooth/FM enabled cellular handsets
- Portable audio/video devices and accessories
- Personal computing systems including pads, tablets, and slates
- Wireless home audio and video entertainment systems including TV, set-top boxes, media servers, and gaming platforms

GENERAL FEATURES
- 2x2 MIMO operation
- Simultaneous and independent WLAN, Bluetooth (supports LE), and FM Tx/Rx operation
- Coexistence with cellular and other on-chip radios
- Low power dissipation
- CMOS and low-swing sine wave input clock
- Digital audio interfaces (I2S and PCM)
- 19.2, 26, 38.4, and 40 MHz crystal clock support with auto-frequency detection using external 32.768 kHz CMOS-level sleep clock
- Power management with external sleep clock support for FM Tx/Rx operation
- Sleep and standby modes for low power operation
- One time programmable (OTP) memory to eliminate need for external EEPROM
- Fully compatible with Marvell Power Management device(s)

IEEE 802.11/STANDARDS
- 802.11 data rates of 1 and 2 Mbps
- 802.11b data rates of 5.5 and 11 Mbps
- 802.11a/g data rates 6, 9, 12, 18, 24, 36, 48, and 54 Mbps for multimedia content transmission
- 802.11g/b performance enhancements
- 802.11n compliant, with maximum data rates up to 145 Mbps (20 MHz channel) and 300 Mbps (40 MHz channel)
- 802.11d international roaming
- 802.11e QoS block acknowledgement (with support for 802.11n extension)
- 802.11h transmit power control
- 802.11h DFS radar pulse detection
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11r fast hand-off for AP roaming
- 802.11v TIM frame transmission
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode

PACKAGING
- TFBGA

PROCESSOR
- CPU
  - Integrated Marvell Feroceon® CPU (ARMv5TE-compliant)
  - 256 MHz maximum CPU clock speed
- DMA
  - Independent 4-Channel Direct Memory Access (DMA)

MEMORY
- Internal SRAM for Tx frame queues/Rx data buffers
- Boot ROM
- ROM patching capability

WLAN MAC
- Ad-Hoc and Infrastructure Modes
- RTS/CTS for operation under DCF
- Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses
- On-chip Tx and Rx FIFO for maximum throughput
- Open System and Shared Key Authentication services
- MPDU Rx (de-aggregation) and Tx (aggregation)
- 20/40 MHz coexistence
- Reduced Inter-Frame Spacing (RIFS) bursting
- Management information base counters
- Radio resource measurement counters
- Block acknowledgement with 802.11n extension
- Dynamic frequency selection (DFS)
- Beamforming
  - 802.11n Explicit Beamformer, supports NDP and Stagger sounding
  - 802.11n Explicit Beamformee, supports immediate feedback generation using uncompress and compress steering matrix or delayed feedback of all feedback types
- TIM frame transmission
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Marvell mobile hotspot

WLAN BASEBAND
- 802.11n 2x2 MIMO (on-chip Marvell MIMO RF radio)
- Backward compatibility with legacy 802.11a/g/b technology
- WLAN/Bluetooth LNA sharing
- PHY data rates up to 300 Mbps
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz packets in 40 MHz channel, and 20 MHz duplicate legacy packets in 40 MHz channel mode operation
- Modulation and Coding Scheme (MCS)—0~15 and 32 (duplicate 6 Mbps)
- Enhanced radar detection for long and short pulse radar
- Enhanced AGC scheme for DFS channel
- Japan DFS requirements for W53 and W56
- Radio resource measurement
- Optional 802.11n MIMO features:
  - 20/40 MHz coexistence
  - Stream STBC reception
  - Short guard interval
  - RIFS on receive path
  - Explicit Beamformer and Beamformee support
  - Greenfield Tx/Rx
- Power save features

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SPECIFICATIONS

WLAN RADIO

- Integrated direct-conversion radio
- 20 and 40 MHz channel bandwidths
- WLAN Rx Path
  - Direct-conversion architecture eliminates need for external SAW filter
  - On-chip gain selectable LNAs with optimized noise figure and power consumption
  - High dynamic range AGC function in receive mode
- WLAN Tx Path
  - External PA with power control
  - Closed/open loop power control (0.5 dB increments)
  - Optimized Tx gain distribution for linearity and noise performance
- WLAN Local Oscillator
  - Fractional-N for multiple reference clock support
  - Fine channel step

WLAN ENCRYPTION

- WEP 64- and 128-bit encryption with hardware TKIP processing (WPA)
- AES-CCMP hardware implementation as part of 802.11i security standard (WPA2)
- Enhanced AES engine performance
- AES-Cipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard
- WLAN Authentication and Privacy Infrastructure (WAPI)

BLUETOOTH

- Bluetooth 4.0 + HS
- Bluetooth Class 2
- Bluetooth Class 1
- Single-ended, shared Tx/Rx path for Bluetooth
- Shared LNA for WLAN/Bluetooth
- Digital audio interfaces including PCM interface for voice applications and I2S for digital stereo applications
- Baseband and radio BDR and EDR packet types—1 Mbps (GFSK), 2 Mbps (/4-DQPSK), and 3 Mbps (8DPSK)
- Fully functional Bluetooth baseband—AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening
- Adaptive Frequency Hopping (AFH) including Packet Loss Rate (PLR) and RSSI
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full master and slave piconet support
- Scatternet support
- Standard UART and SDIO HCI transport layer
- HCI layer verified to function with major profile stack vendors
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- All standard pairing, authentication, link key, and encryption operations
- Standard Bluetooth power saving mechanisms (i.e., hold, sniff modes and sniff-subrating)
- Enhanced low power scan mode
- Dynamic Transmit Power Control (TPC)
- Channel Quality Driven (CQD) data rate
- SBC off load for A2DP streaming
- Wideband Speech Support
- Supports Advertiser, Scanner, Initiator, Master, and Slave roles and connects up to 64 links
- Supports WLAN/Bluetooth Coexistence (BCA) protocols
- Shared RF with BDR/EDR
- Supports encryption (AES)
- Hardware support for intelligent Adaptive Frequency Hopping (AFH)
- BDR/EDR, LE, and WLAN coexistence

FM RADIO

- Worldwide FM band—76–108 MHz
- Full Tx/Rx operation with main clock as well as 32.768 kHz external sleep clock
- Channel spacing/frequency step size (50 kHz steps)
- Stereo analog and digital input/output for Tx/Rx
- FM Rx Path
  - FM/RDS/RBDS receiver
  - Automatic frequency control (AFC)
  - Auto search tuning
  - Softmute
  - Audio mute
  - Mono/stereo blending (signal dependent)
  - Digital FM demodulation
  - RDS data buffer
  - FM audio routed internally as SCO source
  - Programmable pre/de-emphasis (50/75 µs)
  - TMC (traffic alert) supported
  - Enable/disable stereo mode
  - FM audio option to turn off CPU if no RDS
  - Audio silence detection
  - Alternate frequency
- FM Tx Path
  - FM/RDS/RBDS transmitter
  - RDS data buffer
  - High Tx output power (+125 dBµVrms) for loop antenna
  - Auto scan for channel selection
  - Auto channel sync through RDS
  - Audio mute
  - Audio Automatic Gain Control (AGC)
  - Compensation for 32 kHz clock error

COEXISTENCE

- Coexistence interface for external, co-located 2.4 GHz radio
  - Marvell 3/4-wire interface
  - WL_ACTIVE 3/4-wire interface
  - WL_ACTIVE 2-wire interface

HOST INTERFACES

- SDIO 3.0 device interface (SPI, 1-bit SDIO, 4-bit SDIO transfer modes at full clock range up to 100 MHz)[1]
- High-Speed Inter-Chip (HSIC) with Link Power Management (LPM) support
- USB 2.0 interface with LPM support
- High speed UART interface
- Optional I2C-compatible slave interface for FM control

[1] SDIO may be used as host interface for WLAN, Bluetooth, and FM.

PERIPHERAL BUS INTERFACES

- Clocked Serial Unit (CSU)
- 3-Wire, 4-Wire Serial Interface
- 2-Wire Serial Interface
- Wire Serial Interface
- SPI Serial EEPROM
- General Purpose Input Output (GPIO)
- One-Time Programmable (OTP) memory to eliminate need for external EEPROM

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MOVING FORWARD FASTER®

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AUDIO INTERFACES

- Audio Codec Interface
  - Marvell Class D Audio Amplifier
  - TWSI interface for Audio Codec programming
  - I2S (Inter-IC Sound) interface for audio data connection to Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC)
  - Master and slave mode for I2S, MSB, and LSB audio interfaces
  - Tri-state I2S interface capability
- PCM Interface
  - Master or slave mode
  - PCM bit width size of 8 bits or 16 bits
  - Up to 4 slots with configurable bit width and start positions
  - Short frame and long frame synchronization
  - Tri-state PCM interface capability

TEST

- On-chip diagnostic information

THE MARVELL ADVANTAGE: Marvell chipsets come with complete reference designs which include board layout designs, software, manufacturing diagnostic tools, documentation, and other items to assist customers with product evaluation and production. Marvell's worldwide field application engineers collaborate closely with end customers to develop and deliver new leading-edge products for quick time-to-market. Marvell utilizes world-leading semiconductor foundry and packaging services to reliably deliver high-volume and low-cost total solutions.

ABOUT MARVELL: Marvell is a leader in storage, communications, and consumer silicon solutions. Marvell's diverse product portfolio includes switching, transceiver, communications controller, processor, wireless, power management, and storage solutions that power the entire communications infrastructure, including enterprise, metro, home, storage, and digital entertainment solutions. For more information, visit our Web site at www.marvell.com.

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