8-CHANNEL HIGH_QUALITY LOW-POWER AUDIO CODEC FOR PORTABLE APPLICATIONS

Check for Samples: TWL6040

FEATURES

- Four audio digital-to-analog (DAC) channels
- Stereo capless headphone drivers:
  - Up to 104-dB DR
  - Power tune for performance/power consumption tradeoff
- Stereo 8 Ω, 1.5 W per channel speaker drivers
- Differential earpiece driver
- Stereo line-out
- Two audio analog-to-digital (ADC) channels:
  - 96-dBA SNR
- Four audio inputs:
  - Three differential microphone inputs
  - Stereo line-in/FM input
- Two vibrator/haptics feedback channels:
  - Differential H-bridge drivers
- Two low-noise analog microphone bias outputs
- Two digital microphone bias outputs
- Analog low-power loop from line-in to headphone/speaker outputs
- Dual phase-locked loops (PLLs) for flexible clock support:
  - 32-kHz sleep clock input for system low-power playback mode
  - 12-/19.2-/26-/38.4-MHz system clock input
- Accessory plug/unplug detection, accessory button press detection
- Integrated power supplies:
  - Negative charge pump for capless headphone driver
  - Two low dropout voltage regulators (LDOs) for high power supply rejection ratio (PSRR)
- I^2C control
- Thermal protection:
  - Host interrupt
- Power supplies:
  - Analog: 2.1 V
  - Digital I/O: 1.8 V
  - Battery 2.3 to 5.5 V
- Package 6-mm × 6-mm 120-pin PBGA

APPLICATIONS

- Mobile and smart phones
- MP3 players
- Handheld devices

DESCRIPTION

The TWL6040 device is an audio coder/decoder (codec) with a high level of integration providing analog audio codec functions for portable applications, as shown in Figure 1. It contains multiple audio analog inputs and outputs, as well as microphone biases and accessory detection. It is connected to the OMAP4™ host processor through a proprietary PDM interface for audio data communication enabling partitioning with optimized power consumption and performance. Multichannel audio data is multiplexed to a single wire for downlink (PDML) and uplink (PDMUL).

The OMAP4 device provides the TWL6040 device with five PDM audio-input channels (DL0–DL4). Channels DL0–DL3 are connected to four parallel DAC channels multiplexed to stereo headphone (HSL, HSR), stereo speaker (HFL, HFR), and earpiece (EAR) or stereo line outputs (AUXL, AUXR).

The stereo headphone path has a low-power (LP) mode operating from a 32-kHz sleep clock to enable more than 100 hours of MP3 playback time. Very-high dynamic range of 104 dBA is achieved when using the system clock input and DAC path high-performance (HP) mode. Class-AB headphone drivers provide a 1-V_{rms} output and are ground centered for capless connection to headphone, thus enabling system size and cost reduction. The earpiece driver is a differential class-AB driver with 2 V_{rms} capability to a typical 32-Ω load or 1.4 V_{rms} to a typical 16-Ω load.

Stereo speaker path has filterless class-D outputs with 1.5-W capability per channel. For output power maximization supply connection to an external boost is supported. Speaker drivers also support also hearing aid coil loads. For vibrator and haptic feedback support, the TWL6040 has two PWM channels with independent input signals from DL4 or inter-integrated circuit (I^2C™).

Vibrator drivers are differential H-bridge outputs, enabling fast acceleration and deceleration of vibrator motor. An external driver for a hearing aid coil or a piezo speaker requiring high voltage can be connected to line outputs.

The TWL6040 supports three differential microphone inputs (MMIC, HMIC, SMIC) and a stereo line-input (AFML, AFMR) multiplexed to two parallel ADCs. The PDM output from the ADCs is transmitted to the OMAP4 processor through UL0 and UL1. AFML, AFMR inputs can also be looped to analog outputs (LB0, LB1).

Two LDOs provide a voltage of 2.1 V to bias analog microphones (MBIAS and HBIAS). The maximum output current is 2 mA for each analog bias, allowing up to two microphones on one bias. Two LDOs provide a voltage of 1.8 V/1.85 V to bias digital microphones (DBIAS1 and DBIAS2). One bias generator can bias up several digital microphones at the same time, with a total maximum output current of 10 mA.

The TWL6040 has an integrated negative charge pump (NCP) and two LDOs (HS LDO and LS LDO) for high PSRR. The only external supply needed is 2.1 V, which is available from the 2.1-V DC-DC of the TWL6030 power management IC (PMIC) in the OMAP4 system. By powering audio from low-noise 2.1-V DC-DC of low power consumption, high dynamic range and high output swing at headset output are achieved. All other supply inputs can be directly connected to battery or system 1.8-V I/O.

Two integrated PLLs enable operatation from a 12/19.2/26/38.4-MHz system clock (MCLK) or, in LP playback mode, from a 32-kHz sleep clock (CLK32K). The frequency plan is based on a 48-kS/s audio data rate for all channels, and host processor uses sample-rate converters to interface with different sample rates (for example, 44.1 kHz). In the specific case of low-power audio playback, the 44.1-kS/s and 48-kS/s rates are supported by the TWL6040. Transitions between sample rates or input clocks are seamless.

Accessory plug and unplug detections are supported (PLUGDET). Some headsets have a manual switch for submitting send/end signal to the terminal through the microphone input pin. This feature is supported by a periodic accessory button press detection to minimize current consumption in sleep mode. Detection cycle properties can be programmed according to system requirements.

Figure 1 shows a simplified block diagram of the device.

Table 1. ORDERING INFORMATION

PART NUMBER	PACKAGE	ORDERING	MEDIUM
TWL6040	6-mm × 6-mm PBGA	TWL6040A2ZQZ/R	Reel

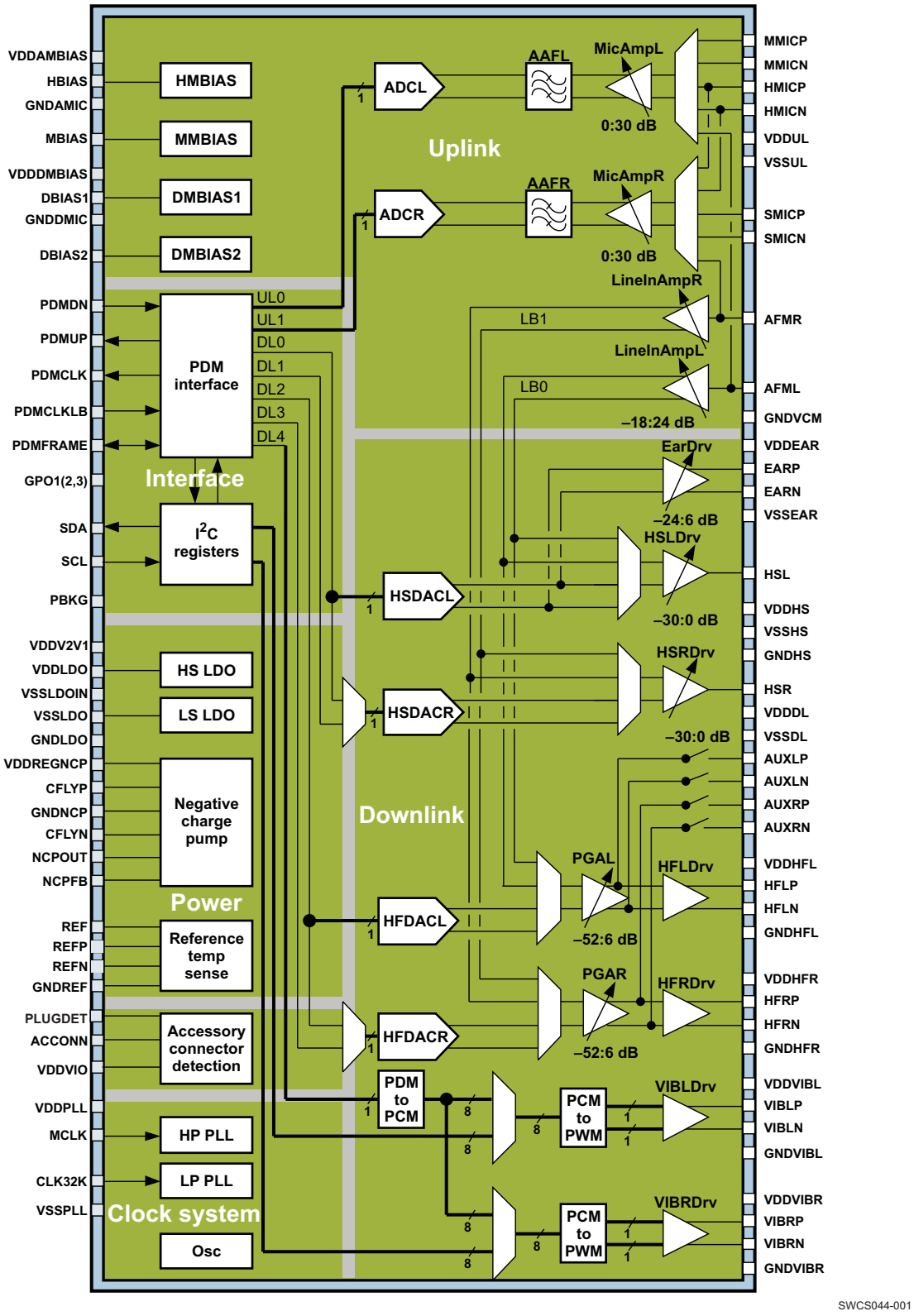


Figure 1. Simplified Block Diagram

Table 2. Terminal Functions

NAME	BALL	TYPE	I/O(1)	DESCRIPTION
MCLK	K7	Digital	I	System clock
CLK32K	H7	Digital	I	Real-time clock (RTC)
AUDPWRON	D8	Digital	I	Power-up signal
NRESPWRON	J9	Digital	I	Power-up reset
NAUDINT	E8	Digital	O	Interrupt
SDA	H6	Digital	I/O	I^2C serial interface data
SCL	G6	Digital	I	I^2C serial interface clock
PDMCLKLB	K8	Digital	I	PDM loopback clock
PDMCLK	L10	Digital	O	PDM reference clock
PDMFRAME	H8	Digital	I/O	PDM frame
PDMDN	K9	Digital	I	PDM downlink audio data
PDMUP	L8	Digital	O	PDM uplink audio data
Uplink Channel				
HBIAS	J3	Power	O	Headset microphone bias supply
MBIAS	K3	Power	O	Main analog microphone bias supply
DBIAS1	J5	Power	O	Digital microphone 1st bias supply
DBIAS2	L4	Power	O	Digital microphone 2nd bias supply
MMICP	K1	Analog	I	Main microphone (+)
MMICN	J2	Analog	I	Main microphone (–)
SMICP	J4	Analog	I	Submicrophone (+)
SMICN	H4	Analog	I	Submicrophone (–)
HMICP	H1	Analog	I	Headset microphone (+)
HMICN	H2	Analog	I	Headset microphone (–)
AFML	F1	Analog	I	Auxiliary or FM radio left input
AFMR	F2	Analog	I	Auxiliary or FM radio right input
Downlink Channel				
EARP	B10	Analog	O	Earphone output (+)
EARN	C11	Analog	O	Earphone output (–)
HSL	J11	Analog	O	Headset left output
HSR	K11	Analog	O	Headset right output
AUXLP	G3	Analog	O	Auxiliary predriver left output (+)
AUXLN	F3	Analog	O	Auxiliary predriver left output (–)
AUXRP	G4	Analog	O	Auxiliary predriver right output (+)
AUXRN	F4	Analog	O	Auxiliary predriver right output (–)
HFLP1	A4	Analog	O	Hands-free left output (+)
HFLP2	B4	Analog	O	Hands-free left output (+)
HFLN1	A5	Analog	O	Hands-free left output (–)
HFLN2	B5	Analog	O	Hands-free left output (–)
HFRP1	B9	Analog	O	Hands-free right output (+)
HFRP2	A9	Analog	O	Hands-free right output (+)
HFRN1	B8	Analog	O	Hands-free right output (–)
HFRN2	A8	Analog	O	Hands-free right output (–)
VIBLP	C1	Analog	O	Vibrator left output (+)
VIBLN	D3	Analog	O	Vibrator left output (–)
VIBRP	A2	Analog	O	Vibrator right output (+)
VIBRN	B1	Analog	O	Vibrator right output (–)

(1) I = Input; O = Output

Table 2. Terminal Functions (continued)

NAME	BALL	TYPE	I/O(1)	DESCRIPTION
Positive Supplies				
VDDVREF	H5	Power	I	Reference system supply
VDDLDO	D1	Power	O	High-side LDO output
VDDEAR	B11	Power	I	Earphone positive supply
VDDHS	J10	Power	I	Headset positive supply
VDDUL	G2	Power	I	Uplink codec positive supply
VDDDL	E9	Power	I	Downlink codec positive supply
VDDPLL	J7	Power	I	PLL positive supply
VDDHFL1	A3	Power	I	Hands-free left positive supply
VDDHFL2	A6	Power	I	Hands-free left positive supply
VDDHFR1	A7	Power	I	Hands-free right positive supply
VDDHFR2	A10	Power	I	Hands-free right positive supply
VDDVIBL	C2	Power	I	Vibrator positive supply
VDDVIBR	B2	Power	I	Vibrator positive supply
VDDAMBIAS	L2	Power	I	Analog microphone bias supply
VDDDMBIAS	K4	Power	I	Digital microphone bias supply
VDDREGNCP	H11	Power	I	Negative charge pump positive supply
VDDV2V1	E2	Power	I	Preregulated main positive supply
VDDVIO	L9	Power	I	Interface I/O supply
Negative Supplies				
CFLYN	F11	Power	O	Flying capacitor negative terminal
CFLYP	G11	Power	O	Flying capacitor positive terminal
NCPOUT1	E10	Power	O	Negative charge pump output
NCPOUT2	E11	Power	O	Negative charge pump output
NCPFB	G9	Power	I	Negative SMPS feedback
VSSLDOIN	D11	Power	I	Low-side LDO input supply
VSSLDO	D10	Power	O	Low-side LDO output
VSSEAR	C10	Power	I	Earphone negative supply
VSSHS	H10	Power	I	Headset negative supply
VSSUL	G1	Power	I	Uplink negative supply
VSSDL	F9	Power	I	Downlink negative supply
VSSPLL	L7	Power	I	PLL negative supply
Ground				
GN DREF	K5	Ground	I	Bandgap reference ground
GNDHS	H9	Ground	I	Headset sense input
GNDAMIC	H3	Ground	I	Analog microphone ground
GNDDMIC	L3	Ground	I	Digital microphone and accessory ground
GNDLDO1	E3	Ground	I	HS and LS LDO ground
GNDLDO2	D9	Ground	I	HS and LS LDO ground
GNDVCM	J1	Ground	I	Codec ground
GNDNCP1	F10	Ground	I	Negative charge pump ground
GNDNCP2	G10	Ground	I	Negative charge pump ground
GNDHFL1	C5	Ground	I	Hands-free left driver ground
GNDHFL2	C4	Ground	I	Hands-free left driver ground
GNDHFL3	C6	Ground	I	Hands-free left driver ground
GNDHFR1	C7	Ground	I	Hands-free right driver ground

Table 2. Terminal Functions (continued)

NAME	BALL	TYPE	I/O(1)	DESCRIPTION
GNDHFR2	C8	Ground	I	Hands-free right driver ground
GNDHFR3	C9	Ground	I	Hands-free right driver ground
GNDDIG	J6	Ground	I	Digital ground
GNDVIBR	B3	Ground	I	Vibrator driver ground
GNDVIBL	D2	Ground	I	Vibrator driver ground
GNDIO	J8	Ground	I	General-purpose I/O ground
PBKG1	F5	Ground	I	Substrate package ground
PBKG2	F6	Ground	I	Substrate package ground
PBKG3	F7	Ground	I	Substrate package ground
PBKG4	E4	Ground	I	Substrate package ground
PBKG5	K10	Ground	I	Substrate package ground
Miscallaneous				
REF	L5	Analog	I/O	Bandgap reference
REFP	K6	Analog	I/O	Positive converter reference
REFN	L6	Analog	I/O	Negative converter reference
ATEST	K2	Analog	O	Analog test pin
GPO1	D4	Digital	O	General-purpose output 1
GPO2	B6	Digital	O	General-purpose output 2
GPO3	B7	Digital	O	General-purpose output 3
DTEST1	A1	Digital	I	Digital test pin 1
DTEST2	L1	Digital	I	Digital test pin 2
DTEST3	A11	Digital	I	Digital test pin 3
PROG	L11	Digital	I	EEPROM programming pin
ACCONN	E1	Analog	I/O	Accessory connector pin
PLUGDET	G5	Analog	I	Accessory plug detection pin

	1	2	3	4	5	6	7	8	9	10	11
A	DTEST1	VIB RP	VDD HFL	HFLP	HFLN	VDD HFL	VDD HFR	HFRN	HFRP	VDD HFR	DTEST3
B	VIB RN	VDD VIBR	GND VIBR	HFLP	HFLN	GPO2	GPO3	HFRN	HFRP	EARP	VDD EAR
C	VIB LP	VDD VIBL		GND HFL	GND HFL	GND HFL	GND HFR	GND HFR	GND HFR	VSS EAR	EARN
D	VDD LDO	GND VIBL	VIB LN	GPO1				AUDP WRON	GND LDO2	VSS LDO	VSS LDOIN
E	ACC ONN	VDD V2V1	GND LDO1	PBKG				NAUD INT	VDD DL	NCP OUT	NCP OUT
F	AFML	AFMR	AUX LN	AUX RN	PBKG	PBKG	PBKG		VSS DL	GND NCP	CFLYN
G	VSS UL	VDD UL	AUX LP	AUX RP	PLUG DET	SCL			NCP FB	GND NCP	CFLYP
H	HMICP	HMICN	GND AMIC	SMICN	VDD VREF	SDA	CLK 32K	PDM FRAME	GND HS	VSS HS	VDD REG NCP
J	GND VCM	MMICN	HBIAS	SMICP	DBIAS1	GND DIG	VDD PLL	GND IO	NRES PWR ON	VDD HS	HSL
K	MMICP	ATEST	MBIAS	VDD DM BIAS	GND REF	REFP	MCLK	PDM CLKLB	PDM DN	PBKG	HSR
L	DTEST2	VDDA MBIAS	GND DMIC	DBIAS2	REF	REFN	VSS PLL	PDM UP	VDD VIO	PDM CLK	PROG

SWCS044-002

Figure 2. Pin Assignment (Top View)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

Stresses beyond those listed below may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated below are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	DC	–0.3		5.5	V
	AC, 1000 spikes of 10 ms	–0.3		6	V
	duration over 7 years				
Ambient operating temperature		–30		85	°C
Storage temperature		–55		150	°C
Electrostatic discharge protection (HBM)		2			kV
Electrostatic discharge protection (CDM)		500			V

THERMAL CHARACTERISTICS(1)

Over operating free-air temperature range (unless otherwise noted)

PACKAGE	POWER (W)	$R_{\Theta JA}$ (°C/W)	$R_{\Theta JB}$ (°C/W)	$R_{\Theta JC}$ (°C/W)	BOARD TYPE
PBGA, 6mm x 6mm	0.4	34	22	8	2S2P

(1) NOTE: The maximum power, 0.4 W, is at 85°C ambient temperature.
(a) $R_{\theta JA}$ (Theta-JA) = Thermal Resistance Junction-to-Ambient, °C/W
(b) $R_{\theta JB}$ (Theta-JB) = Thermal Resistance Junction-to-Board, °C/W
(c) $R_{\theta JC}$ (Theta-JC) = Thermal Resistance Junction-to-Case, °C/W

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage				V
VBAT	2.3	3.7	5.5	
V2V1	2.039	2.127	2.205	
VIO	1.747	1.823	1.89	
Operating junction temperature range	–30		125	°C
Operating ambient temperature range	–30		85	

CURRENT CONSUMPTION

Over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	NOM	MAX	UNIT
Power-off mode: only battery supply present, other supplies pulled down. From VBAT (2.3–5.5 V)		0.54	4.4	µA
Deep-sleep mode: 1.8 V I/O present, other regulated supplies pulled down, plug detection enabled, other modules disabled. From VBAT (3.8 V)		1.4	15.3	
Sleep mode: all supplies present. No accessory connected, plug detection enabled, other modules disabled. From VBAT (3.6 V)		2.4	17.6	
Sleep mode: all supplies present. Accessory connected, accessory unplug and button press detections enabled, other modules disabled. From VBAT (3.6 V)		15.2	40.5	

UPLINK MICROPHONE CHANNEL

Over operating free-air temperature range (unless otherwise noted)

UPLINK MICROPHONE CHANNEL					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Single-ended or differential input swing 0 dBFs (THD > 40 dB)				2	Vpp
Single-ended or differential input slew rate				1	V/µs
Programmable preattenuation		–6		0	dB
Programmable preamplifier gain		6		30	dB
Programmable preamplifier gain step size			6		dB
Absolute gain accuracy	Gain = Min	–0.5		0.5	dB
Relative gain accuracy	Gain = Min to Max referenced to gain = Min	–0.5		0.5	dB
Gain step size accuracy	Referenced to step = Typ	–0.25		0.25	dB
Gain variation with frequency	f = 20–20 kHz, relative to f = 1 kHz without external capacitor	–0.5		0.5	dB
Single-ended input resistance		160	200	240	kΩ
Total harmonic distortion in 20–20 kHz bandwidth Gain = Min, f = 1 kHz	0 dBFs		–42	–40	dB(A)
	–10 dBFs		–72	–70	
	–20 dBFs		–67	–65	
	–40 dBFs		–47	–45	
	–60 dBFs		–27	–25	
Input referred idle channel noise (including microphone bias and typical microphone biasing circuitry)	20 Hz to 8 kHz, gain = 6 dB		10.9	14.8	µVrms(A)
	20 Hz to 8 kHz, gain = 24 dB		2.5	3.3	
	20 Hz to 20 kHz, gain = 6 dB		13.6	18.6	
	20 Hz to 20 kHz, gain = 12 dB		6.7	9.6	
	20 Hz to 20 kHz, gain = 18 dB		4.1	5.6	
	20 Hz to 20 kHz, gain = 24 or 30 dB		3	4	
Signal-to-noise ratio	20 Hz to 8 kHz, gain = 6 dB	92	98		dB(A)
	20 Hz to 8 kHz, gain = 24 dB	86	92		
	20 Hz to 20 kHz, gain = 6 dB	90	96		
	20 Hz to 20 kHz, gain = 24 or 30 dB	84	90		
Power supply rejection from VBAT	Gain = Min				dB(A)
	VBAT > 2.3 V, f < 1 kHz	74			
	VBAT > 2.3 V, f < 8 kHz	56			
	VBAT > 2.3 V, f < 20 kHz	48			
	VBAT > 2.5 V, f < 1 kHz	80			
	VBAT > 2.5 V, f < 8 kHz	62			
	VBAT > 2.5 V, f < 20 kHz	54			
Antialias attenuation at Fs	6-dB gain	15	22		dB
	24-dB gain	30	40		
Interchannel crosstalk and separation	Input at 1 kHz and –20 dBFs Preamplifier Gain = 18 dB			60	dB
Input-to-output leakage	Input at 1 kHz and 0 dBFs		–80	–74	dB
Common mode rejection	20 Hz to 20 kHz		60	45	dB
Delay	MicAmp input to McPDM output			4	µs
Total uplink current from VBAT = 3.6 V (with analog microphone load)	Mono		3	4.6	mA
	Stereo		5.9	7.8	

ANALOG MICROPHONE BIAS

Over operating free-air temperature range (unless otherwise noted)

ANALOG MICROPHONE BIAS					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Positive supply voltage (VDDAMBIAS)	At the pad	2.3	3.6	5	V
Negative supply voltage (GNDAMIC)	At the pad		0		V
Output voltage (V_{OUT})	Normal mode	2.06	2.1	2.14	V
	Sleep mode	2.06	2.1	2.2	
Output current (I_L)	Normal mode	0	0.6	2	mA
	Sleep mode	0		0.2	mA
Integrated noise	f = 20 Hz to 8 kHz		1.65	2.3	µVrms (P)
	f = 20 Hz to 8 kHz		3	4	µVrms (A)
	f = 20 Hz to 20 kHz		3.5	5	µVrms (A)
Power supply rejection from VDDAMBIAS	I_L = 0 to Max, C_f = Min to Max				dB(A)
	VDDAMBIAS > 2.3 V, f < 1 kHz	74			
	VDDAMBIAS > 2.3 V, f < 8 kHz	56			
	VDDAMBIAS > 2.3 V, f < 20 kHz	48			
	VDDAMBIAS > 2.5 V, f < 1 kHz	80	100		
	VDDAMBIAS > 2.5 V, f < 8 kHz	62	80		
	VDDAMBIAS > 2.5 V, f < 20 kHz	54			
Load transient	80% I_L Max in 1 µs			30	mV
Startup time	V_{OUT} at 90%			200	µs
Short-circuit current limit	Output shorted to ground	3	6	10	mA
Output impedance in power-down mode	dc, with respect to GND VOUT from 0 to 2.1 V V2V1 enabled	3			MΩ
Pulldown	DC, with respect to GND			200	Ω
Quiescent current	Normal mode, I_L = 0–Max		200	300	µA
	Sleep mode, I_L = 0–Max/10		10	20	
Parasitic board capacitor C_p				200	pF
External filter resistor value R_f		185	200	215	Ω
External filter capacitor value C_f	Ceramic capacitor	0	220	250	nF
External capacitor ESR	f = 100 kHz			6	Ω
Biasing resistance R_b		2.09	2.2	2.31	kΩ
Microphone equivalent resistance R_m		1	3	6	kΩ

DIGITAL MICROPHONE BIAS

Over operating free-air temperature range (unless otherwise noted)

DIGITAL MICROPHONE BIAS					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Positive supply voltage (VDDDMBIAS)	At the pad	2.3	3.6	5	V
Negative supply voltage (GNDDMIC)	At the pad		0		V
Output dc voltage (V_{OUT})	Normal mode, I_L = 0 to Max	1.75	1.8	1.85	V
	Sleep mode, I_L = 0 to Max/10	1.8	1.85	1.9	
Output current (I_L)		0		10	mA
Power supply rejection from VDDDMBIAS	I_L = 200 µA to Max, normal mode				dB(A)
	V_{OUT} = 1.8 V, f < 20 kHz	40			
Load transient	80% I_L Max in 1 µs			30	mV
Output impedance in power-down mode	DC, with respect to GND	1			MΩ
Startup time				600	µs
Short-circuit current limit	Output shorted to ground	20	30	40	mA
Quiescent current	Normal mode		20	30	µA
	Sleep mode		7	10	
External capacitor value		0.9	2.2	3.3	µF
External capacitor ESR	f < 100 kHz			0.6	Ω
	1 MHz < f < 10 MHz			0.02	Ω

ANALOG LOOP, LINE-IN TO HEADPHONE OUTPUT

Over operating free-air temperature range (unless otherwise noted)

ANALOG LOOP, LINE-IN TO HEADPHONE OUTPUT					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Programmable gain range in line-in amplifier			42		dB
Programmable gain in line-in amplifier		–18		24	dB
Programmable gain step size			6		dB
Single-ended input resistance		40	50	60	kΩ
Maximum input voltage (0 dBFs)	For single-ended input			2	Vpp
Total analog loop SNR output	Gain = 0 dB, 0.5 V_{rms} signal		90		dB(A)
Total analog loop THDN at FS	LineG = 6 dB, HSDrvG = 0 dB, output = 1 V_{rms}		–66		dB
Total stereo analog loop path quiescent current 85% DC 3.8-V Vbat	From VBAT = 3.8 V		2.5	3.5	mA

DOWNLINK (DAC) CHANNEL TO HEADPHONE OUTPUT

Over operating free-air temperature range (unless otherwise noted)

DOWNLINK (DAC) CHANNEL TO HEADPHONE OUTPUT					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Speaker load resistance (R_L)		16	32		Ω
Single-ended output swing 0 dBFs (THD > 40 dB, –4 dB analog gain in HP mode and –2-dB gain in LP mode)	at the ball $R_L + R_f = 32 + 15 = 47$ Ω	1			Vrms
	at the load $R_L + R_f = 32 + 15 = 47$ Ω	0.7			
Programmable gain range		–30		0	dB
Programmable gain step size			2		dB
Absolute gain accuracy	Gain = Max	–0.5		0.5	dB
Relative gain accuracy	Relative to gain = Max	–0.5		0.5	dB
Gain step size accuracy		–0.25		0.25	dB
Gain variation with frequency	f = 20 Hz to 20 kHz, gain = Min to Max relative to 1 kHz at the ball	–1.1	–0.85	–0.6	dB
Idle channel noise	LP mode, at the ball		10	14	μVrms(A)
Gain = Max	HP mode, at the ball		6	9	
Dynamic range –60-dBFs output with –4-dB analog gain	HP mode		104		dB(A)
Dynamic range	LP mode	100	103		dB(A)
–60-dBFs output with –30-dB analog gain	HP mode	105	108		
Signal-to-noise ratio	–1-dBFs output, LP mode	94	97		dB(A)
	–1-dBFs output, HP mode	98	101		
	–10-dBFs output, LP mode	86	89		
	–10-dBFs output, HP mode	90	93		
Total harmonic distortion in 20 Hz–20 kHz bandwidth (sine-wave @1 kHz, gain = Max)	0 dBFs		.	–40	dB(A)
	–10 dBFs			–70	
	–20 dBFs			–56	
	–40 dBFs			–36	
	–60 dBFs			–16	
THD+N	R_L = 32 Ω, Pload = 20 mW (–2.5 dBFS)		0.012	0.1	%
Power supply rejection from VBAT	Gain = Max, 217 Hz TDMA pulse noise	80	100		dB(A)
HS reference GNDHS noise rejection	f = 1 kHz, 10 mV_{rms} amplitude	40			
Group delay				7.1	μs
Offset	From stand-alone IC	–16		16	mV
	After system compensation	–2		2	
L/R gain mismatch	at 0 dBFs, 1 kHz	–0.5		0.5	dB
L/R phase mismatch	at 0 dBFs, 1 kHz	–10		10	degrees
L/R cross-talk	at 0 dBFs, 1 kHz			–60	dB
Output impedance	Driver and pulldown disabled	1			MΩ
Average playback current from VBAT	LP mode		5.3	7	mA
	HP mode		7.4	9.23	

EARPHONE PATH SPECIFICATION

Over operating free-air temperature range (unless otherwise noted)

EARPHONE PATH SPECIFICATION					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Speaker load resistance (R_L)		16	32	100	Ω
Output differential swing 0 dBFs (THD > 40 dB) at 6-dB analog gain	R_L = Typ	2			Vrms
	R_L = Min	1.42			Vrms
Programmable gain range		–24		6	dB
Programmable gain step size			2		dB
Absolute gain accuracy	Gain = Max	–0.5		0.5	dB
Relative gain accuracy		–0.5		0.5	dB
Gain step size accuracy		–0.25		0.25	dB
Gain variation with frequency	f = 20 Hz to 20 kHz, relative to 1 kHz	–0.8	–0.55	0.3	dB
Idle channel noise	f = 20 Hz to 20 kHz		32	45	µVrms(A)
Dynamic range, –60-dBFs output with –24-dB analog gain		87	97		dB(A)
SNR, 0-dBFs output	f = 20 Hz to 20 kHz	87	97		dB(A)
Total harmonic distortion (sine wave @1 kHz, gain = Max)	0 dBFs		–60	–40	dB(A)
	–10 dBFs		–70	–60	
	–20 dBFs		–70	–60	
	–40 dBFs		–50	–40	
	–60 dBFs		–30	–20	
THD+N	R_L = TYP, 0 dBFS output		0.02	0.1	%
THD+N	R_L = TYP, –6 dBFS output		0.015	0.1	
Differential offset		–25		25	mV
Power supply rejection from VBAT	Gain = Max	80	100		dB(A)
Group delay	SINC filter			4.125	µs
	FIR filter			1	µs
Average current from VBAT			3.7	4.8	mA

AUX-OUTPUT PATH SPECIFICATION

Over operating free-air temperature range (unless otherwise noted)

AUX-OUTPUT PATH SPECIFICATION					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Load resistance (R_L)		10	150		kΩ
Output differential swing 0 dBFs (THD > 40 dB)	R_L = Typ	1.7			Vrms
Programmable gain range			58		dB
Programmable gain step size			2		dB
Absolute gain accuracy	Gain = 0 dB	–1.0		1.0	dB
Gain step size accuracy	Gain = 6 to –40 dB	–0.25		0.25	dB
	Gain = –40 to –50 dB	–0.5		0.5	dB
Relative gain accuracy	Gain = 6 to –40 dB	–0.5		0.5	dB
	Gain = –40 to –50 dB	–1.0		1.0	dB
Gain variation with frequency	f= 20 Hz to 20 kHz relative to 1 kHz Gain = 0 dB	–0.5		0.5	dB
Dynamic range, –60-dBFs output with –24-dB analog gain		87	90		dB(A)
SNR, 0-dBFs output		80	90		dB(A)
THD+N	10-kΩ load, HFPGA = 0 dB, 1-kHz signal				%
	1-Vpp single-ended output		0.07		
	2-Vpp single-ended output		0.4		
	1-Vpp differential output		0.07		
	2-Vpp differential output		0.4		
Idle channel noise			40	50	µVrms(A)

HANDS-FREE PATH SPECIFICATION

Over operating free-air temperature range (unless otherwise noted)

HANDS-FREE PATH SPECIFICATION					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Input supply	Battery	2.3		5	V
	SMPS boost			5.5	
Maximum output power (PGA = 0 dB)	R_L = 8 Ω				W
	VDDHF = 5.5 V (THD > 40 dB)	1.3	1.5		
	VDDHF = 4.5 V (THD > 40 dB)	0.9	1		
	VDDHF = 3.6 V (THD > 40 dB)	0.55	0.6		
	VDDHF = 2.8 V (THD > 40 dB)	0.24	0.28		
	VDDHF = 2.3 V (THD > 30 dB)	0.15	0.2		
Programmable gain range (PGA)		–52		6	dB
Programmable gain step size (PGA)			2		dB
Absolute gain accuracy	Gain = 0 dB	–1		1	dB
Relative gain accuracy	Gain = 6 to –40 dB	–0.5		0.5	dB
	Gain = –40 to –50 dB	–1		1	
Gain step size accuracy	Gain = 6 to –40 dB	–0.25		0.25	dB
	Gain = –40 to –50 dB	–0.5		0.5	
Gain variation with frequency	f = 20 kHz relative to 1 kHz	–1.25	–1	–0.75	dB
Dynamic range, –60-dBFs output with –24-dB HFPGA gain		85	93		dB(A)
Idle channel noise	Gain = –24 dB		65	170	µVrms(A)
Total harmonic distortion in f = 20 Hz to 20 kHz (sine wave @ 1 kHz, 0-dB PGA gain setting)	R_L = 8 Ω, VDDHF > 3.6 V				dB(A)
	25 mW < P_{OUT} < 0.5 W		–55	–50	
	1 mW < P_{OUT} < 25 mW		–45	–40	
Power supply rejection from VBAT	Gain = 0 dB				dB(A)
	Idle channel	55	65		
	Intermodulation	70	80		dBc
Carrier frequencey	19.6 MHz PDM clock		384		kHz
	17.64 MHz PDM clock		353		kHz
Average quiescent current from VBAT	Mono		2	3	mA

VIBRA DRIVER PATHS

Over operating free-air temperature range (unless otherwise noted)

VIBRA DRIVER PATHS					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Input supply VDD	Battery or SMPS boost	2.3		5.5	V
DC output voltage	Left channel, R_L = 16 Ω				V
	VDDVIB = 4.8 V	3.3	3.6		
	VDDVIB = 3.8 V	2.6	2.9		
	VDDVIB = 2.5 V	1.6	1.7		
	Right channel, R_L = 8 Ω				V
	VDDVIB = 4.8 V	3.6	3.9		
	VDDVIB = 3.8 V	2.7	3		
	VDDVIB = 2.3 V	1.6	1.8		
Absolute gain accuracy		–0.5		0.5	dB
Voltage step			50		mV
Gain variation with frequency	f = 250 Hz to 8 kHz relative to 1 kHz	–0.5	0	0.5	dB
Total harmonic distortion in f = 20 Hz to 8 kHz	R_L = 8 Ω, V_{DD} > 3.6 V, –1 dBV_{rms}		–35	–30	dB(A)
Latency	PDM input			20.8	µs
	PCM input			10.4	
Load resistance R_L		8	16		Ω
Average quiescent current from VBAT	Mono		1	1.5	mA

INPUT CLOCK PARAMETERS

Over operating free-air temperature range (unless otherwise noted)

SYSTEM CLOCK					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Input frequency accuracy		–100		100	ppm
Input swing	Square wave	1.65		1.89	V
	Sine wave, input common mode 0.5 to 0.7 V	0.4		1	Vpp
Input SSB phase noise @ 1 kHz	12 MHz		–89	–86	dBc/Hz
	19.2 MHz		–86	–83	
	26 MHz		–83	–80	
	38.4 MHz		–80	–77	

SLEEP CLOCK

Over operating free-air temperature range (unless otherwise noted)

SLEEP CLOCK					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Input frequency			32,768		Hz
Input frequency accuracy		–1000		1000	ppm
Input duty cycle		40		60	%
Input SSB phase noise	@ 100Hz		–108	–105	dBc/Hz
	@ 1 kHz		–128	–125	
Input integrated jitter	20 Hz to 20 kHz flat		0.61	0.86	nsrms
	80 Hz to 20 kHz flat		0.31	0.43	

APPLICATION INFORMATION

UPLINK PATH DESCRIPTION

The voice uplink path includes two low-noise input amplifier stages (MicAmpL and MicAmpR) and two ADCs dedicated to the three microphone inputs and stereo auxiliary/FM inputs. Two low-power input amplifiers (LineInAmpL and LineInAmpR) enable stereo analog loops (LB0, LB1) to the downlink section, independent and concurrent with stereo microphone uplink to OMAP4. The auxiliary/FM radio left and right channels can be connected to the microphone preamplifiers for recording, or to a line-in amplifier for direct analog loop to downlink drivers, or simultaneously to both.

Analog microphone bias outputs, MBIAS and HBIAS, have a dedicated supply pin (VDDABIAS), which can be connected to the battery or to an external boost. If full PSR performance is required in a system with minimum battery level below 2.5 V, the latter connection is recommended.

Microphone bias blocks can be set to sleep mode for low quiescent current consumption. In sleep mode, only the output voltage specification is ensured with the specified sleep mode load current.

Mapping of analog inputs to uplink data channels UL0 and UL1 connected to the OMAP4 is indicated in the following table:

	UL0	UL1	LB0	LB1
Main microphone, MMIC	X			
SubMicrophone, SMIC		X		
Headset microphone, HSMIC	X	X		
Left auxiliary/FM radio	X		X	
Right auxiliary/FM radio		X		X

For microphone bias connection, if the negative terminal of the microphone is available, which is usually the case for device internal microphones, the board schematic for a fully differential input shown in Figure 3 is proposed. This approach minimizes differential coupling but provides almost no rejection from bias noise voltage (MBIAS).

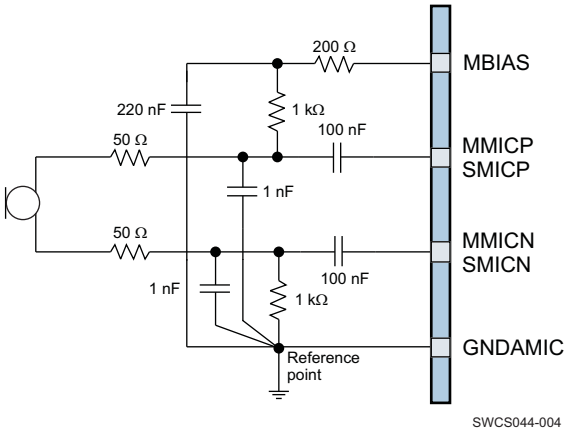


Figure 3. Board With Available Negative Terminal

If the negative terminal of the microphone is not available (that is, it is directly connected to ground), which is usually the case for accessory microphones, the board schematic for a pseudodifferential input shown in Figure 4 is suggested. This approach can suffer from differential coupling, but provides good rejection from bias noise voltage (HBIAS).

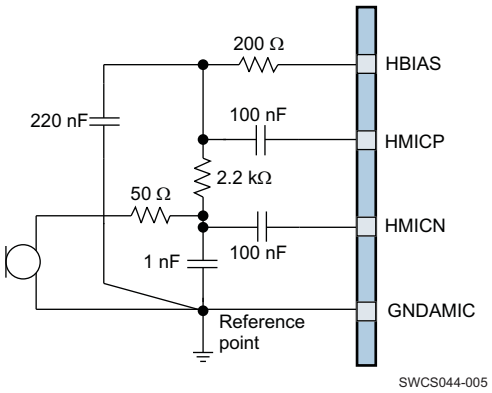


Figure 4. Board With Unavailable Negative Terminal

In all board layouts, the star connection of all the ground lines to a single via to the ground plane (reference point) is highly recommended to minimize degradation from unequal potential grounds.

The schematics and component values in Figure 3 and Figure 4 are general proposals and may not be the optimal choice for specific user applications.

Two LDOs provide an external voltage of 1.8/1.85 V to bias digital microphones (DBIAS1 and DBIAS2). One bias generator can bias several digital microphones at the same time, with a total maximum output current of 10 mA. Digital microphone inputs and clocks are supported by OMAP.

DOWNLINK PATH DESCRIPTION

Mapping of audio data inputs from the OMAP4 to audio driver outputs is shown in the following table.

	DL0	DL1	DL2	DL3	DL4	I²C or Frame(1)	LB0	LB1
Earphone	X(2)							
Left headset	X						X	
Right headset	X	X						X
Left hands-free			X				X	
Right hands-free			X	X				X
Left auxiliary			X(3)				X	
Right auxiliary			X(3)	X(3)				X
Right vibrator					X	X		
Left vibrator					X	X		

(1) The frame line can be used for register write (for example, vibrator data registers) in command mode.
(2) This path cannot be concurrent with L/R headset paths.
(3) These paths can be concurrent, but not independent of L/R hands-free paths.

Headphone/Headset Paths

For music playback, the analog headset path can be configured in two different modes:

- Low-power mode (LP)
- High-performance mode (HP)

The LP mode system is designed to maximize playback time while maintaining better audio performance than provided by current compression algorithms. The only input clock required in this mode is the RTC at 32,768 Hz.

The HP mode improves the dynamic range (DR) performance by 5 dB with tradeoff of increased current consumption compared to LP mode. A high-quality clock (that is, generated by VTCXO) is required in this mode.

The headset path modules (DAC and HS driver) can be individually set in LP and HP modes.

The DAC is followed by a class AB single-ended HS driver, to provide a signal up to 1 Vrms at the ball. Programmable analog attenuation is available in the HS driver. The overall gain of the system is segmented between this analog gain and the digital gain of the application processor, with a minimum step of 0.1 dB. The HS path can drive headphone or line-out loads. Optional EMC or ESD protection circuitry can be inserted between the stereo HS driver and the load connector, without performance degradation at the ball. A single ground feedback is brought star connected from the connector ground to the stereo HS driver feedback.

Hands-Free/Speaker Paths

Hands-free/speaker drivers can be connected to a battery or to an external boost. To reach 1-W output power from a mono speaker, a boosted supply equal to or greater than 4.5 V is recommended.

The board can be designed without an output filter if the traces from the TWL6040 to hands-free (HF) speakers are short. A ferrite bead filter can be used if the board design is failing radiated emission. In both cases, the audio performance is maintained.

There is a short-circuit protection for HF amplifiers to limit power dissipation. A short circuit can exist between output terminals, output and ground, or output and battery.

Short circuit detection in at least one of the two drivers automatically disables both HF drivers and generates an interrupt.

Vibra Paths

Two high-efficiency differential drivers, capable of driving rotational, linear multifunction vibrator devices, are provided. Each vibrator can be independently supplied by an external power source. The left vibrator driver RDSON is optimized for a 16-Ω equivalent load, whereas the right vibrator driver RDSON is optimized for an 8-Ω equivalent load (higher current). Loads with higher equivalent resistance value than stated above are also supported.

Each of the vibrators can be driven through PDM or PCM data. The PDM data comes from the 5th downlink channel. The PCM data can be sent through the PDM interface command mode at a maximum rate of 48 kS/s, or through the I^2C interface for near DC signal. Better than 8-bit resolution on lower bandwidth can be achieved through the PCM signal by averaging the data.

There is no analog or digital gain in the TWL6040 vibrator paths; that is, the signal amplitude is entirely set in the digital companion IC.

Similar to the hands-free drivers, there is a short-circuit protection for vibrator drivers to limit power dissipation if the current exceeds 500 mA in any of the output transistors. Short-circuit detection in at least one of the two drivers automatically disables both vibrator drivers and generates an interrupt.

External Boost

An external boost can be used to supply the following functions:

- Hands-free stereo drivers
- Left and right vibrator drivers
- Main and headset microphone biasing LDOs

Any of the corresponding modules in the TWL6040 device can be independently powered by the battery or by the output of this external boost.

The external boost should provide a minimum output voltage of 4.5 V to allow each HF driver to deliver a typical 2-W peak power into an 8-Ω load. Larger output voltage values enable more output power in the HF loads, but it must not exceed 5.5 V dc for reliability reasons.

By default, the two HF drivers work in phase quadrature (90-degree phase shift) to reduce the rms load current. Figure 5 shows the stereo HF load current waveforms for worst-case (close to 100% modulation or 4-W stereo output power) and typical (less than 50% modulation or 1-W stereo output). Figure 5 also indicates the driver sinking the current (left or right).

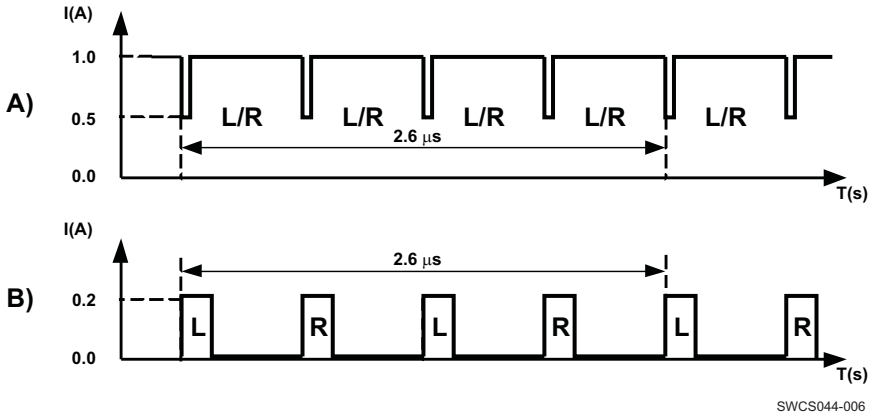


Figure 5. Current Load Waveforms, Worst-Case A) and Typical B)

The following table shows the external boost SMPS recommendations.

Parameter	Test Conditions	Min	Typ	Max	Units
Input voltage	at the ball	2.3		5.0	V
Output voltage			4.5	5	V
Output current		0.003		1.25	A
Output peak power	Stereo HF			4.5	W
	Strereo HF + mono Vibra			5.625	W
Output average power(1)	Stereo HF			0.31	W
	Strereo HF + mono Vibra			0.4	W
Efficiency	I_L=3 mA to 1.3 A	80	90		%
Start-up time				4	ms
Power supply rejection from VBAT	f = 217 Hz	20	30		dB
Output current limit for short-circuit detection				1.6	A

(1) The Max/Typ ratio is based on 12-dB crest factor audio signal.

ACCESSORY DETECTIONS

The standard connector is shown in Figure 6, and has the following terminals:

1. Left headset speaker input
2. Right headset speaker input
3. Microphone input
4. Ground return for speakers and microphone
5. Open/ground switch input

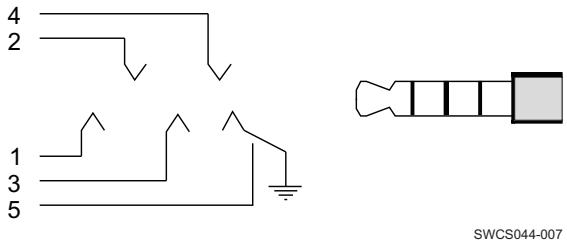


Figure 6. Standard Connector

The TWL6040 is compatible with a system supporting the standard 2.5-mm and 3.5-mm audio-jack connector shown in Figure 7:

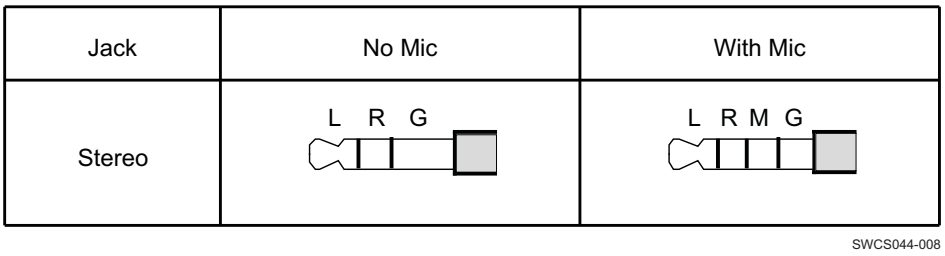


Figure 7. Standard 2.5-mm and 3.5-mm Audio-Jack

With proper board wiring TWL6040 is compatible also with L-R-G-M -jack.

The TWL6040 is not compatible with the 2.5-mm and 3.5-mm audio-jack connectors shown in Figure 8. If this type of connector is inserted, the system performances and/or functionality are not assured, but the TWL6040 is not damaged.

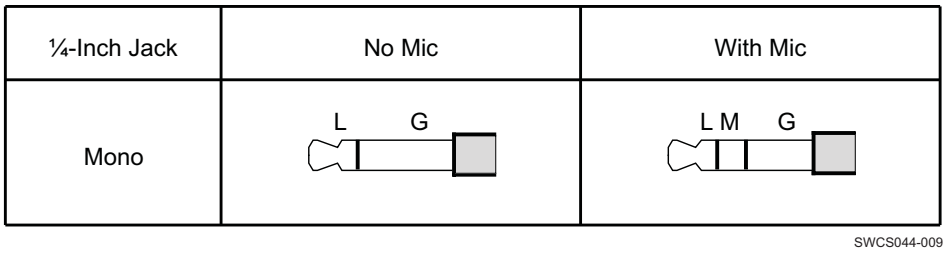


Figure 8. Incompatible 2.5-mm and 3.5-mm Connectors

Plug Detection

The TWL6040 supports plug detection through a mechanical switch closing to ground when a connector is inserted. The plug detection is implemented as a simple comparator with a pullup resistance. The comparator output is debounced to avoid false detection due to perturbation, such as ESD events. When a plug or unplug event is detected, interrupt signal PLUGINT is generated. The maximum value of the plug resistance R_p is 10 Ω.

Figure 9 shows the plug-detection circuit.

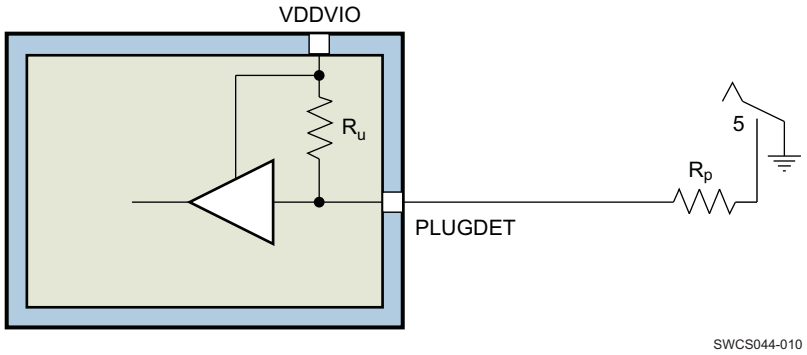


Figure 9. Plug Detection Circuit

Send/End Button Detection

Some headsets have a manual switch for submitting send/end signals to the terminal through the microphone input pin. The two possible configurations are:

- The button switch is parallel to the microphone (most common).
- The button switch is in series with the microphone.

The two configurations are shown in Figure 10.

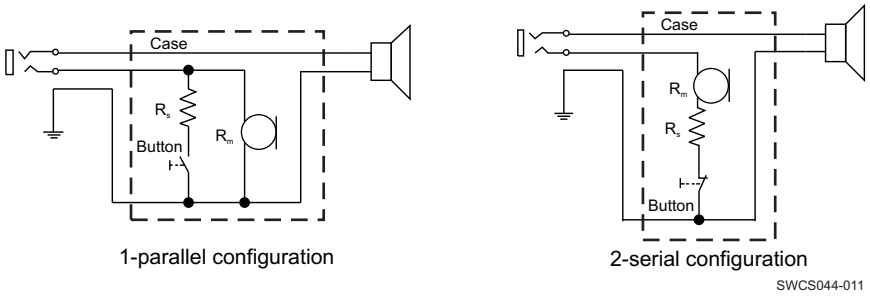


Figure 10. Manual Switch Configuration

In both configurations, the detection is based on an impedance detection involving the microphone. The detection is assured for a maximum R_S of 100 Ω and a microphone having a current-to-voltage transfer function within the mask described in Figure 11.

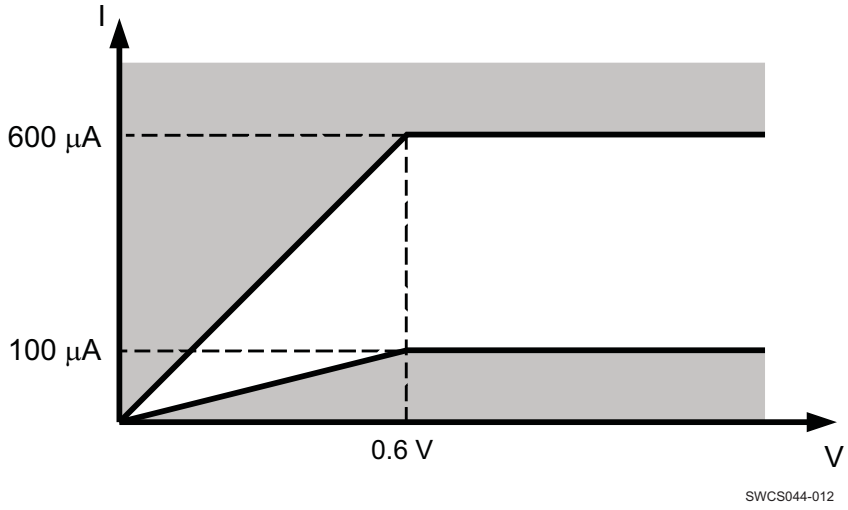


Figure 11. Microphone Current-to-Voltage Transfer Function

Two detection mechanisms are implemented on the TWL6040 to address the parallel and serial hook configurations. By default, these detections are concurrent, but they can be independently disabled by the HKPARADIS bit in register HKCTL1 and the HKSERDIS bit defined in register HKCTL2.

In the parallel configuration for send-event detection, the VDDV2V1 supply pulls up the bias resistance R_b to 2.1 V, while the microphone bias amplifier is in high-impedance output mode. It also provides a threshold V_{th1} for the hook comparator COMP1 through a resistor divider. This comparator is used to detect the short of the microphone bias. The detection analog block diagram is described in Figure 12, and the entire system is powered from the VDDV2V1 supply. During settling and comparison, switch R_i is closed and as much as 600 µA can flow from VDDV2V1 to the microphone, and up to 1.1 mA if the button is pressed.

The same mechanism is used for end-event detection, except that the LDO HBIAS is already biasing the microphone, and VDDV2V1 is used only as a supply for the comparator.

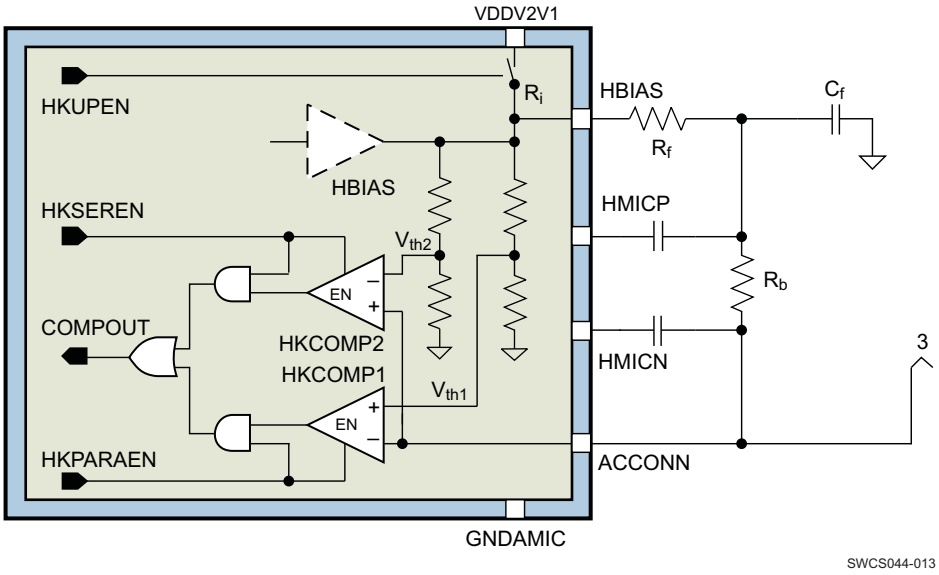


Figure 12. Parallel/Serial Configuration Detection

The detection is performed with a duty cycle compatible with system quiescent-current requirements and timing of the mechanical short. The sequence is programmed by setting three parameters based on the RTC clock:

- Interval period between detection trials
- Settling time (dependent on external RC filter)
- Debounce time for comparison

The minimum recommended duration consists of eight clock cycles for settling and eight clock cycles to debounce the output of the comparator. With one detection every 100 ms, this on-duration allows a duty cycle smaller than 1/500 and a minimum sleep current. Figure 13 shows the timing diagram.

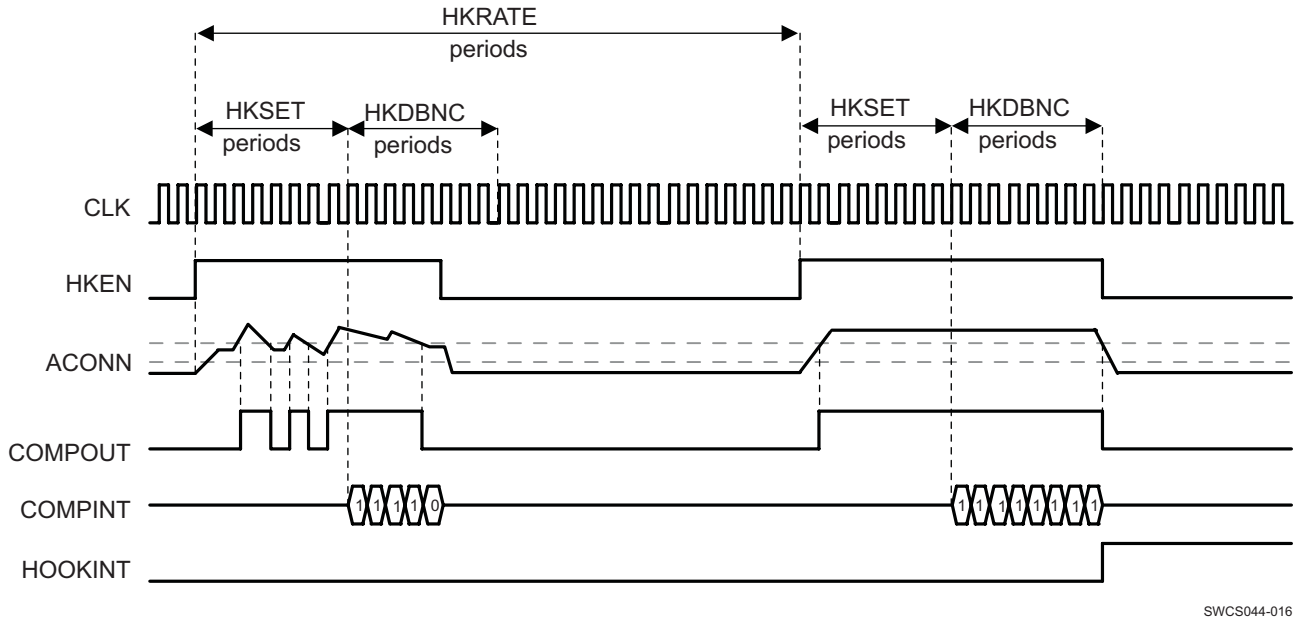


Figure 13. Detection Timing

In end event mode detection, when the HMBIAS module is enabled, the duty cycle is disabled and the analog module detection is always on to avoid transient perturbations coupling to the uplink channel. The duty cycle in this mode can be restored by setting HKSWEN high.

The same detection scheme can be used for serial configuration. The comparator HKCOMP2 can work synchronously with HKCOMP1 and their output can be combined before the debounce function.

When a send event is detected, an interrupt signal is generated and the switch between VDDV2V1 and PAD_MBIAS is disabled. For end event detection, an interrupt signal is generated.

CLOCK SYSTEM

The frequency plan is based on a 48 kS/s audio data rate for all channels. The data converters use a fixed oversampling ratio (OSR) equal to 80 (3.84 MHz). The audio data PDM interface runs at five times the OSR rate, using a clock equal to 19.2 MHz. The application companion uses sample rate converters to interface with other sample rates (for example, 44.1 kHz).

In the specific case of low-power audio playback (LP mode), where only the headphone path is active, the TWL6040 supports the 44.1 kS/s and 48 kS/s rates. The ratio between audio sample rate, data converter clock, and PDM clock remains the same.

The high-quality input clock MCLK from the system can have the following values: 12, 19.2, 26, or 38.4 MHz. The input waveform can be a sine wave or a square wave. If the clock frequency is equal to 19.2 or 38.4 MHz, the clock can be directly divided and level-shifted. If MCLK is 12 MHz or 26 MHz, the high frequency input PLL (HF PLL) generates a 19.2 MHz signal from the MCLK, compatible with the requirement for HS quality in high performance (HP) mode. A clock slicer is inserted between the MCLK input pad and the HF PLL.

The low frequency input PLL (LF PLL) generates a 17.64 MHz or 19.2 MHz signal from the RTC at 32,768 Hz (CLK32K), compatible with the requirement for MP3 playback in low power (LP) mode. In all cases, the input reference clock must meet the phase-noise performance described in INPUT CLOCK PARAMETERS.

Figure 14 shows the clock-system block diagram.

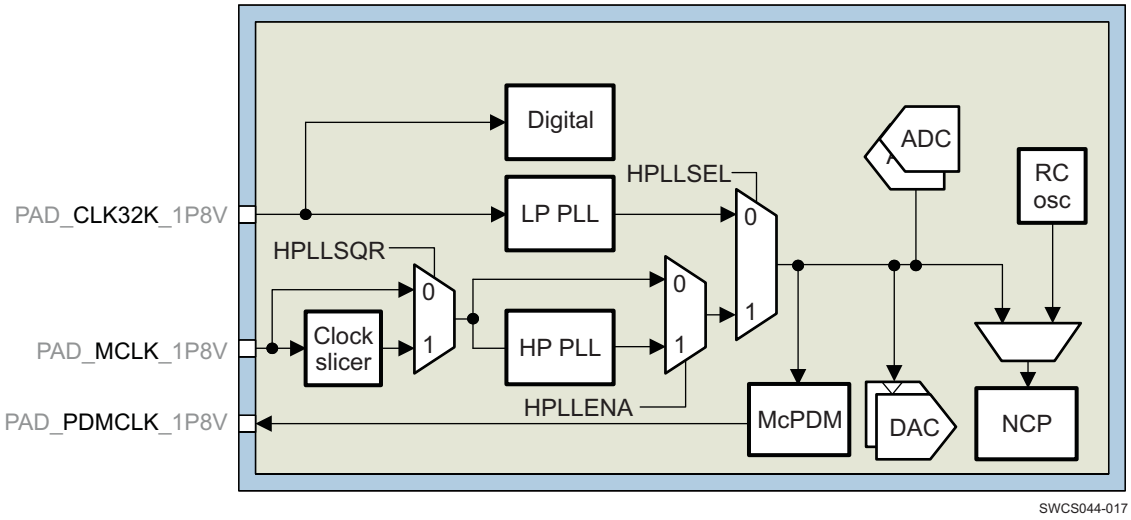


Figure 14. Clock System

POWER MANAGEMENT

The TWL6030 PMIC provides a +2.1-V preregulated supply VDDV2V1 to the TWL6040. The digital I/O buffers and other digital functions are directly powered by the VDDVIO supply for a maximum 5-mA average load current. The TWL6040 has an internal reference system powered from VBAT.

A high-side LDO postregulates VDDV2V1 to VDDLDO supply of +1.6 V for a maximum load of 150 mA. The preamplifiers, PGA, ADCs, DAC, PLL, headset drivers, earpiece driver, auxiliary drivers, and other analog functions use the VDDLDO supply.

An integrated negative charge pump generates a –1.9-V preregulated supply NCPOUT. A low-side LDO postregulates NCPOUT to a VSSLDO supply of –1.6 V for a maximum load of 150 mA, providing the negative supply for the analog functions powered by VDDLDO formerly described.

Figure 15 shows the power-management diagram.

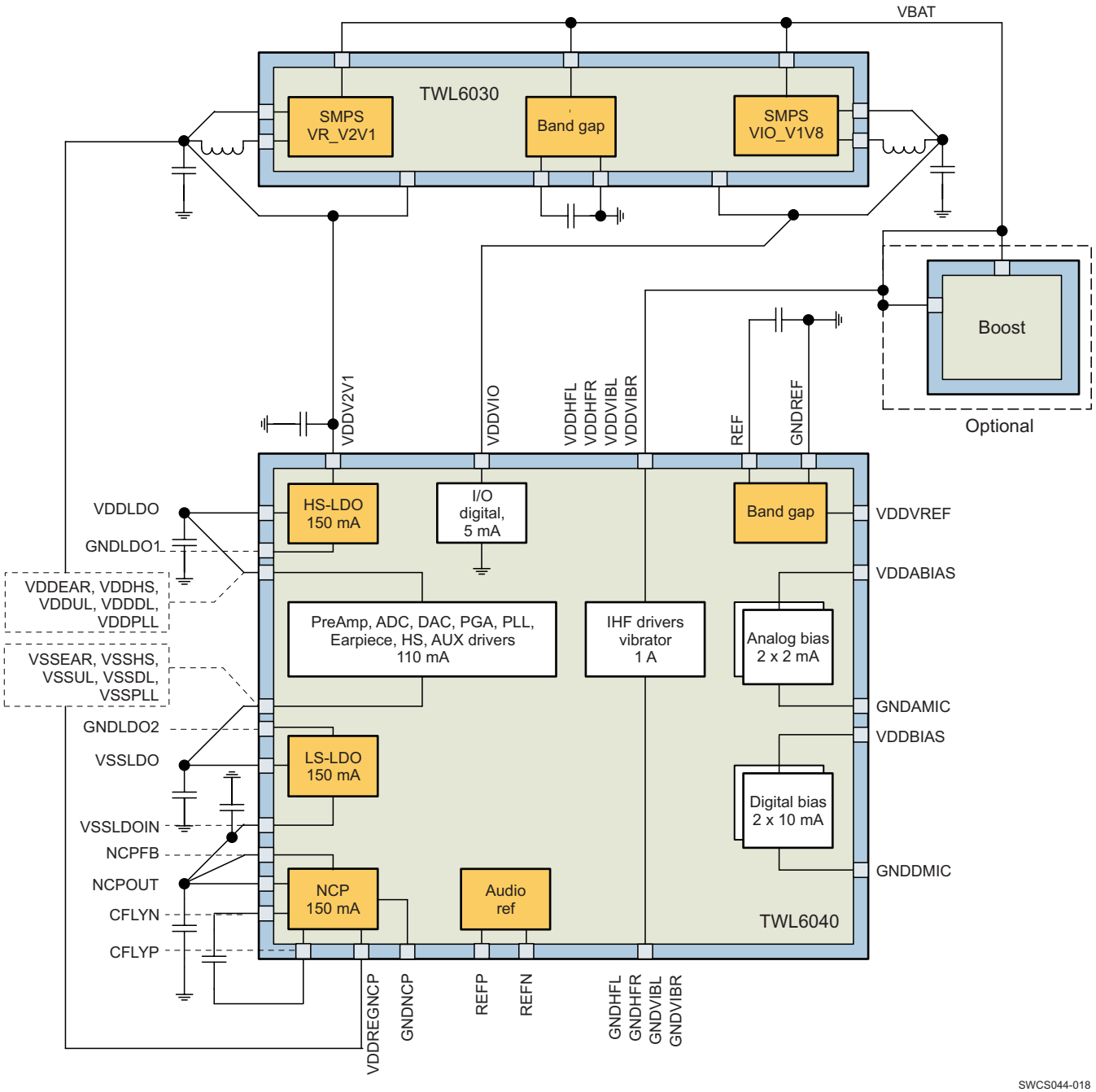


Figure 15. Power-Management Diagram

THERMAL PROTECTION

If the temperature in the TWL6040 increases above a thermal threshold at which damage can occur, a thermal interrupt THINT is generated. Also, immediate action is automatically taken to reduce the amount of power drawn from the device.

Figure 16 shows a timing sequence showing a thermal event.

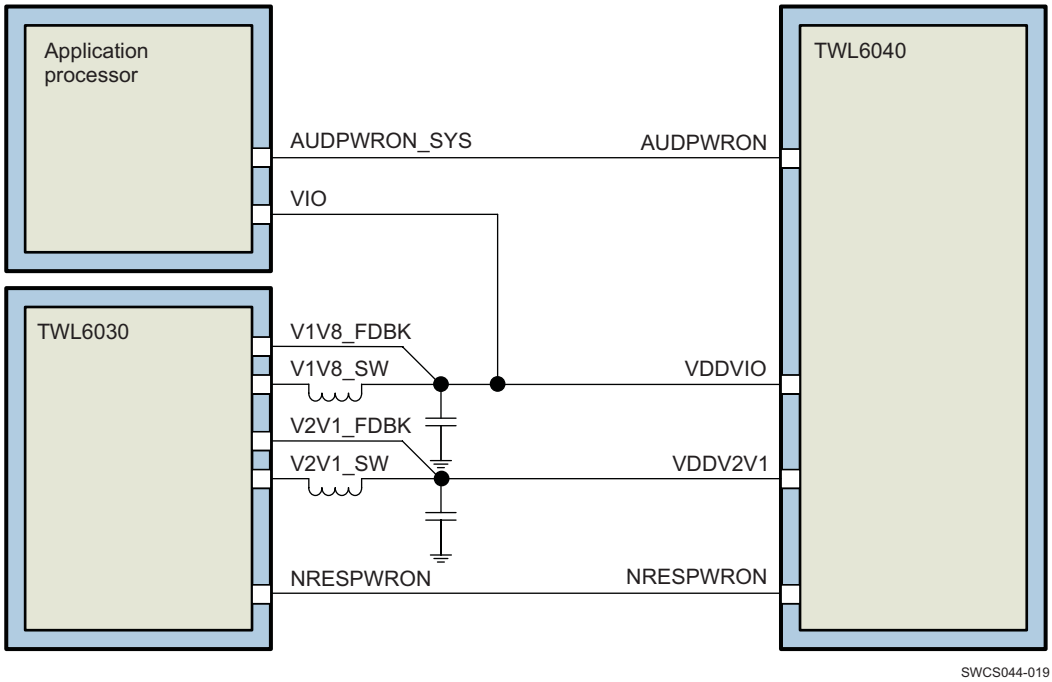


Figure 16. Thermal-Event Timing

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Thermal interrupt threshold	Positive	142	152	162	°C
	Negative	132	142	152	°C

The TWL6040 initiates a power-down sequence (except for the reference system and temperature sensor) when the junction temperature goes above the positive threshold (TSHUTCOMP equals 1). The must to pull the AUDPWRON line down when the thermal-interrupt information is received. In this particular case, pulling AUDPWRON down does not disable the reference system and temperature sensor. The host should only bring the TWL6040 to POWER-ON state (by pulling the AUDPWRON high) when another thermal interrupt is received.

INTERFACES

The TWL6040 has three digital interfaces:

1. I^2C interface for information with noncritical latency
2. PDM interface for the audio signal and the register associated with audio path (gain, control)
3. GPO for audio IC interacting with TWL6040 (drivers, power provider)

Some dual-access registers (addresses 0x0A to 0x1B) can be accessed by the I^2C and PDM interfaces. The concurrent access is disabled by default, and only the PDM interface can write to these registers. The R/W access can be switched to I^2C-only by setting the I2CSEL bit. A concurrent access by the I^2C and PDM interfaces is also possible by setting the PDMI2CSEL bit. In this case, the TWL6040 does not provide arbitration of simultaneous accesses and the functionality of the system cannot be assured. In this mode, software must ensure that access by one interface is complete before using the other one, to avoid collisions.

I^2C

The TWL6040 device provides one I^2C interface. This allows read/write access to the configuration registers of all resources of the system. Table 3 describes the I^2C interface.

Table 3. I^2C Interface

SUPPORTED	NOT SUPPORTED
Compliant to Philips I^2C spec Rev 3.0	General call, bus clear, device ID, CBUS compatibility, SMBus, time-out feature, PMBus, IPMI, ATCA
Slave only (receiver and transmitter)	Master mode (bus arbitration and clock generation)
Standard mode (up to 100 kbits/s)	
Fast mode (up to 400 kbit/s)	
Fast-mode plus (up to 1 Mbit/s)	
High-speed mode (up to 3.4 Mbit/s)	
Four I^2C slave address decoding features	
7-bit device addressing mode	10-bit device-addressing mode
	Clock stretching

The TWL6040 I^2C embeds a single slave address hard coded to 0x4B to address a single register address space of 256 bytes.

PDM Interface

The PDM interface is the oversampled serial interface used for communication between TWL6040 audio and the application processor companion chip. PDM_CLK is 19.2 or 17.64 MHz, and the data rate represented by PDM_FRAME is 1.92 or 1.764 MHz. Words of data can be transmitted from OMAP to the TWL6040 chip using the PDM_DN line (downlink path), but words of data can also be transmitted from the TWL6040 chip to OMAP using the PDM_UP line (uplink path). Both chips are synchronized through the PDM_FRAME line. The OMAP device owns PDM_FRAME by default.

The PDM interface has three modes: normal, command, and test. The normal and command modes are intended for use with OMAP McPDM. The test mode is designed for evaluation and production test.

Figure 17 shows the PDM interface.

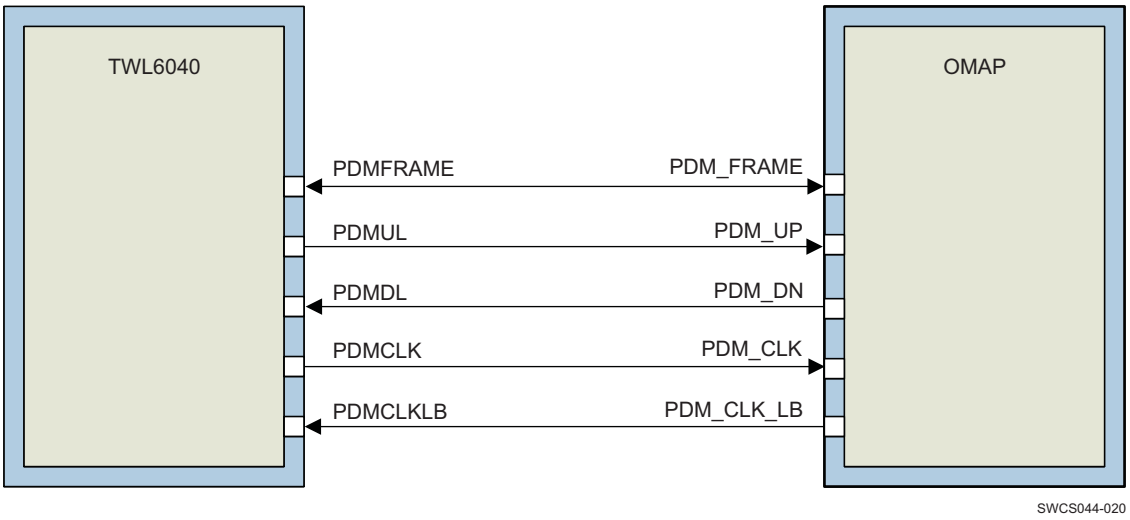


Figure 17. PDM Interface

PDM_CLK is used to generate all internal clocks in the OMAP McPDM interface. The clock-tree architecture in the OMAP may produce multiclock cycle delays under the worst-case conditions. To assure the uplink/downlink data handshake between the TWL6040 and OMAP, the TWL6040 PDM interface uses PDM_CLK_LB, which is the clock reproduced in OMAP. This prevents any critical timing issues.

In normal mode, the ratio between PDM_FRAME and PDM_CLOCK_LB is 10. This ratio is static and the PDM_FRAME low-pulse width is one clock period long. In this mode, the PDM_FRAME signal is driven by OMAP (through its McPDM module) to TWL6040. The OMAP drives the PDM_FRAME line low during one clock cycle, and then drives it high during one clock cycle before releasing the PDM_FRAME driver in Hi-Z state. TWl6040 connects PDM_FRAME to the I/O supply with a pullup resistor to keep it high.

In normal mode, a maximum of 2 × 5 downlink samples can be received during a frame period. As data samples are generated at 3.84 MHz, this mean that two words of five samples can be transmitted during one frame cycle. The receive channels can be enabled through I^2C register bits. A maximum of 2 × 2 uplink samples can be transmitted during a frame. The transmit channels can be enabled by I^2C register bits.

Figure 18 shows the timing in normal mode with two downlink and two uplink channels enabled.

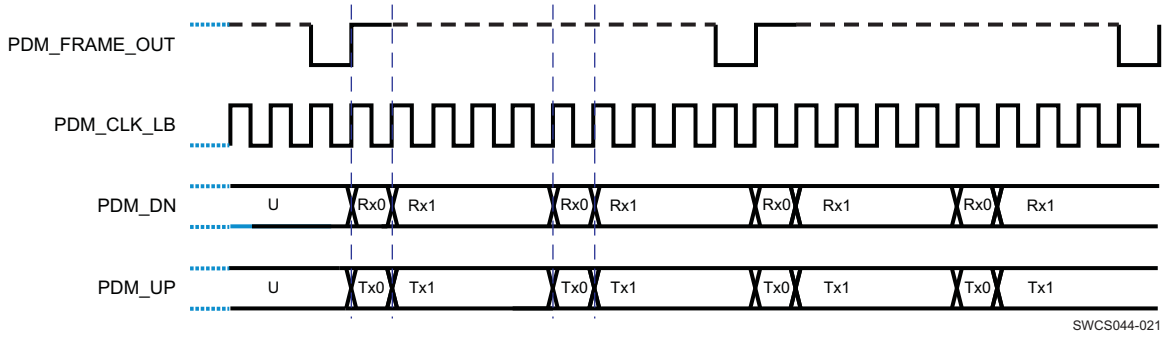


Figure 18. Normal Mode With Two Downlink and Two Uplink Channels Enabled

OMAP starts to send downlink packet on the first rising edge of PDM_CLK_LB, after PDM_CLK_LB goes from high to low while PDM_FRAM_OUT is low. This is the start downlink condition. The uplink path has the same timing as its downlink path.

Figure 19 shows the timing in normal mode with five downlink and two uplink channels enabled.

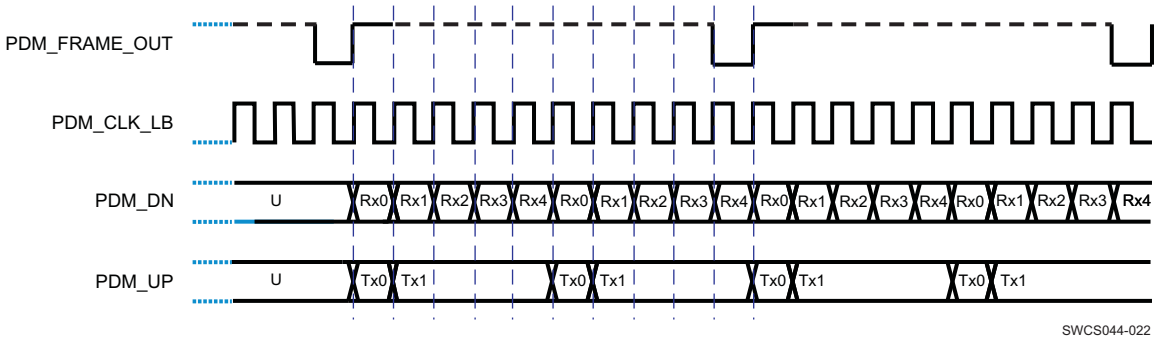


Figure 19. Normal Mode With Five Downlink and Two Uplink Channels Enabled

In command mode, register data can be sent from the OMAP to the TWL6040 using the PDM_FRAME line. This can be the case when OMAP attempts to change the audio gain value on the fly without using the I^2C interfaces, which may be busy, and add a timing mismatch between signal and gain correction. The command mode is available by default, but can be disabled by register.

General-Purpose Interface

The TWL6040 audio provides three general-purpose digital output buffers accessible through the I^2C interface. The goal is to make provisions for the interface of external audio devices or power providers, such as HAC drivers, high-voltage drivers for piezo-electric loads, or external boost supplies for internal HF drivers. The default value of these buffers is low and they have pulldown resistors.

POWER-UP AND POWER-DOWN SEQUENCES

Figure 20 shows the schematic diagram for the power-up and power-down sequences.

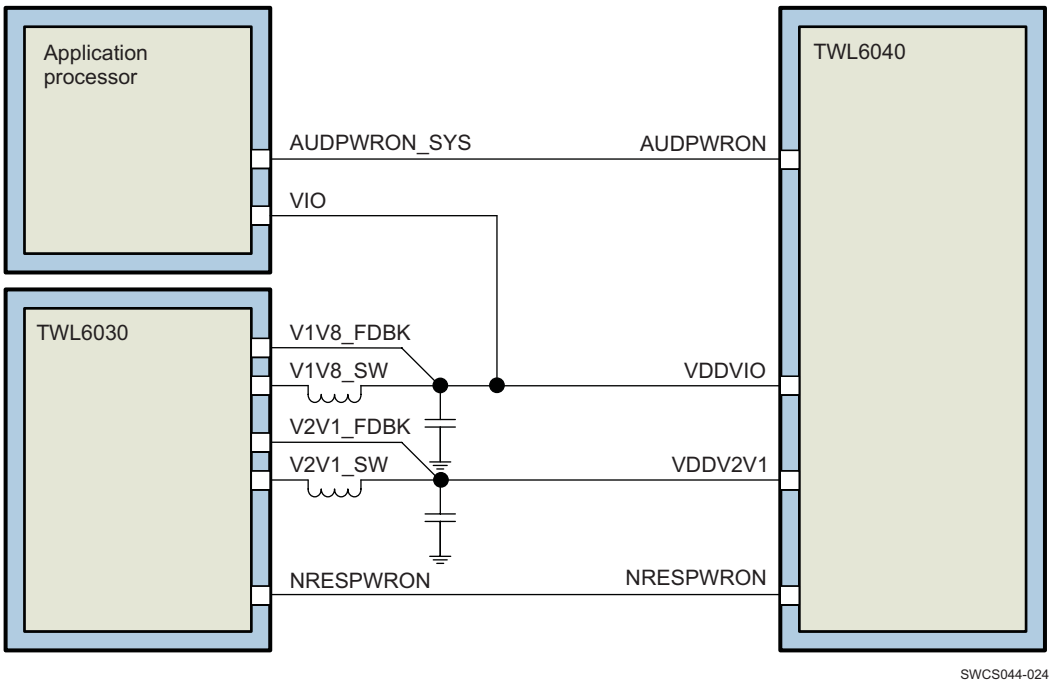


Figure 20. Power-Up and Power-Down Sequences

The NRESPWRON input signal is an active-low reset signal (NRESPWRON) delivered by the TWL6030 at the

end of its own power-on sequence, it is released when all the supply voltage (core and I/Os) are correctly set up. TWL6030 has a VRTC domain powered pulldown on the NRESPWRON signal, ensuring a low-impedance path to ground, even when the VIO supply is off. The TWL6040 uses this signal to reset the register and state-machine running from the I/O supplies, as well as disable the modules directly powered by the VBAT supply.

AUDPWRON is an active-high input signal generated by a GPIO on the application processor side. It triggers the internal power-on and power-off sequences of the TWL6040. The AUDPWRON signal is internally debounced.

Power-Up Sequence

The VIO domain logic and registers are in reset when VIO is high and NRESPWRON is low.

After NRESPWRON goes high, I^2C on the VIO domain, plug detect, and GPO functions are available (deep-sleep mode).

After V2V1 goes high, the hook-detect function is available by I^2C programming (sleep mode).

The power-up sequence is initiated by a low-to-high transition on the AUDPWRON signal. VBAT, VIO, and V2V1 must be within their specified limits when the AUDPWRON transition occurs. The power-up sequence is internally generated by the TWL6040 state-machine and completion of sequence is signaled by the READYINT active-high output-interrupt signal. READYINT signals the application processor that the TWL6040 has completed its power-up sequence and is ready to communicate with the application processor through the I^2C or PDM interface.

Power-Down Sequence

The power-down sequence is initiated by a high-to-low transition of the AUDPWRON signal. The power-down sequence is internally generated by the TWL6040 state-machine.

INTERRUPTS

The TWL6040 drives the NAUDINT line low when an interrupt is internally detected and the host must be notified.

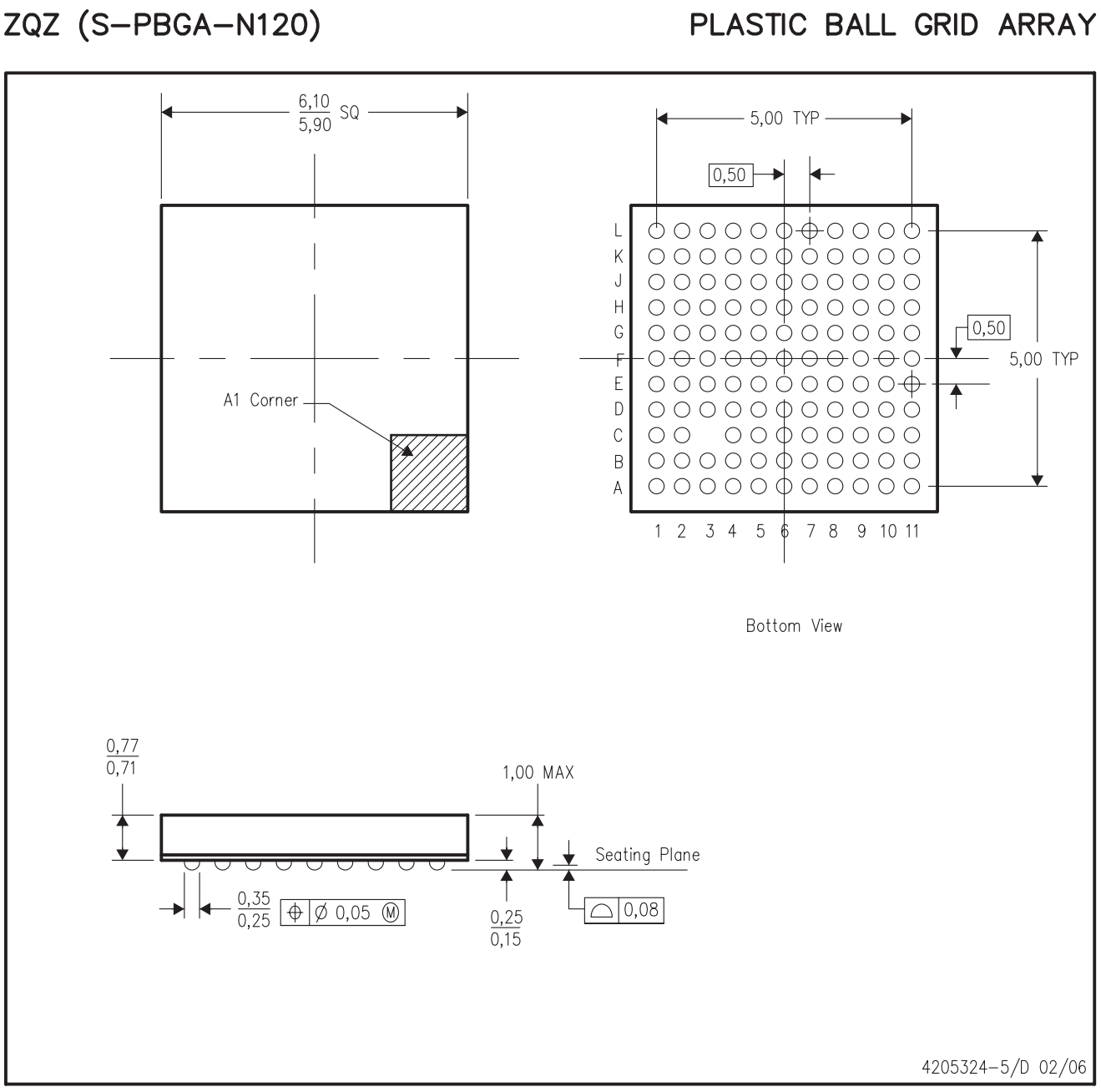
The possible events are:

- THINT: Die temperature overlimit detection
- PLUGINT: Plug insertion detection
- UNPLUGINT: Plug removal detection
- HOOKINT: Hook send/end detection
- HFINT: Left or right hands-free driver overcurrent detection
- VIBINT: Left or right vibrator driver overcurrent detection
- READYINT: Completion of power-up sequence

For each interrupt, an optional mask bit can be set.

PACKAGE CHARACTERISTICS

The package is a ZQZ lead-free 6 × 6 mm^2 MicroStar Junior plastic ball grid array (PBGA) 120ZQZ (PTWL6040A2ZQZ/R) 0.5 mm with 120 physical balls, of which 119 are routable. The mechanical data is shown below.



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This package is lead–free.

SWCS044-026

Figure 21. TWL6040 Mechanical Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TWL6040A2ZQZ	ACTIVE	BGA MICROSTAR JUNIOR	ZQZ	120	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TWL6040A2ZQZR	ACTIVE	BGA MICROSTAR JUNIOR	ZQZ	120	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

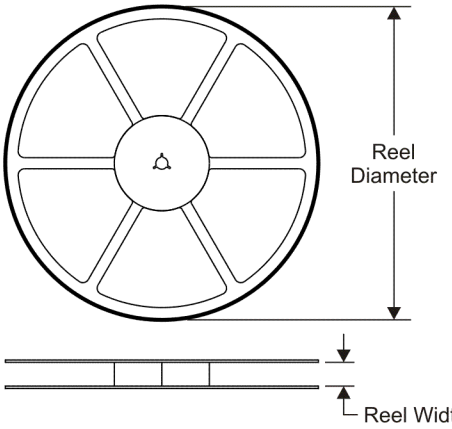
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

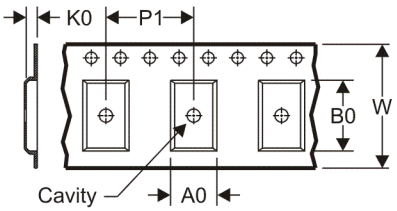
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

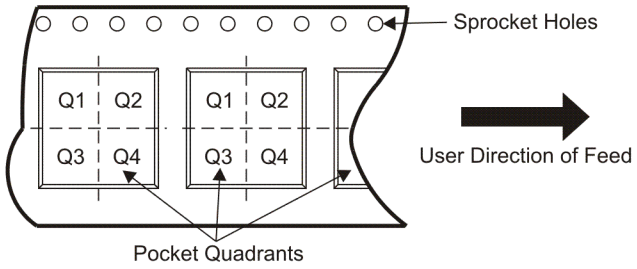


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

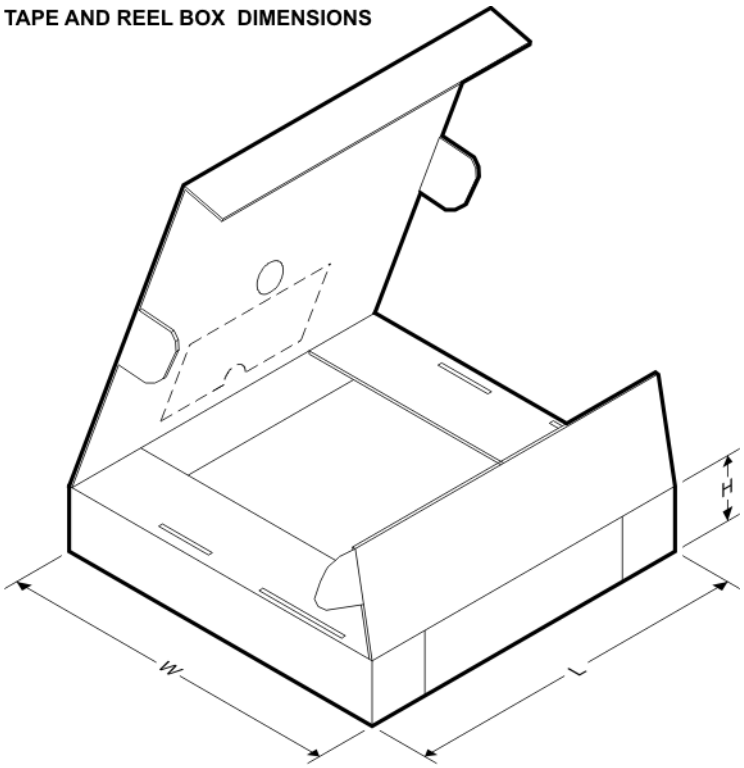
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TWL6040A2ZQZR	BGA MICROSTAR JUNIOR	ZQZ	120	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

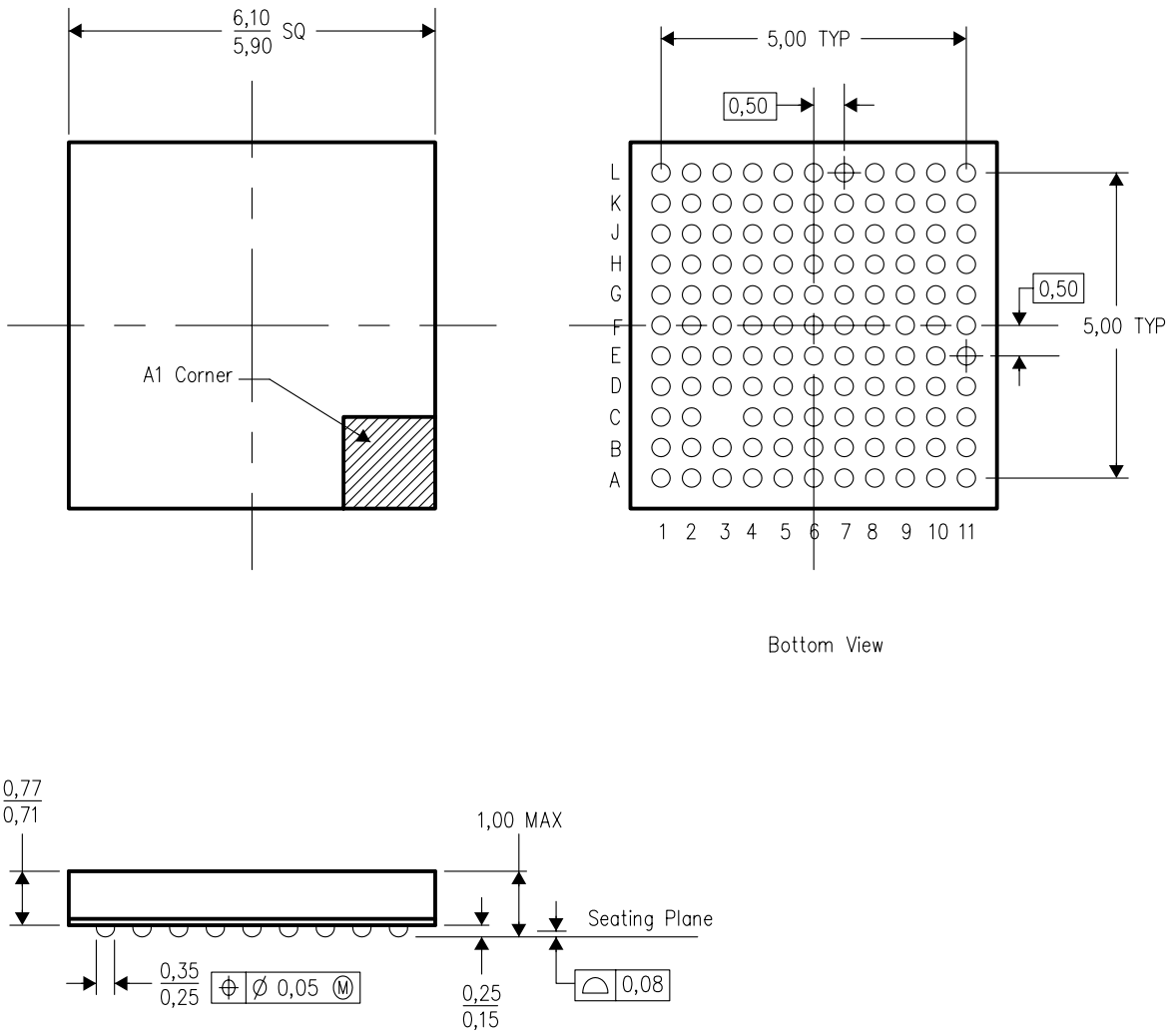
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TWL6040A2ZQZR	BGA MICROSTAR JUNIOR	ZQZ	120	2500	333.2	345.9	31.8

ZQZ (S–PBGA–N120) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This package is lead–free.

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