JL4205A

Multimedia Controller

Revision: 1.4

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0. Revision History

Revision	Description of Changes	Date
1.0	First Formal Release	2007/09/27
1.1	1. Update pin name. 2. Update block diagram. 3. Delete following description in FEATURES paragraph. ➢ Provides lots of GPIOs 4. Add AC Timing Specification.	2007/12/31
1.2	1. Change the video frame rate to “up to VGA@30fps”. 2. Rename pin 35 to USB_REF. 3. Modify block diagram in chapter 3. 4. Delete the CompactFlash Card /ATA Interface paragraph in AC Characteristics, paragraph 6.8. 5. Add Chapter 9 CHIP REVISION HISTORY. 6. Change ordering information of JL4205A to JL4205A-V2.	2008/05/14
1.3	1. Remove following display features in paragraph 2. ● Smaller size TFT-LCD panel with 8-bit CPU interface 2. Remove paragraph 5.4, “DDI (Digital Display Interface) Table".	2008/05/28

1. General Description

JL4205A is a multi-media system on chip (SoC) designed and developed by Jeilin Technology, Taiwan. With LCD of different size, JL4205A can be applied to make digital photo frame. Jeilin Technology will provide complete system design to allow client or distributor enter easier and earlier the digital photo frame market.

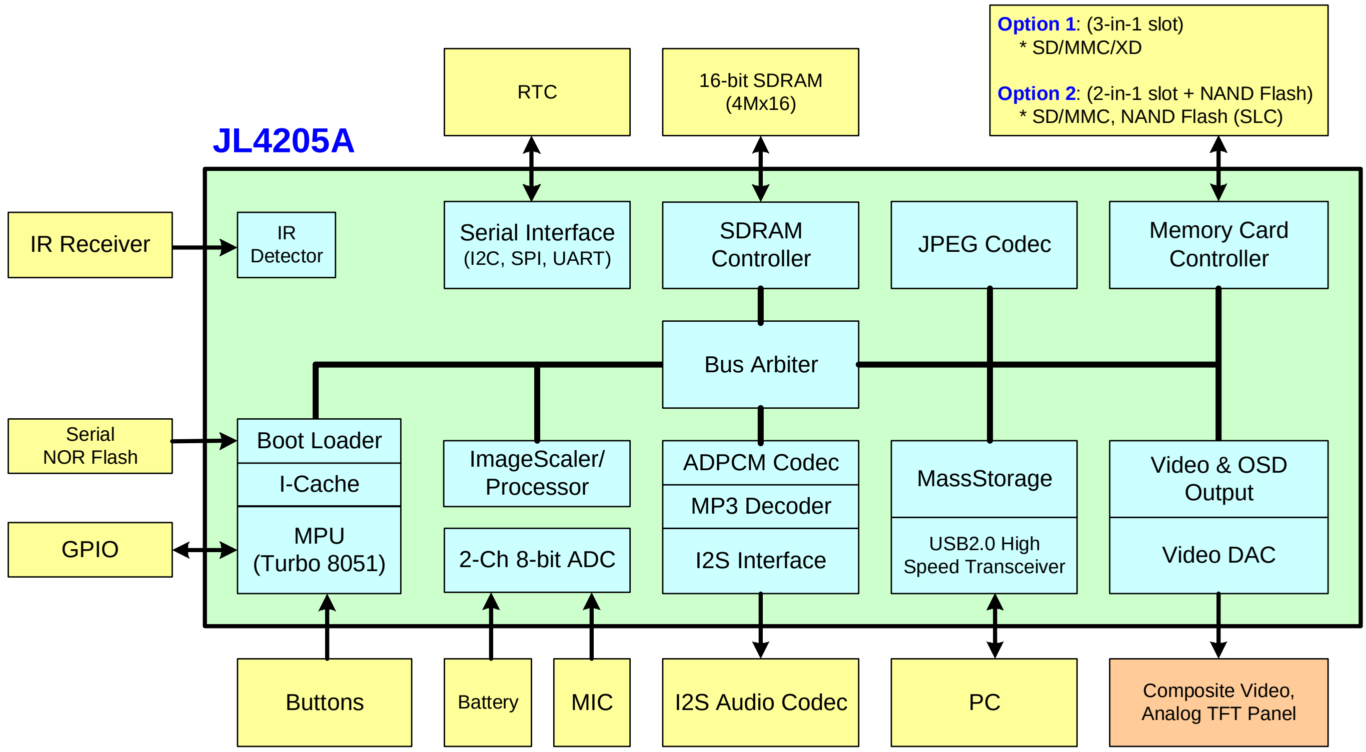
JL4205A digital photo frame can play back photos (JPEG), movie (Motion JPEG), and music (MP3) from memory card or built-in memory. This will allow user to directly view and share photos and listen to music without developing the photos for viewing later. JL4205A digital photo frame has added many functions that traditional photo frame does not have, for example, auto slide browsing, music playing in the background while photo browsing, transition effects while photo browsing, clock, alarm clock, and calendar. All these functions can be achieved without using a computer.

2. Features

- USB Interface
  - High-speed USB 2.0 device function with embedded PHY
  - Supports Mass-Storage Class (MSC)
  - Supports PictBridge interface (direct picture print)
- Storage Media
  - SD/MMC Interface
    - Complies with SD 2.0
    - Complies with MMC 4.0
  - NAND Flash/XD/SmartMedia Interface
- Display Feature
  - Embedded four 10-bit video DACs: one for TV display and three for analog LCD panel.
  - Embedded TV Encoder (NTSC/PAL) to output CVBS (Composite Video).
  - Supports analog RGB TFT-LCD panel
  - Supports 8-bit CCIR601/656 output interfaces
- OSD Feature
  - Font-based OSD
  - Graphic-based OSD
- Audio Feature
  - 8/16-bit PCM, 4-bit IMA-ADPCM audio codec
  - AC97/I^{2}S interface
  - Embedded 2 channels of 8-bit ADC for voice record and battery detect
- MP3 Feature

  - Built-in MP3 decoder engine
  - Supports both ISO 11172-3 and ISO 13818-3 layer III audio decoding
  - Supports 8 KHz, 11.025 KHz, 12 KHz,16 KHz, 22.05 KHz, 24 KHz, 32 KHz, 44.1 KHz, 48 KHz sampling rate
  - Ten-band equalizer with 64 steps for -20 to 20 dB gain.
  - Photo slide show with MP3 background playback.
- JPEG codec
  - Supports photo resolution up to 16,384 x 16,384 pixels
  - High-speed JPEG compression/decompression rate: 27 MPixel/sec
  - Supports non-progressive JPEG
  - Supports baseline JPEG format
  - Supports thumbnail decoding
- Video Playback
  - File Format：Only Support Motion JPEG
  - Audio Signal：PCM Format、ADPCM Format
  - Video Frame Rate：up to VGA@30fps
  - Supports video scaling and Picture-In-Picture functions
- SDRAM interface
  - Supports 16-bit SDRAM up to 8Mx16 bits
- Image Display Functions
  - Preview, Slide Show, Zoom, Pan, Rotate, and so on
  - Image Rotation: 0, 90, 180, or 270 degree in clockwise or counter-clockwise direction
  - Image scale function to fit screen
  - Picture In Picture display
  - Transition Effect in photo playback
- Embedded Turbo 8051
  - Supports ISP Function: It is easy-to-use function to upgrade the system firmware directly from memory cards.
- Provides UART, SPI-master and I^2C-master serial ports
- Package：128-pin LQFP

3. Block Diagram

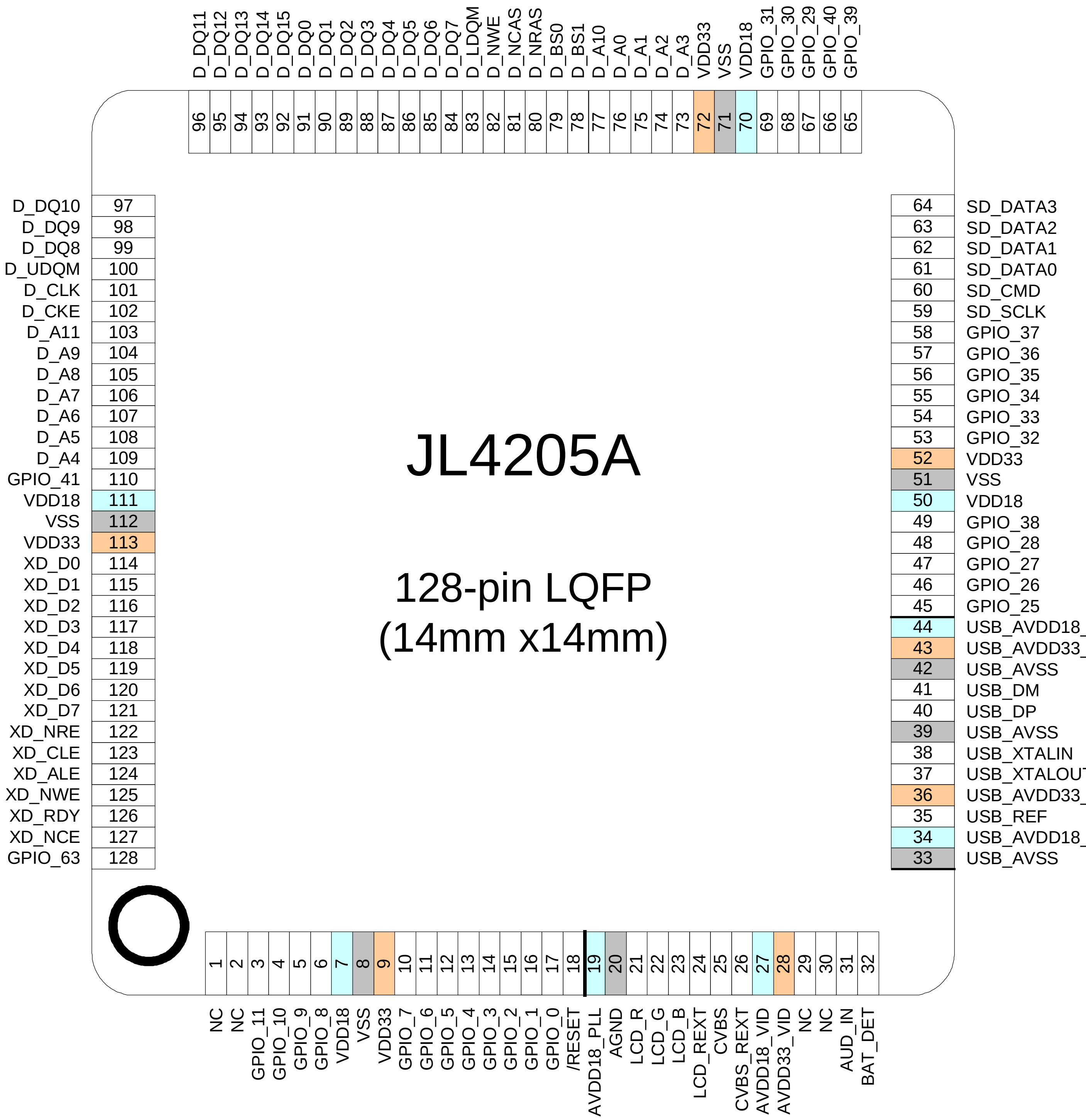


4. Applications

- Digital Photo Frame (DPF)
    - Viewing Photos (JPEG)
    - Viewing Movie (Motion JPEG AVI)
    - Listening to MP3 music
- USB2.0 Card Reader
- DPF with Clock/Calendar

5. Pin Assignment and Pin Description

5.1 Pin Assignment



5.2 Pin Description

Pin#	Pin name	Type	Description	Memo
1	NC		Reserved pin	
2	NC		Reserved pin	
3	GPIO_11	B2	General purpose I/O, bit 11	DDI_11
4	GPIO_10	B2	General purpose I/O, bit 10	DDI_10
5	GPIO_9	B2	General purpose I/O, bit 9	DDI_9
6	GPIO_8	B2	General purpose I/O, bit 8	DDI_8
7	VDD18	P	Core power 1.8V	
8	VSS	G	Ground	
9	VDD33	P	Pad power 3.3V	
10	GPIO_7	B2	General purpose I/O, bit 7	DDI_7
11	GPIO_6	B2	General purpose I/O, bit 6	DDI_6
12	GPIO_5	B2	General purpose I/O, bit 5	DDI_5
13	GPIO_4	B2	General purpose I/O, bit 4	DDI_4
14	GPIO_3	B2	General purpose I/O, bit 3	DDI_3
15	GPIO_2	B4	General purpose I/O, bit 2	DDI_2
16	GPIO_1	B4	General purpose I/O, bit 1	DDI_1
17	GPIO_0	B4	General purpose I/O, bit 0	DDI_0
18	/RESET	B2	Reserved pin, which must be pull-high with a 10K ohms resistor	
19	AVDD18_PLL	P	PLL power 1.8V	
20	AGND	G	Analog ground	
21	LCD_R	A	R channel analog output signal	
22	LCD_G	A	G channel analog output signal	
23	LCD_B	A	B channel analog output signal	
24	LCD_REXT	A	The reference current for the video DAC. This pin should connect a resistor to ground. The output current I =128*1.25/Rext (mA)	
25	CVBS	A	Composite video signal output	
26	CVBS_REXT	A	The reference current for the video DAC. This pin should connect a resistor to ground. The output current I =128*1.25/Rext(mA)	
27	AVDD18_VID	P	Video DAC power 1.8V	
28	AVDD33	P	ADC/DAC power 3.3V	
29	NC	A	Reserved pin	

Pin#	Pin name	Type	Description	Memo
30	NC	A	Reserved pin	
31	AUD_IN	A	Audio signal input	
32	BAT_DET	A	Battery voltage detect input	
33	USB_AVSS	G	USB PHY ground	
34	USB_AVDD18_PLL	P	USB PLL power 1.8V	
35	USB_REF	A	Connect 12.1Kohm (1%) resistor to ground. The purpose of RES is to provide a reference for the current resource of the high-speed driver.	
36	USB_AVDD33_BIAS	P	3.3V power for BIAS	
37	USB_XTALOUT	A	Oscillator output. Connect to a 12Mhz crystal	
38	USB_XTALIN	A	Oscillator input. Connect to a 12Mhz crystal	
39	USB_AVSS	G	USB PHY ground	
40	USB_DP	A	USB D+	
41	USB_DM	A	USB D-	
42	USB_AVSS	G	USB PHY ground	
43	USB_AVDD33_TRV	P	3.3V power for USB transceiver	
44	USB_AVDD18_CDR	P	1.8V power for CDR	
45	GPIO_25	B2	General purpose I/O #25	
46	GPIO_26	B2	General purpose I/O #26	
47	GPIO_27	B2	General purpose I/O #27	
48	GPIO_28	B2	General purpose I/O #28	
49	GPIO_38	B2	General purpose I/O #38	
50	VDD18	P	Core power 1.8V	
51	VSS	G	Ground	
52	VDD33	P	Pad power 3.3V	
53	GPIO_32	B2	General purpose I/O #32	
54	GPIO_33	B2	General purpose I/O #33	
55	GPIO_34	B2	General purpose I/O #34	
56	GPIO_35	B2	General purpose I/O #35	
57	GPIO_36	B2	General purpose I/O #36	
58	GPIO_37	B2	General purpose I/O #37	
59	SD_SCLK	B8	Clock signal for SD/MMC Clock Output	
60	SD_CMD	B4	Command signal for SD/MMC Bus State Output	
61	SD_DATA0	B4	Data bit 0 of SD/MMC	
62	SD_DATA1	B4	Data bit 1 of SD/MMC	

Pin#	Pin name	Type	Description	Memo
63	SD_DATA2	B4	Data bit 2 of SD/MMC	
64	SD_DATA3	B4	Data bit 3 of SD/MMC	
65	GPIO_39	B16	General purpose I/O #39	
66	GPIO_40	B2	General purpose I/O #40	
67	GPIO_29	B2	General purpose I/O #29	
68	GPIO_30	B2	General purpose I/O #30	
69	GPIO_31	B2	General purpose I/O #31	
70	VDD18	P	Core power 1.8V	
71	VSS	G	Ground	
72	VDD33	P	Pad power 3.3V	
73	D_A3	O8	SDRAM address bus 3, which must be pull-high with a 10K ohm resistor for normal operation	
74	D_A2	O8	SDRAM address bus 2, which must be pull-high with a 10K ohm resistor for normal operation	
75	D_A1	O8	SDRAM address bus 1	
76	D_A0	O8	SDRAM address bus 0	* Note 1
77	D_A10	O8	SDRAM address bus 10	
78	D_BS1	O8	SDRAM bank address 1	
79	D_BS0	O8	SDRAM bank address 0	
80	D_NRAS	O8	SDRAM raw address strobe output	
81	D_NCAS	O8	SDRAM column address strobe output	
82	D_NWE	O8	SDRAM write strobe	
83	D_LDQM	O8	SDRAM low byte data write mask	
84	D_DQ7	B8	SDRAM data bus 7	
85	D_DQ6	B8	SDRAM data bus 6	
86	D_DQ5	B8	SDRAM data bus 5	
87	D_DQ4	B8	SDRAM data bus 4	
88	D_DQ3	B8	SDRAM data bus 3	
89	D_DQ2	B8	SDRAM data bus 2	
90	D_DQ1	B8	SDRAM data bus 1	
91	D_DQ0	B8	SDRAM data bus 0	
92	D_DQ15	B8	SDRAM data bus 15	
93	D_DQ14	B8	SDRAM data bus 14	
94	D_DQ13	B8	SDRAM data bus 13	
95	D_DQ12	B8	SDRAM data bus 12	

Pin#	Pin name	Type	Description	Memo
96	D_DQ11	B8	SDRAM data bus 11	
97	D_DQ10	B8	SDRAM data bus 10	
98	D_DQ9	B8	SDRAM data bus 9	
99	D_DQ8	B8	SDRAM data bus 8	
100	D_UDQM	O8	SDRAM high byte data write mask	
101	D_CLK	O8	SDRAM clock	
102	D_CKE	O8	SDRAM clock enable	
103	D_A11	O8	SDRAM address bus 11	
104	D_A9	O8	SDRAM address bus 9	
105	D_A8	O8	SDRAM address bus 8	
106	D_A7	O8	SDRAM address bus 7	
107	D_A6	O8	SDRAM address bus 6	
108	D_A5	O8	SDRAM address bus 5	
109	D_A4	O8	SDRAM address bus 4	
110	GPIO_41	B2	General purpose I/O #41	
111	VDD18	P	Core power 1.8V	
112	VSS	G	Ground	
113	VDD33	P	Pad power 3.3V	
114	XD_D0	B4	Data bit 0 of XD	
115	XD_D1	B4	Data bit 1 of XD	
116	XD_D2	B4	Data bit 2 of XD	
117	XD_D3	B4	Data bit 3 of XD	
118	XD_D4	B4	Data bit 4 of XD	
119	XD_D5	B4	Data bit 5 of XD	
120	XD_D6	B4	Data bit 6 of XD	
121	XD_D7	B4	Data bit 7 of XD	
122	XD_NRE	O4	Read strobe for XD	
123	XD_CLE	O4	Command latch enable for XD	
124	XD_ALE	O4	Address latch enable for XD	
125	XD_NWE	O4	Write strobe for XD	
126	XD_RDY	O4	Ready signal for XD	
127	XD_NCE	O4	Chip enable signal for XD	
128	GPIO_63	B16	General purpose I/O #63	

NOTE:

*1: Pull up/down these two pins with 10K ohm resistor to select system booting method.

Booting Mode	Function
0	Booting from iROM
1	Booting from Serial NOR Flash

*2: All digital input pin can take 5V tolerance

Type	Description
P	Power pin
G	Ground pin
A	Analog pin
I	3.3V CMOS input pin
O4	3.3V CMOS output pin with 4mA driving ability
O8	3.3V CMOS output pin with 8mA driving ability
O24	3.3V CMOS output pin with 24mA driving ability
B2	3.3V CMOS bi-direction pin with 2mA driving ability
B4	3.3V CMOS bi-direction pin with 4mA driving ability
B8	3.3V CMOS bi-direction pin with 8mA driving ability
B16	3.3V CMOS bi-direction pin with 16mA driving ability
OD	3.3V CMOS open drain output pin

5.3 GPIO Mux Table:

NOTE: Each GPIO pin has its own function select registers, Alt[2:1], firmware can configure each GPIO pin to different function individually.

Alt[2:1]= 00		Alt[2:1]= 01		Alt[2:1]= 10	
GPIO_0	B	DDI_0	O	-	
GPIO_1	B	DDI_1	O	-	
GPIO_2	B	DDI_2	O	-	
GPIO_3	B	DDI_3	O	-	
GPIO_4	B	DDI_4	O	-	
GPIO_5	B	DDI_5	O	-	
GPIO_6	B	DDI_6	O	-	
GPIO_7	B	DDI_7	O	-	
GPIO_8	B	DDI_8	O	-	
GPIO_9	B	DDI_9	O	-	
GPIO_10	B	DDI_10	O	-	
GPIO_11	B	DDI_11	O	CCIR601_In_CLK	I
GPIO_25	B	I2S_PWDN		AC_Link_nReset	O
GPIO_26	B	I2S_WS	O	AC_Link_Sync	O
GPIO_27	B	I2S_BCK	O	AC_Link_BClk	I
GPIO_28	B	I2S_DATA_OUT	O	AC_Link_SDataOut	O
GPIO_29	B	SCL	OD	-	
GPIO_30	B	SDA	OD	-	
GPIO_31	B	AC_Link_SDataIn	I	PG1_Out_1	O
GPIO_32	B	IR_In_0	I	-	
GPIO_33	B	SPI_nCS_1	O	PWM Signal Output	O
GPIO_34	B	SPI_nCS_0	O	ROM_NCS	O
GPIO_35	B	SPI_SCK	O	-	
GPIO_36	B	SPI_DO	O	UART_TX	O
GPIO_37	B	SPI_DI	I	UART_RX	I
GPIO_38	B	AC_Link_SDataIn	I	PG1_Out_1	O
GPIO_39	B	NF_nCE1	O	PLL1_Out	O
GPIO_40	B	NF_RDY1	I	PWM Signal Output	O
GPIO_63	B	PG1_Out_1	O	-	

6. AC Characteristics

6.1 Serial Peripheral Interface

- SPI mode 0

Symbol	Parameter	Min.	Max.	Unit
tClSh	-CS low to SCK high	-	230	ns
tShCh	SCK high to –CS high	-	125	ns
tCRT	Clock Rise Time	0.1	-	V/ns
tCFT	Clock Fall Time	0.1	-	V/ns
tSU:DAT	Data in Setup Time	10	-	ns
tHD:DAT	Data in Hold Time	5	-	ns
tV	Output Valid	-	5	ns
tHO	Output Hold Time	-	5	ns
tWH	SCK High Time	-	35	ns
tWL	SCK Low Time	-	35	ns

* The definition of signal timing is defined by SPI_SCK=13.5MHz.

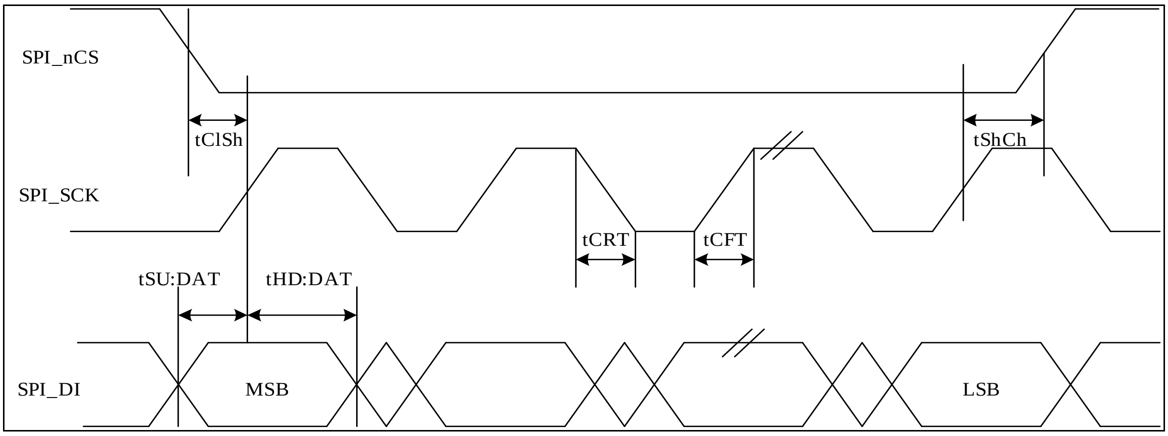


Figure 6.1: Input Timing Diagram of SPI

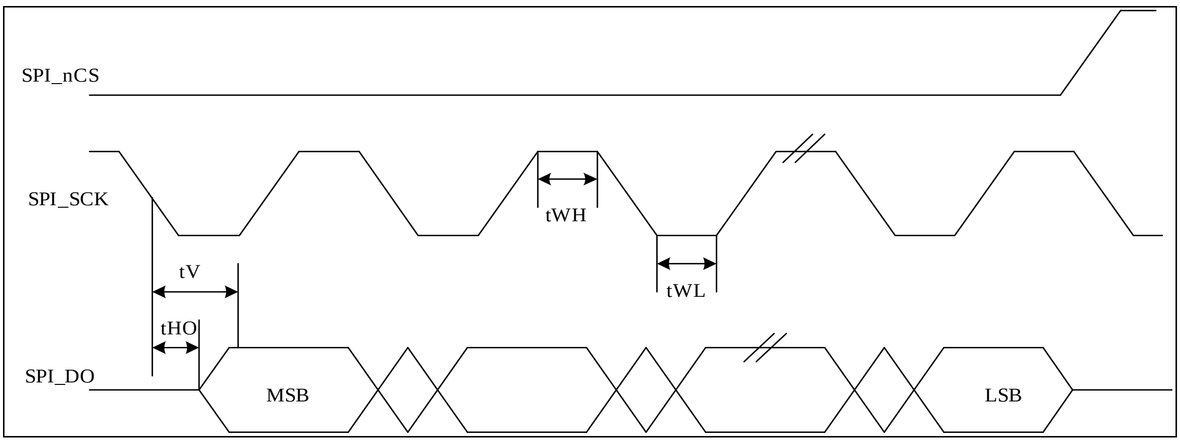


Figure 6.2: Output Timing Diagram of SPI

6.2 Inter-IC Sound Interface

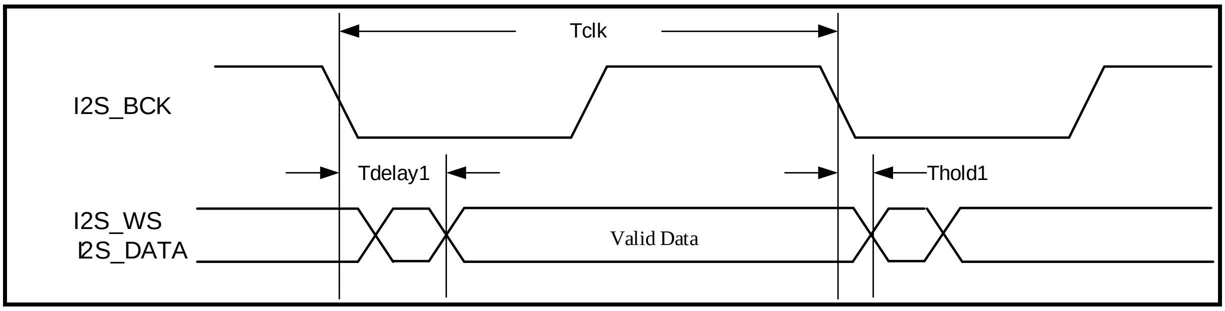


Figure 6.3: Timing Diagram of I2S

Symbol	Parameter	Min.	Max.	Unit
Tclk	Bit clock frequency	20.84	125	us
Tdelay1	output delay from CLK rising edge	0	3	ns
Thold1	output data hold time from CLK rising edge	0	3	ns

6.3 I2C Interface

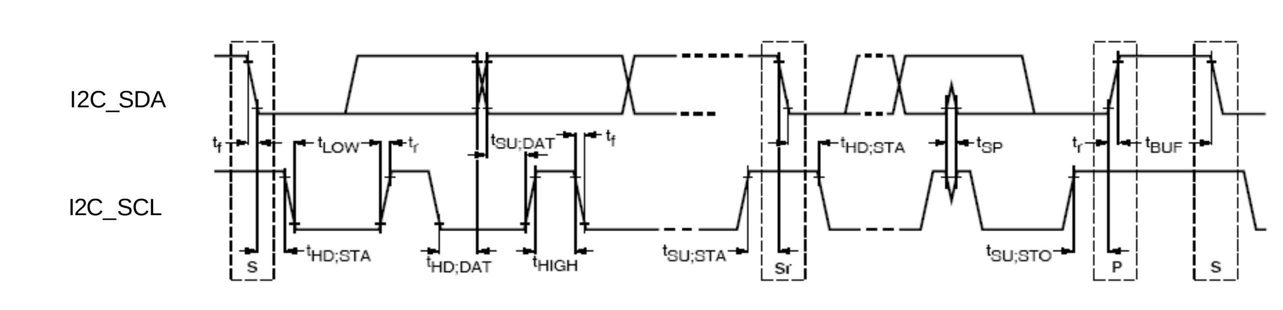


Figure 6.4: Timing Diagram of I2C-bus

Symbol	Parameter	Standard-Mode		Fast- Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	KHz
$t_{HD; STA}$	Hold time (repeated) START condition After this period, the first clock pulse is generated	4.0	-	0.6	-	us
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	us
$t_{SU; STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	us
$t_{HD; DAT}$	Data hold time for I2C bus devices	0	3.45	0	0.9	us
$t_{SU; DAT}$	Data set-up time	250	-	100	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	$20+0.1C_b$	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	$20+0.1C_b$	300	ns
$t_{SU; DAT}$	Set-up time for STOP condition	4.0	-	0.6	-	us
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	us
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes

1. C_b = total capacitance of one bus line in PF.
2. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

6.4 SDRAM Interface

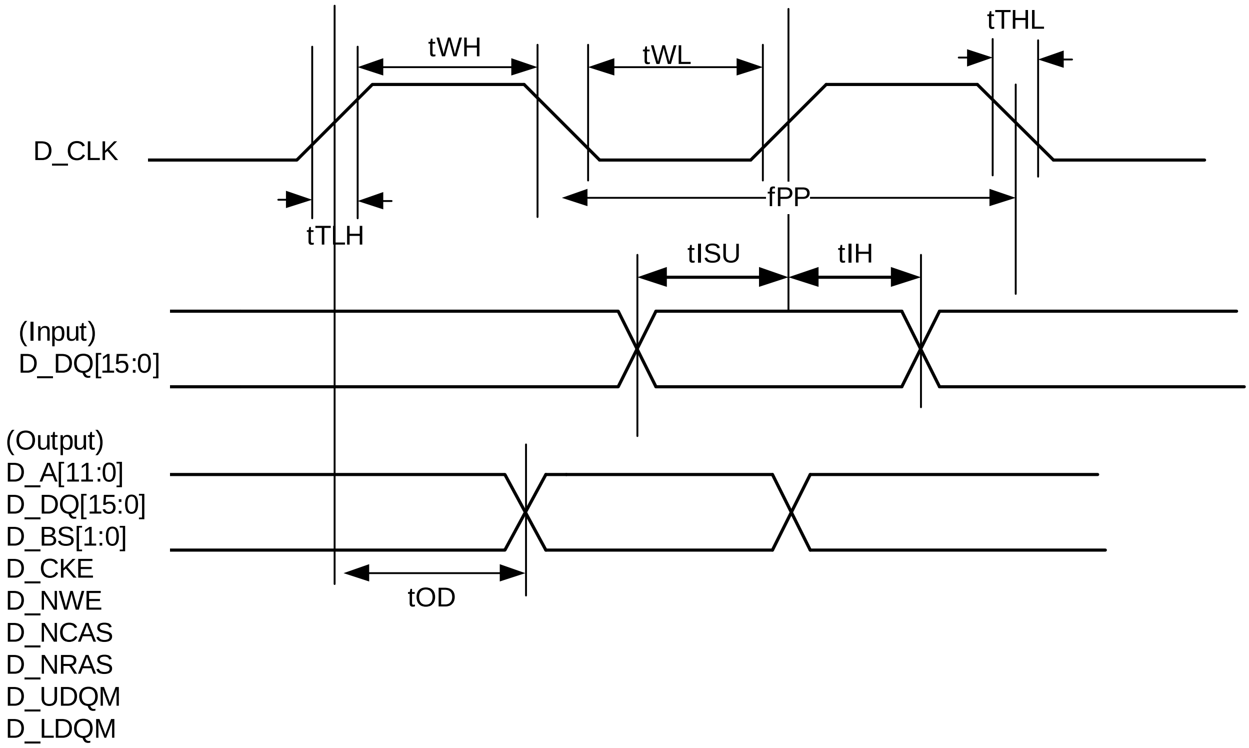


Figure 6.5: Timing Diagram of SDRAM Interface

Symbol	Parameter	Min.	Max.	Unit
fPP	Clock frequency	-	108	MHz
tWL	Clock low time	4.62	-	ns
tWH	Clock High time	4.62	-	ns
tTLH	Clock rise time		2	ns
tTHL	Cock fall time		2	ns
tISU	Input set-up time	2		ns
tIH	Input hold time	1		ns
tOD	Output delay time		3.5	ns

6.5 Secure Digital/ MultiMedia Card Interface

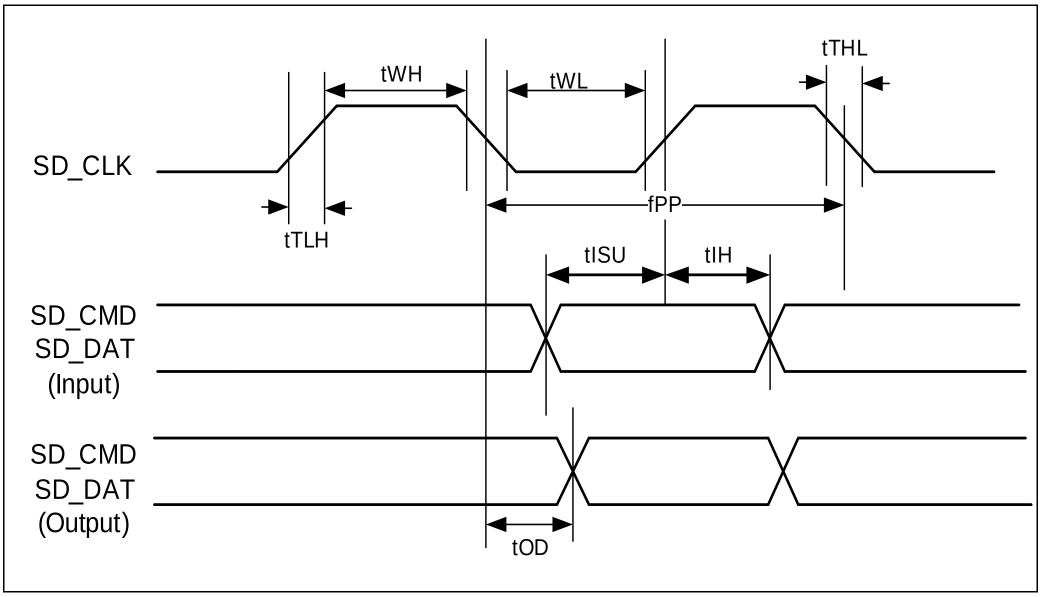


Figure 6.11: Timing Diagram of Data Input/Output Referenced to Clock

Symbol	Parameter	Min.	Max.	Unit
fPP	Clock frequency	-	36	MHz
tWL	Clock low time	20	-	ns
tWH	Clock High time	7	-	ns
tTLH	Clock rise time		3	ns
tTHL	Cock fall time		3	ns
tISU	Input setup time	10		ns
tIH	Input hold time	5		ns
tOD	Output delay time		3	ns

* The definition of signal timing is defined by SD_CLK=36MHz.

6.6 XD / NAND Flash Interface

Symbol	Parameter	Min.	Max.	Unit
tCLhWl	CLE high to –WE low	27	-	ns
tWhCLl	-WE high to CLE low	55	-	ns
tClWl	-CE low to –WE low	27	-	ns
tWhCh	-WE high to –CE high	55	-	ns
tWP	-WE pulse width	55	-	ns
tALhWl	ALE high to –WE low	27	-	ns
tWhALl	-WE high to ALE low	80	-	ns
tDS	Data setup time	10	-	ns
tDH	Data hold time	5	-	ns
tWC	Write cycle time	135	-	ns
tWH	-WE high hold time	80	-	ns
tRR	Ready to –RE Low	70	-	ns
tRP	Read pulse width	55	-	ns
tRC	Read cycle time	135	-	ns
tOD	-WE output delay time	-	0	ns
tREH	-RE high hold time	80	-	ns

- The definition of signal timing is defined by Peri_clk=36MHz.
- The definition of read/write pulse width is defined with 2*Peri_clk, this timing can be redefined by setting register.
- The definition of read/write high hold time is defined with 3*Peri_clk, this timing can be redefined by setting register.

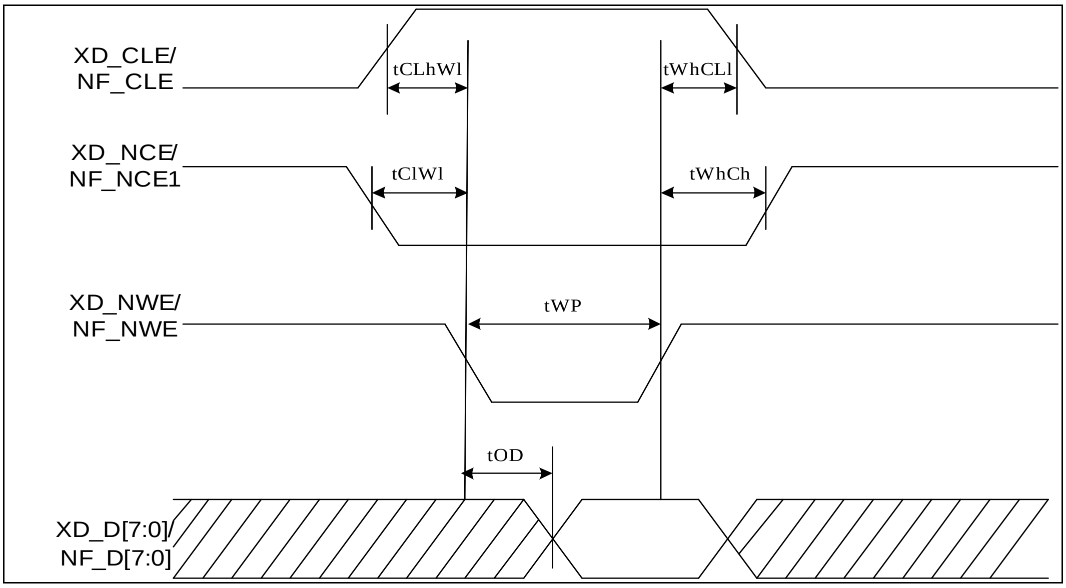


Figure 6.12: Command output Timing

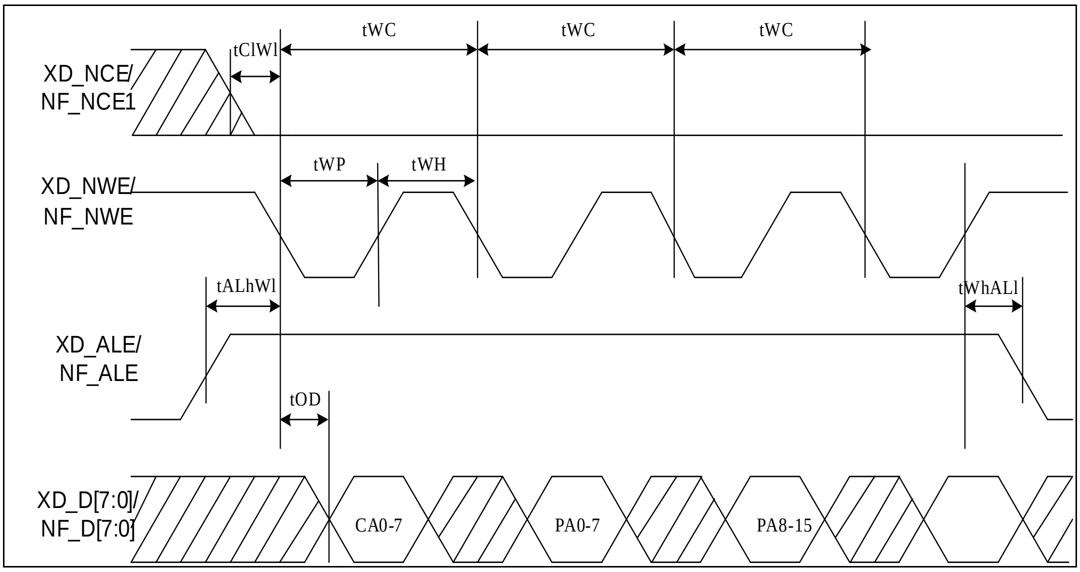


Figure 6.13: Address output Timing

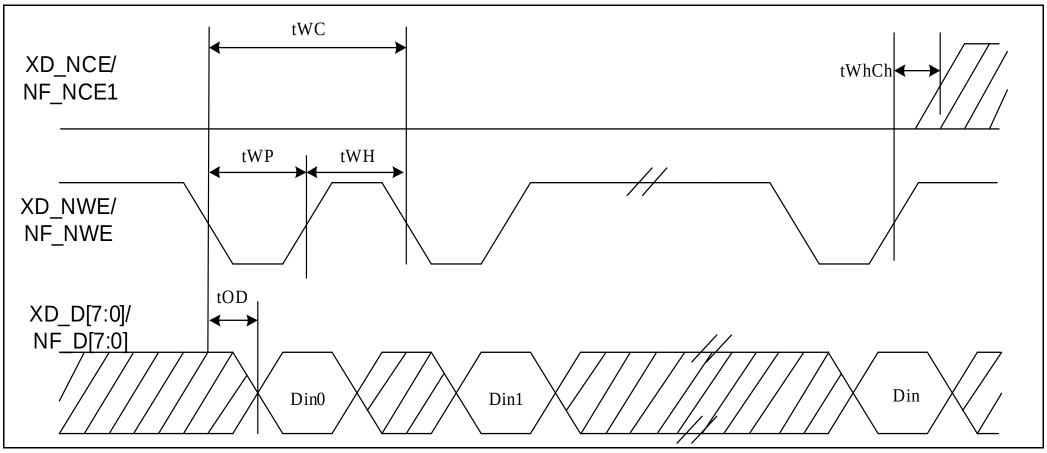


Figure 6.14: Data output Timing

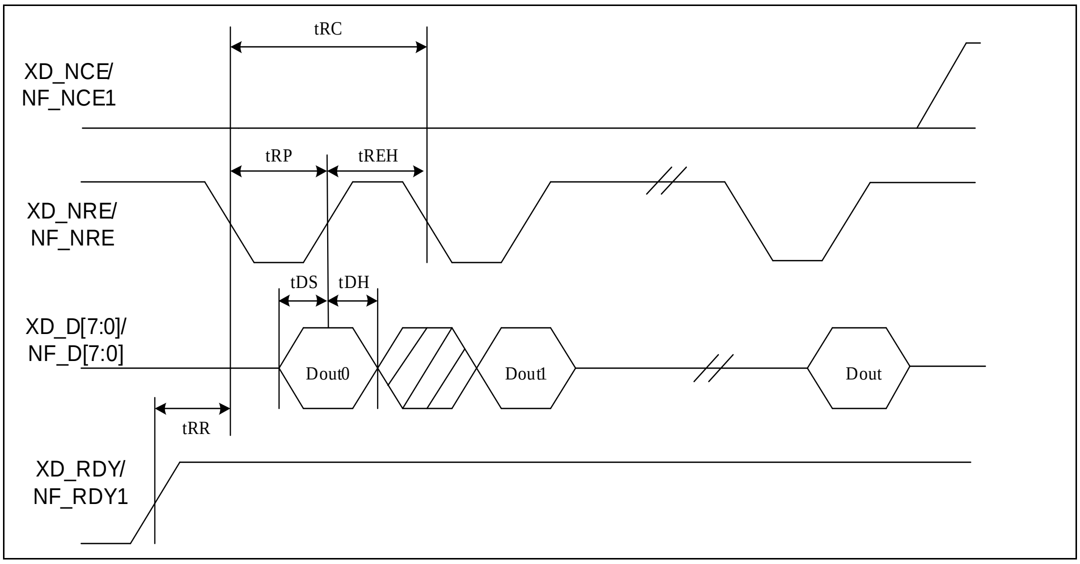


Figure 6.15: Data Input Timing

6.7 Digital Display Interface

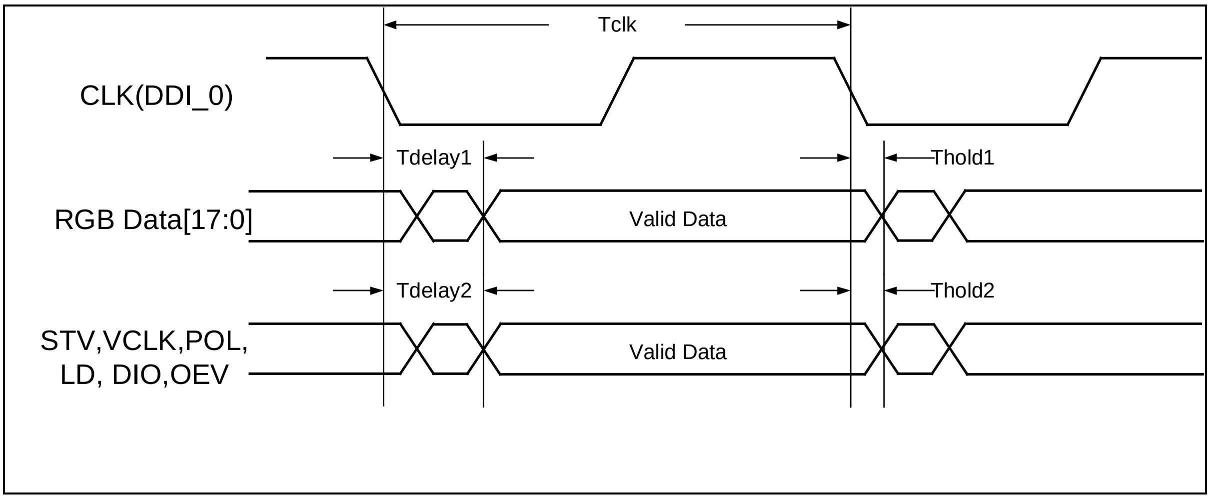


Figure 6.27: Timing Diagram of Digital Display Interface

Symbol	Parameter	Min.	Max.	Unit
Fclk	Pixel clock frequency (Fclk = 1/Tclk)	25	32	MHz
Tdelay1	RGB Data output delay from CLK rising edge	0	5	ns
Thold1	RGB Data output data hold time from CLK rising edge	0	5	ns
Tdelay2	STV, VCLK, POL, LD, DIO, OEV output delay from CLK rising edge	0	3	ns
Thold2	STV, VCLK, POL, LD, DIO, OEV output data hold time from CLK rising edge	0	3	ns

7. Electrical Characteristic

- Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply (3.3V)	-0.3 to 3.6	V
V_{CC1}	Power Supply (1.8V)	-0.3 to 1.98	V
V_{IN}	Input Voltage	-0.3 to V_{CC}+0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{CC}+0.3	V
T_{STG}	Storage Temperature	-55 to 150	℃

- Recommended Operation Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply (3.3V)	3.0	3.3	3.6	V
V_{CC1}	Power Supply (1.8V)	1.62	1.8	1.98	V
T_{OPR}	Operating Temperature	0	25	70	℃

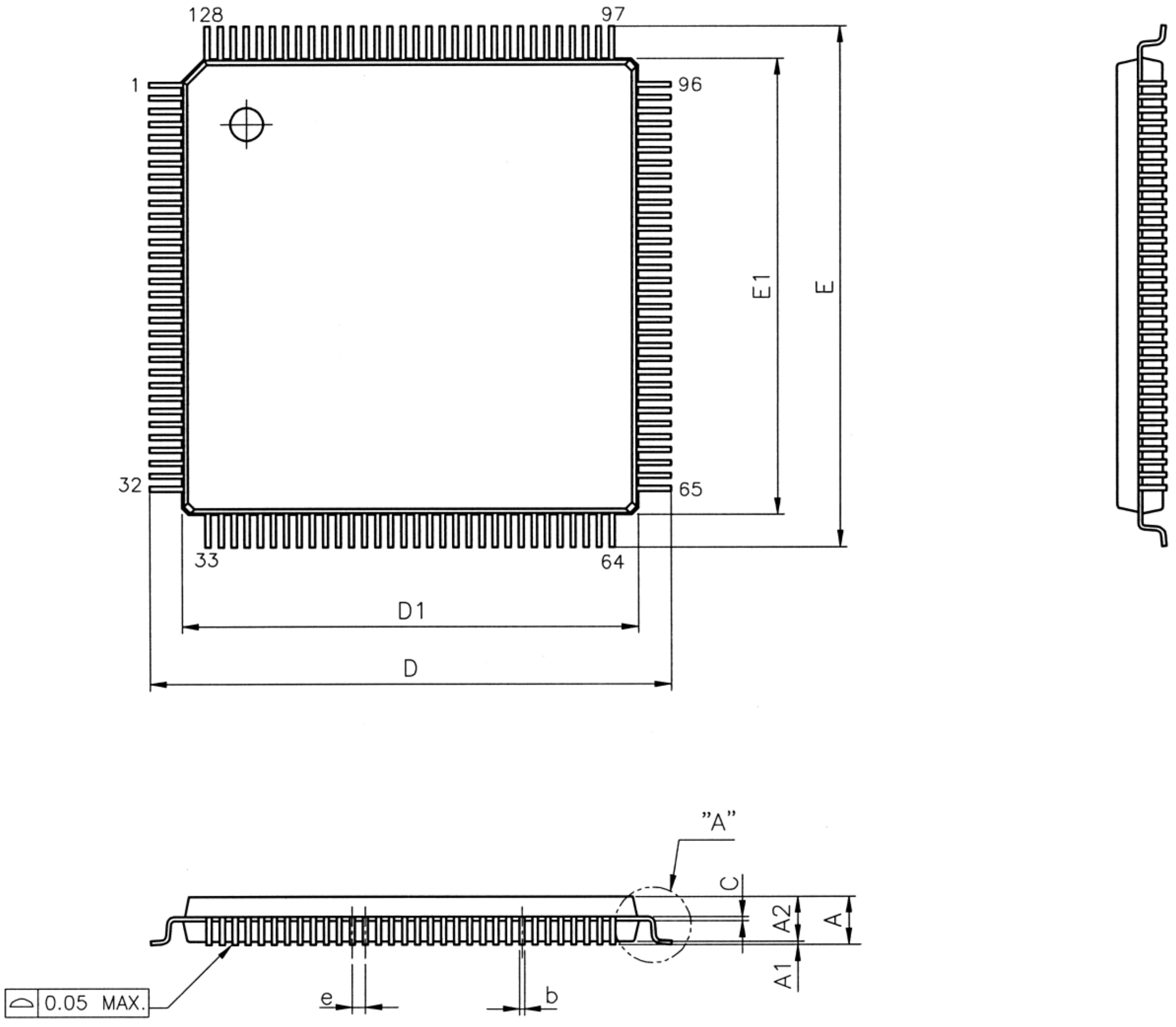
- DC Electrical Characteristics for 3.3 volts operation

(Under Recommended Operating Conditions and V_{CC} = 3.0V ~ 3.6V, Tj = 0℃ to + 70℃)

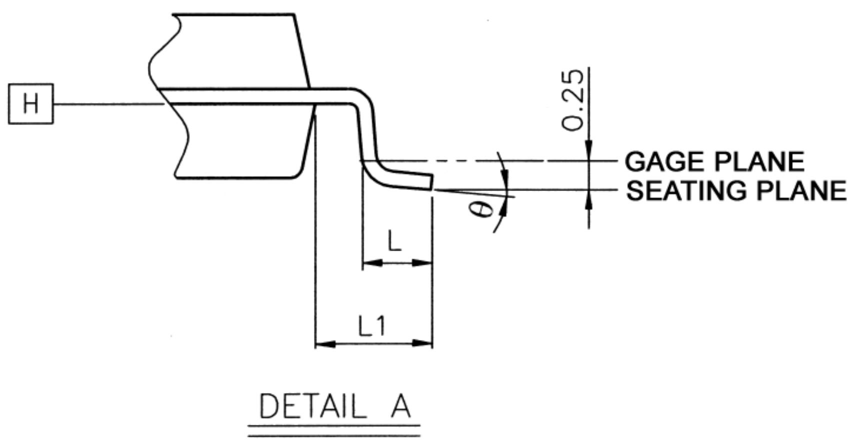
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		Vcc+0.3	V
V_{T-}	Schmitt Input Low Voltage		-0.3		0.8	V
V_{T+}	Schmitt Input High Voltage		2.0		Vcc+0.3	V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V

8. Package Outline and Dimension

- Package Outline (128-pin LQFP)



- Package Outline (128-pin LQFP) – continued



- Dimension (128-pin LQFP)

Dimension	Min	Nom	Max
A	-	-	1.60
A1	0..05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
c	0.09	-	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Unit: mm

REF: Reference

BSC: Basic Spacing between Centers (integrated circuit package dimension)

9. Chip Revision History

Revision	Description of Changes	Date
JL4205A	First Announce	2007/3/20
JL4205A-V2	● Correct core voltage to 1.8 volts. ● Fix some bugs in MP3 block. ● Modify the function of internal pattern generator to control backlight brightness of LCD panel via GPIO_33 (pin 54).	2008/2/15

10. Ordering Information

Part Number	Package	Status	Note
JL4205A-V2	128-pin LQFP	Available	N/C

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