Power Management and USB Single Chip

Check for Samples: TPS65921

FEATURES

- **3 Step-Down Converters:**
  - **Up to 1.2 A of output current for VDD1**
    - **TPS65921B supports VDD1 up to 1.2 A**
    - **TPS65921B1 supports VDD1 up to 1.4 A (necessary for 1-GHz operation)**
  - **SmartReflex™ dynamic voltage management**
  - **3.2 MHz fixed frequency operation**
  - **V_{IN} range from 2.7 to 4.5 V**
  - **Typical 30 µA quiescent per converter**
- **4 general-purpose configurable LDOs:**
  - **Dynamic voltage scaling**
  - **220 mA maximum current for one LDO**
  - **V_{IN} range from 2.7 to 4.5 V**
  - **2 LDOs with low noise and high PSRR**
- **RTC with alarm wake up mechanism**
- **Clock management**
  - **32-kHz crystal oscillator**
  - **Clock slicer for 26, 19.2, and 38.4 MHz**
  - **HF clock output buffer**
- **USB:**
  - **USB HS 2.0 transceiver**
  - **USB 1.3 OTG-compliant**
  - **12-bit ULPI 1.1 interface**
  - **USB power supply (5-V CP for VBUS)**
- **Control**
  - **High-speed I^2C™ interface**
  - **All resource configurable by I^2C**
- **Keypad interface up to 8 × 8**
- **10-bit A/D converter**
- **Hot-die, thermal shutdown protection**
- **µ*BGA 120 balls ZQZ**

APPLICATIONS

- **Mobile phones and smart phones**
- **MP3 players**
- **Handheld devices**
- **E-Books**
- **OMAP™ and low power DSP supply**

DESCRIPTION

The TPS65921 device is a highly integrated power-management circuit (IC) that supports the power and peripheral requirements of the OMAP application processors. The device contains power management, a universal serial bus (USB) high-speed (HS) transceiver, an analog-to-digital converter (ADC), a real-time clock (RTC), a keypad interface, and an embedded power control (EPC). The power portion of the device contains three buck converters, two controllable by a dedicated SmartReflex™ class-3 interface, multiple low-dropout (LDO) regulators, an EPC to manage the power-sequencing requirements of OMAP, and an RTC module. The USB module provides a HS 2.0 transceiver suitable for direct connection to the OMAP universal transceiver macrocell interface (UTMI) + low pin interface (ULPI) with an integrated charge pump (CP).

The device also provides auxiliary modules: ADC, keypad interface, and general-purpose inputs/outputs (GPIOs) muxed with the JTAG functions. The keypad interface implements a built-in scanning algorithm to decode hardware-based key presses and to reduce software use, with multiple additional GPIOs that can be used as interrupts when they are configured as inputs.

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Main battery supply voltage(2)		0.0		5.0	V
Voltage on any input(3)	Where supply represents the voltage applied to the power supply pin associated with the input(4)	–0.3		1.0 × Supply + 0.3	V
VBUS input		–0.3		7	V
Storage temperature range		–55		125	°C
Operating ambient temperature (T_A)		–40		85	°C
Operating junction temperature (T_J)	Absolute maximum rating	–40		125	°C
Operating junction temperature (T_J)	For parametric compliance	–40		150	°C
Ambient temperature for parametric compliance	With maximum 125°C as junction temperature (T_J)	–40		85	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
(2) The product will have negligible reliability impact if voltage spikes of 5.2 V occur for a total (cumulative over lifetime) duration of 10 milliseconds.
(3) Excepts VBAT input pads and VBUS pad.
(4) Supply equals the reference level of each pin.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Power and USB Path					
VBAT/VBAT.USB main battery supply voltage and		2.7	3.6	4.5	V
VBUS		0		7	V
HFCLKIN Input Clock					
Frequency $1/t_{C(HFCLKIN)}$		19.2, 26 or 38.4			MHz
Pulse duration, HFCLKIN low or high (BP)		0.45 × $t_{C(HFCLKIN)}$		0.55 × $t_{C(HFCLKIN)}$	ns
HFCLKIN stability		–150		150	ppm
Rise time of HFCLKIN (BP)		0		5	ns
Fall time of HFCLKIN (BP)		0		5	ns
Input dynamic range	LP/HP (sine wave)	0.3	0.7	1.45	Vpp
	BP/PD (square wave)	0		1.85(1)	Vpp
Harmonic content of input signal (with 0.7-V_{PP} amplitude): Second component - LP/HP (sine wave)				–25	dBc
V_{IH} voltage input high(1)	BP (square mode)	0.65 × IO.1P8			V
V_{IL} voltage input low(1)	BP (square mode)			0.35 × IO.1P8	V
Crystal Oscillator					
Parallel resonance crystal frequency $1/t_{C(32KHZ)}$			32.768		kHz
Input voltage, Vin (normal mode)		1.0	1.3	1.55	V
Crystal tolerance at room temperature, 25°C		–30		30	ppm
Crystal tolerance versus temperature range (–40°C to 85°C)		–200		200	ppm
Crystal quality factor		13k		54k	
Maximum drive power				1	µW
Operating drive level				0.5	µW

(1) Bypass input maximum voltage is the same as the maximum voltage provided for the I/O interface (IO.1P8V).

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RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

32KXIN 32KXOUT duty cycle	Crystal	40%		60%	
	Square wave	45%		55%	
32-kHz clock rise/fall time	Square wave with capacitive load equivalent to 30 pF			0.1 × $t_{C(32KHZ)}$	µs
V_{IH} voltage input high	Square wave in bypass mode(1)	0.65 × VBRTC			V
V_{IL} voltage input low	Square wave in bypass mode(1)			0.35 × VBRTC	V
DCDC Converters and LDOs					
VDD1.IN, VDD2.IN, VDD3.IN input voltage range for step-down converter VDD1, VDD2, VIO		2.7	3.6	4.5	V
VMMC1.IN input voltage range for LDO VMMC1		Maximum (2.7, output voltage selected + 250 mV)	3.6	4.5	V
VDAC.IN input voltage range for LDO VDAC		2.7	3.6	4.5	V
VAUX12S.IN input voltage range for LDO VAUX2		Maximum (2.7, output voltage selected + 250 mV)	3.6	4.5	V
VINT.IN input voltage range for LDO VINTANA1, VINTANA2, VINTDIG and VRTC		Maximum (2.7, output voltage selected + 200 mV)	3.6	4.5	V
VPLLA3R.IN input voltage range for LDO VPLL1		2.7	3.6	4.5	V
VDD1.OUT ouput voltage range for VDD1 step-down converter		0.6		1.45	V
VDD2.OUT ouput voltage range for VDD2 step-down converter		0.6		1.5	V
VIO.OUT ouput voltage range for VIO step-down converter			1.8/1.85		V
VMMC1.OUT output voltage range for LDO VMMC1		1.85		3.15	V
VDAC.OUT output voltage range for LDO VDAC		1.2		1.8	V
VAUX2.OUT output voltage range for LDO VAUX2		1.3		2.8	V
VPLL1.OUT output voltage range for LDO VPLL1		1.0		1.8	V
VINTANA1.OUT output voltage for LDO VINTANA1			1.5		V
VINTANA2.OUT output voltage for LDO VINTANA2			2.5/2.75		V
VINTUSB1P5V.OUT output voltage for LDO VINTUSB1P5		1.35	1.5	1.65	V
VINTUSB1P8V.OUT output voltage for LDO VINTUSB1P8		1.62	1.8	1.98	V
VUSB3P1V.OUT output voltage for LDO VUSB3P1			3.1		V
VINTDIG.OUT output voltage range for LDO VINTDIG		1.35	1.5	1.65	V
VRTC.OUT output voltage range	Normal mode	1.45	1.5	1.55	V
	Backup mode	1.0	1.3	1.55	V
External Components					
Crystal: Nominal load cap on each oscillator input CXIN and CXOUT (2)		9	10	12.5	pF
Crystal ESR (3)				90	kΩ
Crystal shunt capacitance, C_O				1	pF
External coil for VDD1	Value	0.7	1	1.3	µH
	DCR			0.1	Ω
	Saturation current for TPS65921B	1.8			A
	Saturation current for TPS65921B1	2.1			A

(2) Nominal load capacitor on each oscillator input defined as CXIN = CXOUT = Cosc × 2 – (Cint + Cpin). Cosc is the load capacitor defined in the crystal oscillator specification, Cint is the internal capacitor, and Cpin is the parallel input capacitor.

(3) The crystal motional resistance Rm relates to the equivalent series resistance (ESR) by the following formula:

$$ESR = R_m \left(1 + \frac{C_0}{C_L}\right)^2$$

Measured with the load capacitance specified by the crystal manufacturer. In fact, if CXIN = CXOUT = 10 pF, then CL = 5 pF. Parasitic capacitance from the package and board must also be considered.

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RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

External coil for VDD2 and VIO	Value	0.7	1	1.3	µH
	DCR			0.1	Ω
	Saturation current	900			mA
External capacitor for VDD1, VDD2, VIO connected to VDD1.IN, VDD2.IN, VDD3.IN, and VDD1.OUT, VDD2.OUT, VIO.OUT	Value(4)	5	10	15	µF
	ESR at switching frequency	1		20	mΩ
Filtering capacitor for VMCC1.IN, VDAC.IN, VAUX12S.IN, VPPLA3R.IN, VINT.IN, VBAT.USB, VMMC1.OUT, VDAC.OUT, VAUX2.OUT, VPPL1, VINTDIG, VINTANA1, VINTANA2, VRRTC	Value	0.3	1	2.7	µF
	ESR	20		600	mΩ
Filtering capacitor for VUSB3V1, VUSB1V8, VUSB1V5	Value	0.5	2.2	6.5	µF
	ESR	20		600	mΩ
Filtering capacitor for voltage reference	Connected from V_{REF} to REFGND	0.3	1	2.7	µF
External capacitor for charge pump and VBUS	Filtering capacitor (Connected between VBUS.CPOUT and GND) and called CVBUS	1.41 (The minimum can be reduced to 1.2 µF, provided the charge-pump is only used to supply VUSB3V1 LDO)	4.7	6.5	µF
	Flying capacitor (Connected between CP.CAPP and CP.CAPM) called CVBUS.FC	1.32 (The minimum can be reduced to 1.2 µF, provided the charge-pump is only used to supply VUSB3V1 LDO)	2.2	3.08	µF
	Filtering capacitor ESR for CVUSB.IN and CVBUS.FC			20	mΩ
	Filtering capacitor CVBUS.IN	5	10	15	µF
External capacitor for power reference filter	Filtering capacitor	0.3	1	2.7	µF

(4) For TPS65921B1, in case of OMAP frequency ≥ 1 GHz, replace 10-µF capacitor on VDD1.OUT by two 22-µF capacitors. One capacitor must be placed near the PMIC and one near the OMAP device.

ELECTRICAL CHARACTERISTICS

CRYSTAL OSCILLATOR

When selecting a crystal, the system designer must consider the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system. The following table lists the switching characteristics of the oscillator.

Table 1. Base Oscillator Switching Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Crystal: Internal capacitor on each input (Cint)	8	10	12	pF
Crystal: Parallel input capacitance (Cpin)			1.0	pF
Parallel resonance crystal frequency		32.768		kHz
Pin-to-pin capacitance		1.6	1.8	pF

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Table 1. Base Oscillator Switching Characteristics (continued)

PARAMETER			MIN	TYP	MAX	UNIT
Maximum drive power					1.0	µW
Operating drive level					0.5	µW
Crystal quality factor			13k		54k	
t_{SX}	Start-up time, all conditions				500	ms
	Start-up time, 25°C				360	
I_{DDA}	Active current consumption (configured through the LOJIT bit)	High jitter mode			1.8	µA
		Low jitter mode			0.8	
I_{DDQ}	Current consumption	Low battery mode (1.2 V)			1	µA
		Startup			8	

CLOCK SLICER

PARAMETER	MODE(1)	MIN	TYP	MAX	UNIT
Internal coupling capacitor		4.2	5	5.7	pF
Parallel input resistance over 10 to 40 MHz range	LP	15		60	kΩ
	HP	30		75	kΩ
	BP/PD	1		100	MΩ
Parallel input capacitance over 10 to 40 MHz range	LP	0.3		0.8	pF
	HP	0.3		0.7	
	BP/PD	0.08		1	
	BP/PD	40		230	
Output duty cycle with V_{IN} = 0.2 V_{PP}	LP/HP	40%	50%	60%	
Propagation delay	LP	4		18	ns
	HP	3		15	
	BP/PD	0.2		3	
Power supply rejection ratio sideband (1% RMS of supply voltage added sine 5 MHz)	LP/HP	26			dBc
Current consumption at maximum input of 40 MHz	LP			175	µA
	HP			235	µA
	BP/PD			39	nA
Power-up time	LP/HP			1	ms
Output peak-to-peak jitter with an input peak-to-peak jitter < 0.1% and for jitter frequency below 300 kHz	LP/HP			0.2%	
Output peak-to-peak jitter with an input peak-to-peak jitter < 0.1% and for jitter frequency above 300 kHz	LP/HP			1.0%	

(1) Bypass input maximum voltage is the same as the maximum voltage provided for the I/O interface.

32KCLKOUT OUTPUT CLOCK

NAME	PARAMETER DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		32.768		kHz
C_L	Load capacitance			40	pF
V_{OUT}	Output clock voltage, depending on output reference level IO.1P8		1.8(1)		V
V_{OH}	Voltage output high	V_{OUT} – 0.45		V_{OUT}	V
V_{OL}	Voltage output low	0		0.45	V

(1) The output voltage depends on output reference level which is IO.1P8.

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The following table details the output clock timing characteristics. The following figure shows the 32KCLKOUT output clock waveform.

NAME	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
CK0	$1/t_{C(32KCLKOUT)}$	Frequency		32.768		kHz
CK1	$t_{W(32KCLKOUT)}$	Pulse duration, 32KCLKOUT low or high	0.40 × $t_{C(32KCLKOUT)}$		0.60 × $t_{C(32KCLKOUT)}$	ns
CK2	$t_{R(32KCLKOUT)}$	Rise time, 32KCLKOUT (1)			16	ns
CK3	$t_{F(32KCLKOUT)}$	Fall time, 32KCLKOUT (1)			16	ns
	SSB Phase Noise	At 1-kHz offset from the carrier			–110	dBc/Hz

(1) The output capacitive load is equivalent to 30 pF.

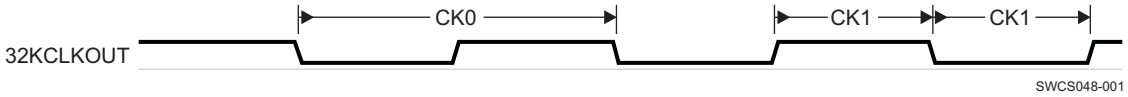

Figure 1. 32KCLKOUT Output Clock

HFCLKOUT OUTPUT CLOCK

The following table summarizes the HFCLKOUT output clock electrical characteristics.

Table 2. HFCLKOUT Output Clock Electrical Characteristics

NAME	PARAMETER DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		19.2, 26, or 38.4		MHz
C_L	Load capacitance			30	pF
V_{OUT}	Output clock voltage, depending on output reference level IO.1P8		1.8 (1)		V
V_{OH}	Voltage output high	V_{OUT} – 0.45		V_{OUT}	V
V_{OL}	Voltage output low	0		0.45	V

(1) The output voltage depends on output reference level which is IO.1P8.

The following table details the HFCLKOUT output clock timing characteristics.

Table 3. HFCLKOUT Output Clock Switching Characteristics

NAME	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
CHO1	$1/t_{C(HFCLKOUT)}$	Frequency		19.2, 26, or 38.4		MHz
CHO2	$t_{W(HFCLKOUT)}$	Pulse duration, HFCLKOUT low or high	0.4 × $t_{C(HFCLKOUT)}$		0.6 × $t_{C(HFCLKOUT)}$	ns
CHO3	$t_{R(HFCLKOUT)}$	Rise time, HFCLKOUT, low drive (1)				ns
		- Load: 5 pF			3.8	
		- Load: 10 pF			5.5	
		Rise time, HFCLKOUT, high drive (1)				
		- Load: 10 pF			2.9	
		- Load: 20 pF			5.0	

(1) Low drive: MISC_CFG[CLK_HF_DRV] = 0 (default)
High drive: MISC_CFG[CLK_HF_DRV] = 1

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Table 3. HFCLKOUT Output Clock Switching Characteristics (continued)

NAME	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
CHO4	$t_{F(HFCLKOUT)}$	Fall time, HFCLKOUT, low drive(1)				ns
		- Load: 5 pF			3.5	
		- Load: 10 pF			5.1	
		Fall time, HFCLKOUT, high drive(1)				
		- Load: 10 pF			2.7	
		- Load: 20 pF			4.7	

Figure 2 shows the HFCLKOUT output clock waveform.

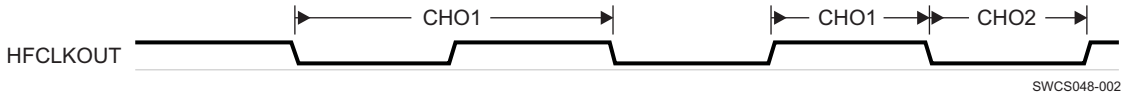
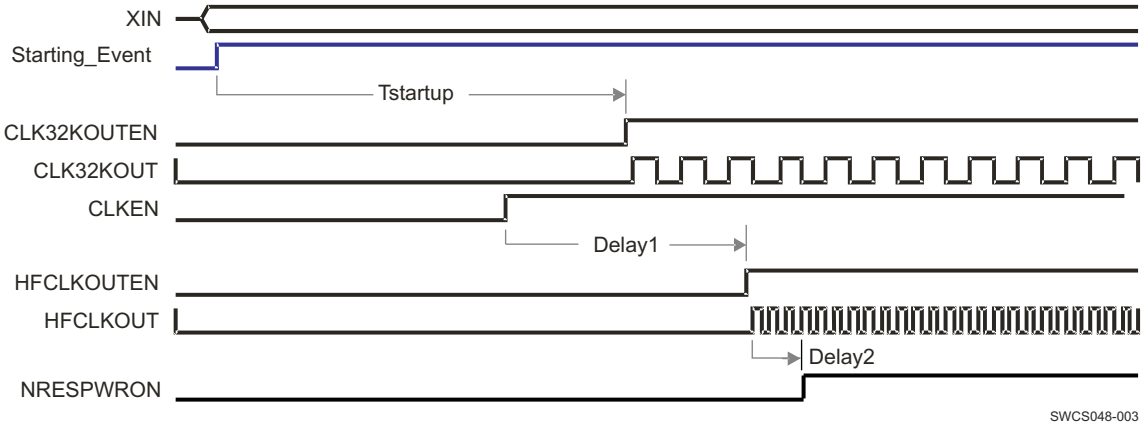


Figure 2. HFCLKOUT Output Clock

Figure 3 shows the 32KCLKOUT and HFCLKOUT clock stabilization time.



A. Tstartup, Delay1, Delay2, and Delay3 depend on the boot mode (See Power timing chapter).

Figure 3. 32KCLKOUT and HFCLKOUT Clock Stabilization Time

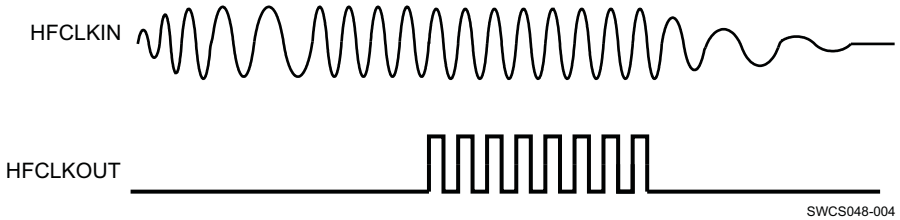


Figure 4. HFCLKOUT Behavior

VDD1 DCDC CONVERTER

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6		1.45	V
Output voltage step	0.6 to 1.45 V		12.5		mV
Output accuracy(1)	0.6 to < 0.8 V	–6%		6%	
	0.8 to 1.45 V	–5%		5%	
Switching frequency			3.2		MHz
Conversion efficiency(2)	I_O = 10 mA, sleep		82%		
	100 mA < I_O < 400 mA		85%		
	400 mA < I_O < 600 mA		80%		
	600 mA < I_O < 800 mA		75%		
Output current	Active mode Output voltage 0.6 V to 1.45 V for TPS65921B/TPS65921B1			1.2	A
	Active mode Output Voltage 1.2 V to 1.45 V for TPS65921B1			1.4	A
	Sleep mode			10	mA
Ground current (I_Q)	Off at 30°C			3	µA
	Sleep, unloaded		30	50	
	Active, unloaded, not switching			300	
Short-circuit current	V_{IN} = V_{MAX}		2.2		A
Load regulation	0 < I_O < I_{MAX}			20	mV
Transient load regulation at 1.2 A(3)	I_O = 10 mA to (I_{MAX}/3) + 10 mA, maximum slew rate is I_{MAX}/3/100 ns	–65		50	mV
Line regulation				10	mV
Transient line regulation	300 mV_{PP} ac input, 10-µs rise and fall time			10	mV
Start-up time			0.25	1	ms
Recovery time	From sleep to on with constant load		< 10	100	µs
Slew rate (rising or falling)(4)		4	8	16	mV/µs
Output ripple	Active (PWM and PSM)	–10		10	mV
	Sleep (PFM)	–2%		2%	
Current limit for PWM/PSM mode switch. PSM is below this limit, and PWM is above this limit.	Active mode	150		200	mA
Overshoot	Softstart			5%	
Output pulldown resistance	In Off mode		500	700	Ω

(1) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(2) VBAT = 3.6 V, VDD1 = 1.2 V, Fs = 3.2 MHz, L = 1 µH, L_{DCR} = 100 mΩ, C = 10 µF, ESR = 10 mΩ
(3) For negative transient load, the output voltage must discharge completely and settle to its final value within 100 ms. Transient load is specified at Vout max with a ±50% external capacitor accuracy and includes temperature and procress variation.
(4) Load current varies proportional to the output voltage. The slew rate is for increasing and decreasing voltages and the load current is 1.1 A.

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VDD2 DCDC CONVERTER

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6	1.0	1.5	V
Output voltage step	0.6 to 1.45 V		12.5		mV
Output accuracy(1)	0.6 to < 0.8 V	–6%		6%	
	0.8 to 1.45 V	–5%		5%	
Switching frequency			3.2		MHz
Conversion efficiency(2)	I_O = 10 mA, sleep		82%		
	100 mA < I_O < 300 mA		85%		
	300 mA < I_O < 500 mA		80%		
Output current	Active mode			600	mA
	Sleep mode			10	mA
Ground current (I_Q)	Off at 30°C			1	µA
	Sleep, unloaded		30	50	
	Active, unloaded, not switching			300	
Short-circuit current	V_{IN} = V_{MAX}		1.2		A
Load regulation	0 < I_O < I_{MAX}			20	mV
Transient load regulation(3)	I_O = 10 mA to (I_{MAX}/3) + 10 mA, maximum slew rate is I_{MAX}/3/100 ns	–65		50	mV
Line regulation				10	mV
Transient line regulation	300 mV_{PP} ac input, 10-µs rise and fall time			10	mV
Output pulldown resistance	In OFF mode		500	700	Ω
Start-up time			0.25	1	ms
Recovery time	From sleep to on with constant load		25	100	µs
Slew rate (rising or falling)(4)		4	8	16	mV/µs
Output ripple	Active (PWM and PSM)	–10		10	mV
	Sleep (PFM)	–2%		2%	
Current limit for PWM/PSM mode switch. PSM is below this limit, and PWM is above this limit.	Active mode	150		200	mA
Overshoot	Softstart			5%	

(1) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(2) VBAT = 3.8 V, VDD1 = 1.3 V, Fs = 3.2 MHz, L = 1 µH, L_{DCR} = 100 mΩ, C = 10 µF, ESR = 10 mΩ
(3) Output voltage must be able to discharge the load current completely and settle to its final value within 100 µs.
(4) Load current varies proportional to the output voltage. The slew rate is for increasing and decreasing voltages and the load current is 1.1 A.

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VIO DCDC CONVERTER

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
Input voltage range		2.7	3.6	4.5	V
Output voltage(1)			1.8 1.85		V
Output accuracy	DC accuracy only	–3%		3%	
	Including all variations (line and load regulations, line and load transients, temperature, and process)	–4%		4%	
Switching frequency			3.2		MHz
Conversion efficiency(2)	I_O = 10 mA, sleep		85%		
	100 mA < I_O < 400 mA		85%		
	400 mA < I_O < 600 mA		80%		
Output current	On mode			700	mA
	Sleep mode			10	mA
Ground current (I_Q)	Off at 30°C			1	µA
	Sleep, unloaded		30	50	
	Active, unloaded, not switching			300	
Load regulation	0 < I_O < I_{MAX}			20	mV
Line regulation				10	mV
Transient load regulation	I_O = 10 mA to (I_{MAX}/3) + 10 mA, maximum slew rate is I_{MAX}/3/100 ns	–65		50	mV
Transient line regulation	300 mV_{PP} ac input, 10-µs rise and fall time			10	mV
Start-up time			0.25	1	ms
Recovery time	From sleep to on with constant load		< 10	100	µs
Slew rate (rising or falling)		4	8	16	mV/µs
Output ripple	Active (PWM and PSM)	–10		10	mV
	Sleep (PFM)	–2%		2%	
Current limit for PWM/PSM mode switch. PSM is below this limit, and PWM is above this limit.	Active mode	150		200	mA
Overshoot	Softstart			5%	
Output pulldown resistance	In Off mode		500	700	Ω

(1) This voltage is tuned according to the platform and transient requirements.
(2) VBAT = 3.8 V, VIO = 1.8 V, Fs = 3.2 MHz, L = 1 µH, LDCR = 100 mΩ, C = 10 µF, ESR = 10 mΩ

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VMMC1 LOW DROPOUT REGULATOR

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.7	3.6	5.5	V
V_{OUT}	Output voltage including all variations (line and load regulations, line and load transients, temperature, and process)		1.7945 2.7645 2.91 3.0555	1.85 2.85 3.0 3.15	1.9055 2.9355 3.09 3.2445	V
I_{OUT}	Rated output current	On mode Low-power mode			220 5	mA
	DC load regulation	On mode: $0 < I_O < I_{MAX}$			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	50 40 25			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 290 17 20 1	µA
V_{DO}	Dropout voltage(1)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(2)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV
	Overshoot	Softstart			3%	
	Pulldownresistance	Default in off mode	250	320	450	Ω

(1) For nominal output voltage
(2) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, follow the output voltage specification.

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VDAC LOW DROPOUT REGULATOR

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage including all variations (line and load regulations, line and load transients, temperature, and process)		1.164 1.261 1.746	12 1.3 1.8	1.236 1.339 1.854	V
I_{OUT}	Rated output current	On mode Low-power mode			70 5	mA
	DC load regulation	On mode: $0 < I_O < I_{MAX}$			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 20 kHz 20 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	65 45 40			dB
	Output noise	200 Hz < f < 5 kHz 5 kHz < f < 400 kHz 400 kHz < f < 10 MHz			400 125 50	nV/√Hz
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 1$ mA Off mode at 55°C			150 350 15 25 1	µA
V_{DO}	Dropout voltage(1)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(2)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 60 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV
	Overshoot	Softstart			3%	
	Pull down resistance	Default in off mode	250	320	450	Ω

(1) For nominal output voltage
(2) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, follow the output voltage specification.

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VAUX2 LOW DROPOUT REGULATOR

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage including all variations (line and load regulations, line and load transients, temperature, and process)		–3%	1.3 1.5 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.8	+3%	V
I_{OUT}	Rated output current	On mode			100	mA
		Low-power mode			5	
	DC load regulation	On mode: $0 < I_O < I_{MAX}$			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz	50			dB
		10 kHz < f < 100 kHz	40			
		f = 1 MHz	30			
		$V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$				
	Ground current	On mode, $I_{OUT} = 0$			70	µA
		On mode, $I_{OUT} = I_{OUTmax}$			170	
		Low-power mode, $I_{OUT} = 0$			17	
		Low-power mode, $I_{OUT} = 5$ mA			20	
		Off mode at 55°C			1	
V_{DO}	Dropout voltage(1)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(2)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV			10	mV
		Slew: 40 mV/µs				
	Overshoot	Softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω
		Configurable as HighZ in off mode	100			MΩ

(1) For nominal output voltage
(2) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, follow the output voltage specification.

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VPLL1 LOW DROPOUT REGULATOR

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage including all variations (line and load regulations, line and load transients, temperature, and process)		0.97	1.0	1.03	V
			1.164	1.2	1.236	
			1.261	1.3	1.339	
			1.746	1.8	1.854	
I_{OUT}	Rated output current	On mode			40	mA
		Low-power mode			5	
	DC load regulation	On mode: $0 < I_O < I_{MAX}$			20	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz	50			dB
		10 kHz < f < 100 kHz	40			
		f = 1 MHz	30			
		$V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$				
	Ground current	On mode, $I_{OUT} = 0$			70	µA
		On mode, $I_{OUT} = I_{OUTmax}$			110	
		Low-power mode, $I_{OUT} = 0$			15	
		Low-power mode, $I_{OUT} = 1$ mA			16	
		Off mode at 55°C			1	
V_{DO}	Dropout voltage(1)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation(2)	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 60 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV
	Overshoot	Softstart			3%	
	Pulldown resistance	Default in off mode	250	320	450	Ω

(1) For nominal output voltage
(2) Transient load regulation is always included in the overall accuracy of the selected output voltage option. For voltage levels that have a tighter output voltage specification than the transient load regulation, follow the output voltage specification.

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INTERNAL LDOS

Internal LDOs (except USBCP, which is a boost) are described in following table.

NAME	USAGE	TYPE	VOLTAGE RANGE (V)	DEFAULT VOLTAGE (V)	MAXIMUM CURRENT
VINTANA1	Internal	LDO	1.5	1.5	50 mA
VINTANA2	Internal	LDO	2.5, 2.75	2.75	250 mA
VINTDIG	Internal	LDO	1.5	1.5	100 mA
USBCP	Internal	Charge pump	5	5	100 mA
VUSB1V5	Internal	LDO	1.5	1.5	30 mA
VUSB1V8	Internal	LDO	1.8	1.8	30 mA
VUSB3V1	Internal	LDO	3.1	3.1	14 mA
VRRTC	Internal	LDO	1.5	1.5	30 mA
VBRTC	Internal	LDO	1.3	1.3	100 µA

VOLTAGE REFERENCES

PARAMETER	TEST CONDITONS	MIN	TYP	MAX	UNIT
Internal bandgap reference voltage	On mode, measured through TESTV terminal	1.272	1.285	1.298	V
Reference voltage (V_{REF} terminal)	On mode	0.7425	0.75	0.7575	V
Retention mode reference	On mode	0.492	0.5	0.508	V
I_{REF} NMOS sink		0.9	1.0	1.1	µA
Ground current	Bandgap			25	µA
	I_{REF} block			20	
	Preregulator			15	
	V_{REF} buffer			10	
	Retention reference buffer			10	
Output spot noise	100 Hz			1	µV/√Hz
A-weighted noise (rms)			200		nV (rms)
P-weighted noise (rms)			150		nV (rms)
Integrated noise	20 Hz to 100 kHz		2.2		µV
I_{BIAS} trim bit LSB				0.1	µA
Ripple rejection	< 1 MHz from VBAT	60			dB
Start-up time				1	ms

BATTERY THRESHOLD LEVELS(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Main battery charged threshold VMBCH	Measured on VBAT terminal	3.14	3.2	3.3	V
Main battery low threshold VMBLO	Measured on VBAT terminal (monitored on terminal ONNOFF)	2.55	2.7	2.8	V
Main battery high threshold VMBHI	Measured on terminal VBAT	2.5	2.65	3.0	V
Batteries not present threshold VBNPR	Measured on terminal VBAT	1.6	1.8	2.6	V
	Measured on terminal VBAT in slave mode	1.95	2.1	2.6	V

(1) Backup ball must always be tied to ground.

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POWER CONSUMPTION

The typical power consumption is obtained in the nominal operating conditions and with the TPS65921 standalone.

MODE		DESCRIPTION		TYPICAL CONSUMPTION
C021 boot mode	WAIT-ON	The phone is apparently off for the user, a main battery is present and well-charged. The RTC registers, registers in backup domain are maintained. The wak-eup capabilities (like the PWRON button) are available.	VBAT = 3.8 V and Quartz present	64 µA × 3.8 V = 243.2 µW
	ACTIVE No Load HFCLK = 26 MHz	Subsystem is powered by the main battery. All supplies are enabled with no external load, internal reset is released, and the associated processor is running. USB intertupt handler consumes 433 µA (typ).	VBAT = 3.8 V	(2995 + 433) µA × 3.8 V = 13026 µW
	ACTIVE No Load HFCLK = 38.4 MHz			(3879 + 433) µA × 3.8 V = 16386 µW
	SLEEP No Load	The main battery powers subsystem. Selected supplies are enabled but in low-consumption mode and associated processor is in low-power mode.	VBAT = 3.8 V	492 µA × 3.8 V = 1870 µW

USB CHARGE PUMP

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	On mode: V_{IN} = VBAT	2.7	3.6	4.5	V
V_O	Output voltage		4.625	5.0	5.25	V
I_{load}	Rated output current	VBAT > 3 V at VBUS	0		100	mA
		2.7 V < VBAT < 3 V, at VBUS	0		50	
	Efficiency	I_{LOAD} = 100 mA, VBAT = 3.6 V		55%		
	Setting time	$I_{LOADmax/2}$ to $I_{LOADmax}$ in 5 µs		100	400	µs
	Start-up time				3	ms
	Short-circuit limitation current		250	350	450	mA
	DC load regulation	$I_{LOADmin}$ to $I_{LOADmax}$		250	500	mV
	DC line regulation	3.0 V to $VBAT_{max}$		250	350	mV
		I_{LOAD} = 100 mA				
	Transient load regulation	$I_{VBUS_5Vmax/2}$ – IVBUS_5Vmax 50 µs, C = 2 × 4.7 µF		300	350	mV
		0 – $I_{VBUS_5Vmax/2}$, 50 µs, C = 2 × 4.7 µF			350	
	Transient line regulation	$VBAT_{min}$ to $VBAT_{max}$ in 50 µs, C = 2 × 4.7 µF		300	350	mV

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HOT-DIE DETECTION AND THERMAL SHUTDOWN

PARAMETER	THRESHOLD (NOMINAL)(1)
Thermal hot-die selection THERM_HDSEL[1:0]	Threshold (nominal)(1)
00 (1st hot-die threshold)	Rising temp: 120°C
	Falling temp: 111°C
01 (2nd hot-die threshold)	Rising temp: 130°C
	Falling temp: 121°C
10 (3rd hot-die threshold)	Rising temp: 140°C
	Falling temp: 131°C
11 (4th hot-die threshold)	Not used
Thermal shutdown enable	Threshold (nominal)(1) - Rising temp: 150°C
	Threshold (nominal)(1) - Falling temp: 140°C

(1) The minimum/maximum range is ±5%

USB

LS/FS SINGLE-ENDED RECEIVERS

	PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
USB Single-Ended Receivers						
Skew between VP and VM	SKWVP_VM	Driver outputs unloaded	–2	0	2	ns
Single-ended hysteresis	V_{SE_HYS}		50			mV
High (driven)	V_{IH}		2			V
Low	V_{IL}				0.8	V
Switching threshold	V_{TH}		0.8		2	V

LS/FS DIFFERENTIAL RECEIVER

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
Differential input sensitivity	VDI	Ref. USB2.0	200			mV
Differential common mode range	VCM	Ref. USB2.0	0.8		2.5	V

LS/FS TRANSMITTER

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
Low	VOL	Ref. USB2.0	0		300	mV
High (driven)	VOH	Ref. USB2.0	2.8		3.6	V
Output signal crossover voltage	VCRS	Ref. USB2.0, covered by eye diagram	1.3		2.0	V
Rise time	TFR	Ref. USB2.0, covered by eye diagram	75		300	ns
Fall time	TFF		75		300	ns
Differential rise and fall time matching	TFRFM		80%		125%	
Low-speed data rate	TFDRATE	Ref. USB2.0, covered by eye diagram	1.4775		1.5225	Mbps
Source jitter total (including frequency tolerance):						

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PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
- To next transition	TDJ1	Ref. USB2.0, covered by eye diagram	–25		25	ns
- For paired transitions	TDJ2		–10		10	
Source SE0 interval of EOP	TFEOPT	Ref. USB2.0, covered by eye diagram	1.25		1.5	µs
Downstream eye diagram		Ref. USB2.0, covered by eye diagram				
Differential common mode range	VCM	Ref. USB2.0	0.8		2.5	V

FS TRANSMITTER

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
Low	VOL	Ref. USB2.0	0		300	mV
High (driven)	VOH	Ref. USB2.0	2.8		3.6	V
Output signal crossover voltage	VCRS	Ref. USB2.0, covered by eye diagram	1.3		2.0	V
Rise time	TFR	Ref. USB2.0	4		20	ns
Fall time	TFF	Ref. USB2.0	4		20	ns
Differential rise and fall time matching	TFRFM	Ref. USB2.0, covered by eye diagram	90%		111.11%	
Driver output resistance	ZDRV	Ref. USB2.0	28		44	Ω
Full-speed data rate	TFDRATE	Ref. USB2.0, covered by eye diagram	11.97		12.03	Mbps
Source jitter total (including frequency tolerance):						
- To next transition	TDJ1	Ref. USB2.0, covered by eye diagram	–2		2	ns
- For paired transitions	TDJ2		–1		1	
Source SE0 interval of EOP	TFEOPT	Ref. USB2.0, covered by eye diagram	160		175	ns
Downstream eye diagram		Ref. USB2.0, covered by eye diagram				
Upstream eye diagram						

HS DIFFERENTIAL RECEIVER

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
High-speed squelch detection threshold (differential signal amplitude)	VHSSQ	Ref. USB2.0	100		150	mV
High-speed disconnect detection threshold (differential signal amplitude)	VHSDSC	Ref. USB2.0	525		625	V
High-speed differential input signaling levels		Ref. USB2.0, specified by eye pattern templates				mV
High-speed data signaling common mode voltage range (guidelines for receiver)	VHSCM	Ref. USB2.0	–50		600	mV
Receiver jitter tolerance		Ref. USB2.0, specified by eye pattern templates			150	ps

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HS TRANSMITTER

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
High-speed idle level	VHSOI	Ref. USB2.0	–10		10	mV
High-speed data signaling high	VHSOH	Ref. USB2.0	360		440	mV
High-speed data signaling low	VHSOL	Ref. USB2.0	–10		10	mV
Chirp J level (differential voltage)	VCHIRPJ	Ref. USB2.0	700		1100	mV
Chirp K level (differential voltage)	VCHIRPK	Ref. USB2.0	–825		–500	mV
Rise Time (10% – 90%)	THSR	Ref. USB2.0, covered by eye diagram	500			
Fall time (10% – 90%)	THSR	Ref. USB2.0, covered by eye diagram	500			
Driver output resistance (which also serves as high-speed termination)	ZHSDRV	Ref. USB2.0	40.5		49.5	Ω
High-speed data range	THSDRAT	Ref. USB2.0, covered by eye diagram	479.76		480.24	Mbps
Data source jitter		Ref. USB2.0, covered by eye diagram				
Downstream eye diagram		Ref. USB2.0, covered by eye diagram				
Upstream eye diagram		Ref. USB2.0, covered by eye diagram				

UART TRANSCEIVER

PARAMETER		MIN	MAX	UNIT
$t_{PH_DP_CON}$	Phone D+ connect time	100		ms
$t_{PH_DISC_DET}$	Phone D+ disconnect time	150		ms
f_{UART_DFLT}	Default UART signaling rate (typical rate)		9600	bps

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
UART Transmitter CEA-2011						
Phone UART edge rates	$t_{PH_UART_EDGE}$	DP_PULLDOWN asserted			1	Ms
Serial interface output high	V_{OH_SER}	ISOURCE = 4 mA	2.4	3.3	3.6	V
Serial interface output low	V_{OL_SER}	ISINK = –4 mA	0	0.1	0.4	V
UART Receiver CEA-2011						
Serial interface input high	V_{IH_SER}	DP_PULLDOWN asserted	2.0			V
Serial interface input low	V_{IL_SER}	DP_PULLDOWN asserted			0.8	V
Switching threshold	V_{TH}		0.8		2.0	V

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PULLUP/PULLDOWN RESISTORS

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
Pullup Resistors						
Bus pullup resistor on upstream port (idle bus)	R_{PUI}	Bus idle	0.9	1.1	1.575	kΩ
Bus pullup resistor on upstream port (receiving)	R_{PUA}	Bus driven/driver's outputs unloaded	1.425	2.2	3.09	
High (floating)	V_{IHZ}	Pullups/pulldowns on both DP and DM lines	2.7		3.6	V
Phone D+ pullup voltage	$V_{PH_DP_UP}$	Driver's outputs unloaded	3.0	3.3	3.6	V
Pulldown Resistors						
Phone D+/– pulldown	$R_{PH_DP_DWN}$ $R_{PH_DM_DWN}$	Driver's outputs unloaded	14.25	18	24.8	kΩ
High (floating)	V_{IHZ}	Pullups/pulldowns on both DP and DM lines	2.7		3.6	V
D+/– Data line						
Upstream facing port	C_{INUB}	[1.0]		22	75	pF
On-the-go device leakage	$V_{OTG_DATA_LKG}$	[2]			0.342	V
Input impedance exclusive of pullup/pulldown	Z_{INP}	Driver's outputs unloaded	300			kΩ

OTG VBUS

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
VBUS Wakeup Comparator						
VBUS wake-up delay	$DEL_{VBUS_WK_UP}$				15	µs
VBUS Comparators						
A-device session valid	$V_{A_SESS_VLD}$		0.8	1.1	1.4	V
A-device V_{BUS} valid	$V_{A_VBUS_VLD}$		4.4	4.5	4.625	V
B-device session end	$V_{B_SESS_END}$		0.2	0.5	0.8	V
B-device session valid	$V_{B_SESS_VLD}$		2.1	2.4	2.7	V
VBUS Line						
A-device VBUS input impedance to ground	$R_{A_BUS_IN}$	SRP (VBUS pulsing) capable A-device not driving VBUS	13.77		100	kΩ
B-device VBUS SRP pulldown	$R_{B_SRP_DWN}$	5.25 V / 8 mA, pullup voltage = 3 V	0.656	10		kΩ
B-device VBUS SRP pullup	$R_{B_SRP_UP}$	(5.25 V – 3 V) / 8 mA, pullup voltage = 3 V	0.85	1.3	1.75	kΩ
B-device VBUS SRP rise time maximum for OTG-A communication	$t_{RISE_SRP_UP_MAX}$	0 to 2.1 V with < 13 µF load			34	ms
B-device VBUS SRP rise time minimum for standard host connection	$t_{RISE_SRP_UP_MIN}$	0.8 to 2.0 V with > 97 µF load	46			ms

OTG ID

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
VBUS Wakeup Comparator						
ID wake-up comparator	$R_{ID_WK_UP}$	Wakeup when ID shorted to ground.	30		100	kΩ
ID Comparators — ID External Resistors Specifications						
ID ground comparator	R_{ID_GND}	ID_GND interrupt	4	20	25	kΩ

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PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
ID Float comparator	R_{ID_FLOAT}	ID_FLOAT interrupt	200		500	kΩ
ID Line						
Phone I_D pullup to $V_{PH_ID_UP}$	$R_{PH_ID_UP}$	ID unloaded (VRUSB)	70	90	286	kΩ
Phone I_D pullup voltage	$V_{PH_ID_UP}$	Connected to VRUSB	2.5		3.2	V
ID line maximum voltage					5.25	V

USB CHARGER DETECTION

USB Charger Detection Debounce Time							
REQUIREMENT	**PARAMETER**	**NB CLOCK**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Minimum 10 ms	DEBVBUS_TIME	448	ACTIVE/SLEEP mode	13.7		13.7	ms
Minimum 20 ms	DEBUSBCHG_TIME	896	ACTIVE/SLEEP mode	27.3		27.3	ms

Table 4. Voltages

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT	REF
Logic Threshold	V_{LGC}		0.8	2.0	V	1.4.4
D+ Source Voltage	V_{DP_SRC}	Output current > 250 µA	0.5	0.675	V	
Data Detect Voltage	V_{DAT_REF}		0.25	0.4	V	
Data Line Leakage Voltage	V_{DAT_LKG}		0	3.6	V	3.9

Table 5. Currents

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNIT	REF
Portable Device Current from Charging Host Port during chirp	$I_{DEV_HCHG_CHRP}$			710	mA	3.6.2
Data Contact Detect Current Source	I_{DP_SRC}		7	13	µA	
D- Sink Current	I_{DM_SINK}		50	150	µA	

Table 6. Resistances

D+ pulldown resistance	R_{DP_DWN}			14.25	24.8	kΩ
D- pulldown resistance	R_{DM_DWN}			14.25	24.8	kΩ

Table 7. USB Charger Detection (Wait and Debounce Timing)

USB Charger Detection (Wait and Debounce Timing)							
Requirement	**PARAMETER**	**NB CLOCK**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Minimum 200 us	D+ Current source on-time TIDP_SRC_ON	8	ACTIVE/SLEEP mode(1)	244.1		244.1	µs
Minimum 40 ms	D+ Voltage source on-time TVDP_SRC_ON	1792	ACTIVE/SLEEP mode(1)	54.7		54.7	ms
Minimum 40 ms	D+ Voltage source off to high current TVDP_SRC_HICRNT	1792	ACTIVE/SLEEP mode(1)	54.7		54.7	ms
Minimum 2 s	DATA_CONTACT_DETECT Timeout TDCD_TIMEOUT	89600	ACTIVE/SLEEP mode(1)	2.73		2.73	s

(1) Note: LS Device mode not supported

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MADC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10		Bit
Input dynamic range for external input ADCIN0		0		1.5	V
MADC voltage reference			1.5		V
Differential nonlinearity		–1		1	LSB
Integral nonlinearity	Best fitting	–2		2	LSB
Offset	Best fitting	–28.5		28.5	mV
Input bias			1		µA
Input capacitor CBANK				10	pF
Input current leakage				1	µA

MADC Analog Input Range and Prescaler Ratio

MADC CHANNEL	INT/EXT	ANALOG INPUT RANGE (V)		PRESCALER			
		MIN	MAX	OUTPUT RANGE (V)		DIVIDER RATIO	NOTE
				MIN	MAX		
ADCIN0: General-purpose input (1)	External	0.0	1.5	N/A	N/A	1	No prescaler
ADCIN1:7 Reserved	Internal	N/A	N/A	N/A	N/A	N/A	Not used
ADCIN8: VBUS Voltage (VBUS)	Internal	0.0	6.5	0.0	1.5	3/14	Prescaler in USB subchip. Rdivider = (6 × 2.76 kΩ)/(28 × 2.76 kΩ) (typ) (2)
ADCIN9: Reserved	Internal						Not used
ADCIN10:11 Reserved	Internal	N/A	N/A	N/A	N/A	N/A	
ADCIN12: Main battery voltage (VBAT)	Internal	2.7	4.7	0.675	1.175	0.25	Prescaler integrated Rdivider = 9.85 kΩ/(4 × 9.85 kΩ) (typ) (3)
ADCIN13:15 Reserved	Internal	N/A	N/A	N/A	N/A	N/A	

(1) General-purpose input has to be tied to ground when TPS65921 internal power supply (VINTANA1) is off.
(2) Tolerance for resistors-type (PL_VHSR): ±19%
(3) Tolerance for resistors-type (PL_HR): ±12%

The table below summarizes the sequence conversion timing characteristics. Figure 5 shows one conversion sequence general timing diagram.

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
F	Running frequency		1		MHz
T = 1/F	Clock period		1		µs
N	Number of analog inputs to convert in a single sequence	0		16	
Tstart	SW1, SW2, or USB asynchronous request or real-time STARTADC request	3		4	µs

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Tsettling time	Settling time to wait before sampling a stable analog input (capacitor bank charge time) Tsettling is calculated from the max((Rs + Ron)*Cbank) of all possible input sources (internal or external). Ron is the resistance of the selection analog input switches (5 kOHM). This time is software programmable by OCP register; default value is 12 µs.	5	12	260	µs
Tstartsar	The successive approximation registers ADC start time		1		µs
Tadc time	The successive approximation registers ADC conversion time		10		µs
Tcapture time	Tcapture time is the conversion result capture time.		2		µs
Tstop		1		2	µs
Full Conversion Sequence Time	Only one channel (N = 1) (1)	22		39	µs
	All channels(2)	352		624	
Conversion Sequence Time	Without Tstart and Tstop: Only one channel (N = 1) (1)	18		33	µs
	Without Tstart and Tstop: All channels(1)	288		528	
STARTADC pulse duration	STARTADC period is T	0.33			µs

(1) General-purpose input ADCIN0 must be tied to ground when TPS65921 internal power supplies (VINTANA1) is off.
(2) Total Sequence Conversion Time General Formula: Tstart + N × (1 + Tsettling + Tadc + Tcapture) + Tstop.

This table is illustrated in Figure 5. The Busy parameter indicates that a conversion sequence is running, and the channel N result register parameter corresponds to the result register of RT/GP selected channel.

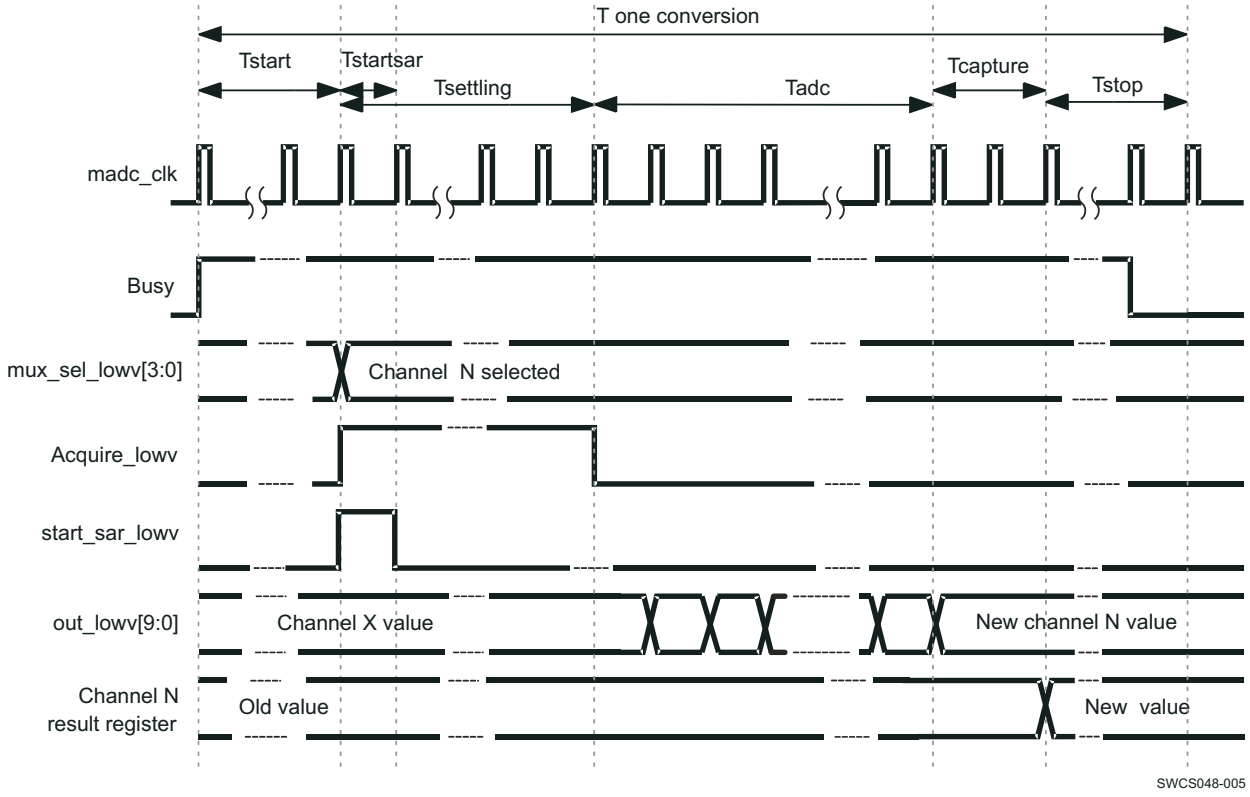

Figure 5. One Conversion Sequence General Timing Diagram

MADC Power Consumption

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power on consumption	Running frequency f = 1 MHz		1 (1)		mA
Power down consumption			1		µA

(1) The consumption is given in stand-alone mode.

TPS65921 INTERFACE TARGET FREQUENCIES

Table below assumes testing over the recommended operating conditions.

I/O INTERFACE	INTERFACE DESIGNATION		TARGET FREQUENCY
			1.5 V
SmartReflex I2C General-purpose I2C	I^2C Interface	Slave high-speed mode	3.6 Mbps
		Slave fast-speed mode	400 kbps
		Slave standard mode	100 kbps
USB	USB	High speed	480 Mbps
		Full speed	12 Mbps
		Low speed	1.5 Mbps
JTAG	Real/View® ICE tool		30 MHz
	XDS560 and XDS510 tools		30 MHz
	Lauterbach™ tool		30 MHz

I^2C Timing

The TPS65921 provides two I^2C HS slave interfaces (one for general-purpose and one for SmartReflex). These interfaces support the standard mode (100 kbps), fast mode (400 kbps), and HS mode (3.5 Mbps). The general-purpose I^2C module embeds four different slave hard-coded addresses (ID1 = 48h, ID2 = 49h, ID3 = 4Ah, and ID4 = 4Bh). The SmartReflex I^2C module uses one slave hard-coded address (ID5). The master mode is not supported.

Table 8 and Table 9 assume testing over the recommended operating conditions.

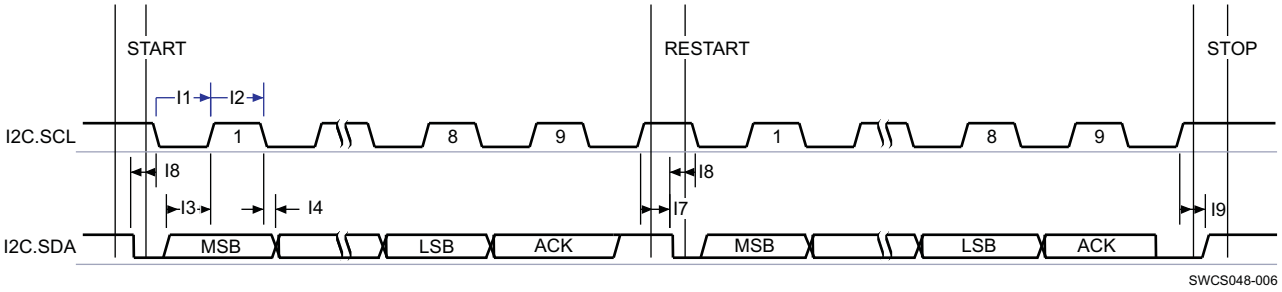

Figure 6. I^2C Interface—Transmit and Receive in Slave Mode

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Table 8. I²C Interface Timing Requirements (1) (2)

NO.	PARAMETER		MIN	MAX	UNIT
Slave High-Speed Mode					
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	10		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0	70	ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	160		ns
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	160		ns
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	160		ns
Slave Fast-Speed Mode					
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	100		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0	0.9	µs
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	0.6		µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	0.6		µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	0.6		µs
Slave Standard Mode					
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	250		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0		ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	4.7		µs
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	4		µs
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	4		µs

(1) The input timing requirements are given by considering a rising or falling time of:
80 ns in high-speed mode (3.4 Mbits/s)
300 ns in fast-speed mode (400 Kbits/s)
1000 ns in standard mode (100 Kbits/s)
(2) SDA is equal to I2C.SR.SDA or I2C.CNTL.SDA
SCL is equal to I2C.SR.SCL or I2C.CNTL.SCL

Table 9. I²C Interface Switching Requirements (1) (2)

NO.	PARAMETER		MIN	MAX	UNIT
Slave High-speed Mode					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	160		ns
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	60		ns
Slave Fast-speed Mode					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	1.3		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	0.6		µs
Slave Standard Mode					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	4		µs

(1) The capacitive load is equivalent to:
100 pF in high-speed mode (3.4 Mbits/s)
400 pF in fast-speed mode (400 Kbits/s)
400 pF in standard mode (100 Kbits/s)
(2) SDA is equal to I2C.SR.SDA or I2C.CNTL.SDA
SCL is equal to I2C.SR.SCL or I2C.CNTL.SCL

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JTAG INTERFACES

Table 10 and Table 11 assume testing over the recommended operating conditions.

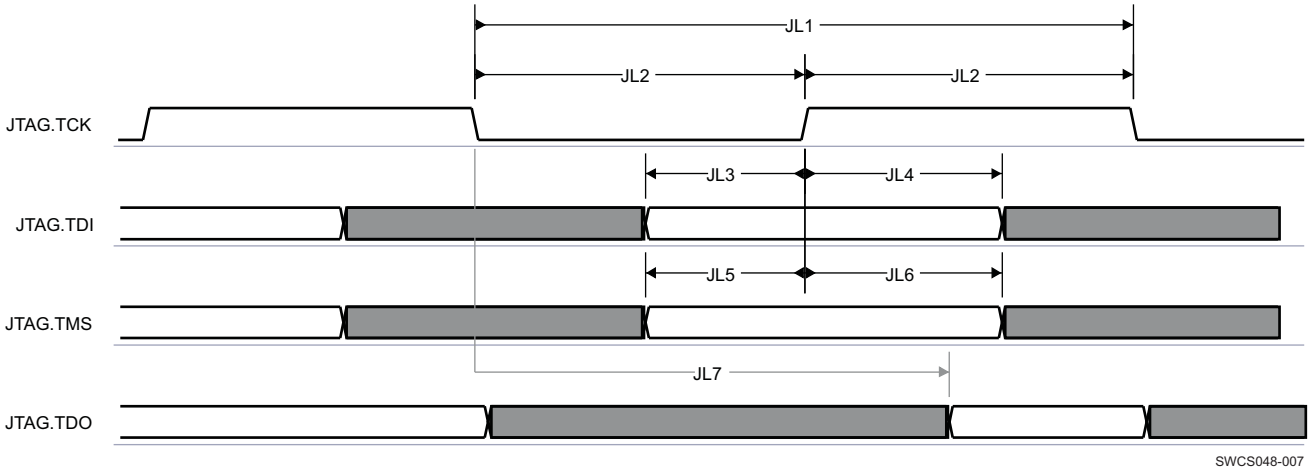

Figure 7. JTAG Interface Timing

The input timing requirements are given by considering a rising or falling edge of 7 ns.

JTAG Interface Timing Requirements

Table 10. JTAG Interface Timing Requirements

NO.	PARAMETER		MIN	MAX	UNIT
Clock					
JL1	$t_{c(TCK)}$	Cycle time, JTAG.TCK period	30		ns
JL2	$t_{w(TCK)}$	Pulse duration, JTAG.TCK high or low (1)	0.48 × P	0.52 × P	ns
Read Timing					
JL3	$t_{su(TDIV-TCKH)}$	Setup time, JTAG.TDI valid before JTAG.TCK high	8		ns
JL4	$t_{h(TDIV-TCKH)}$	Hold time, JTAG.TDI valid after JTAG.TCK high	5		ns
JL5	$t_{su(TMSV-TCKH)}$	Setup time, JTAG.TMS valid before JTAG.TCK high	8		ns
JL6	$t_{h(TMSV-TCKH)}$	Hold time, JTAG.TMS valid after JTAG.TCK high	5		ns

(1) P = JTAG.TCK clock period

The capacitive load is equivalent to 35 pF.

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JTAG Interface Switching Characteristics

Table 11. JTAG Interface Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
Write Timing					
JL7	$t_{d(TCK-TDOV))}$	Delay time, JTAG, TCK active edge to JTAG.TDO valid	0	14	ns

NO.	PARAMETER		MIN	MAX	UNIT
Clock					
JL1	$t_{c(TCK)}$	Cycle time, JTAG.TCK period	30		ns
JL2	$t_{w(TCK)}$	Pulse duration, JTAG.TCK high or low(1)	0.48 × P	0.52 × P	ns
Read Timing					
JL3	$t_{su(TDIV-TCKH)}$	Setup time, JTAG.TDI valid before JTAG.TCK high	8		ns
JL4	$t_{h(TDIV-TCKH)}$	Hold time, JTAG.TDI valid after JTAG.TCK high	5		ns
JL5	$t_{su(TMSV-TCKH)}$	Setup time, JTAG.TMS valid before JTAG.TCK high	8		ns
JL6	$t_{h(TMSV-TCKH)}$	Hold time, JTAG.TMS valid after JTAG.TCK high	5		ns

(1) P = JTAG.TCK clock period

Debouncing Time

Debounce times are listed in Table 12.

Table 12. Debouncing Time

DEBOUNCING FUNCTIONS	BLOCK	PROGRAMMABLE	DEBOUNCING TIME	DEFAULT
Main battery charged threshold (<3.2 V)	Battery monitoring	No	580 µs	580 µs
Main battery low threshold detection (<2.7 V)		No	60 µs	60 µs
Main battery plug detection		No	60 µs	60 µs
Debouncing functions interrupt generation debounce	POWER	No	125.6 µs	125.6 µs
Plug/unplug detection VBUS (1)	USB	Yes	0 to 250 ms (32/32768-second stgif)	30 ms
Plug/unplug detection ID (2)	USB	Yes	0 to 250 ms (32/32768-second stgif)	50 ms
Debouncing functions interrupt generation debounce for VBUS and ID (3)	POWER	Yes	0 to 233 ms	28 ms
Hot-die detection	Thermistor	No	60 µs	60 µs
Thermal shutdown detection		No	60 µs	60 µs
PWRON (4)	Start/stop button	No	31.25 ms	31.25 ms
NRESWARM	Button reset	No	60 µs	60 µs
MMC1/2 (plug/unplug)	GPIO	Yes	0 or 28 ms ± 2 ms	0 ms

(1) Programmable in the VBUS_DEBOUNCE register.
(2) Programmable in the ID_DEBOUNCE register.
(3) Programmable in the RESERVED_E[2:0] CFG_VBUSDEB register
(4) The PWRON signal is debounced 1024 × CLK32K (maximum 1026 × CLK32K) falling edge in master mode.

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DEVICE INFORMATION

Figure 8 shows the ball locations for the 120-ball plastic ball grid array (PBGA) package and is used in conjunction with ball description to locate signal names and ball grid numbers.

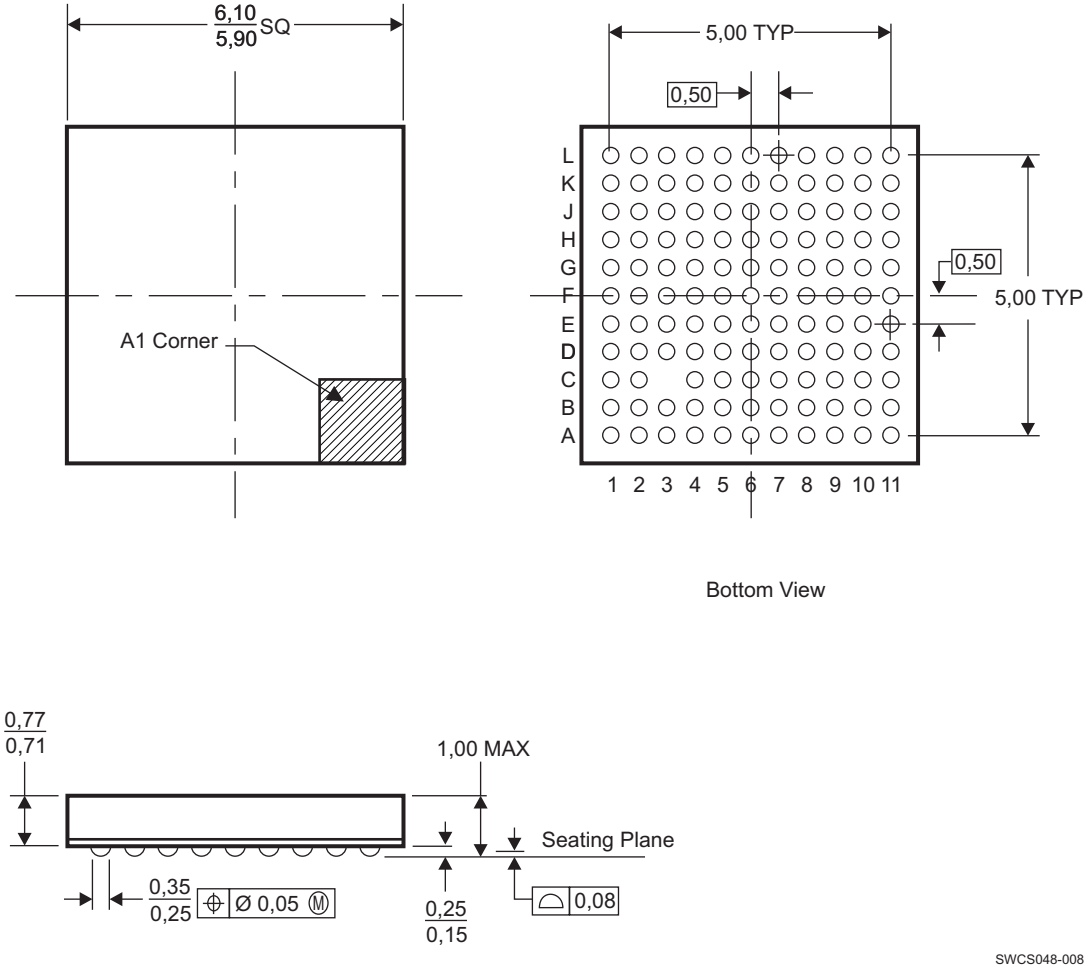

Figure 8. PBGA Bottom View

Table 13. Terminal/Pin Functions

NAME	BALL	SUPPLIES	TYPE	I/O	DESCRIPTION	PU/PD
ADCIN0	F2		Analog	I/O	General-purpose ADC input	NO
STARTADC	H7	VDDIO/DGND	Digital	I	ADC conversion request/JTAG test data input	NO
I2C.CNTL.SDA	C4	VDDIO/DGND	Digital	I/O	I^2C bidirectional data signal	External PU
I2C.CNTL.SCL	B3	VDDIO/DGND	Digital	I/O	I^2C bidirectional clock signal	External PU
I2C.SR.SDA	D4	VDDIO/DGND	Digital	I/O	HS I^2C bidirectional data signal	External PU
I2C.SR.SCL	A3	VDDIO/DGND	Digital	I/O	HS I^2C bidirectional Clock signal	External PU
PWRON	D5	VBAT/GND	Digital	I	Input detects a control command to start or stop the system.	External PU
REGEN	G3		Digital	O	Enable signal for external LDO	PU

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Table 13. Terminal/Pin Functions (continued)

MSECURE	G8	VDDIO/DGND	Digital	I	Security and digital rights management	NO
BOOT0	E5	VBAT/GND	Digital	I	Power-up sequence selection	Programmable PD (default active)
BOOT1	F6	VBAT/GND	Digital	I	Power-up sequence selection	Programmable PD (default active)
NRESPWRON	E7	VDDIO/DGND	Digital	O	Output control the NRESPWRON of the application processor	NO
NRESWARM	H8	VDDIO/DGND	Digital	I	Warm reset signal	PU
NSLEEP1	K4	VDDIO/DGND	Digital	I	ACTIVE-SLEEP state transition control signal	NO
INT1	A9	VDDIO/DGND	Digital	O	Output line interrupt	NO
SYSEN	B9	VDDIO/DGND	Digital	O	System enable output	NO
CLKEN	F10	VDDIO/DGND	Digital	O	Clock Enable	NO
32KCLKOUT	G6	VDDIO/DGND	Digital	O	32-kHz clock output	PD disabled in ACTIVE state
32KXOUT	G11	VRTC/REFGND	Analog	I	32-kHz crystal oscillator	NO
32KXIN	H11	VRTC/REFGND	Analog	I	32-kHz crystal oscillator	NO
HFCLKIN	C8	VDDIO/DGND	Analog	I	Sine wave or square wave input	NO
HFCLKOUT	K8	VDDIO/DGND	Digital	O	50% duty cycle square wave output	NO
VREF	G10	VREF/REFGND	Analog	O	Bandgap voltage	NO
GND_AGND	K7	AGND	Analog	I/O	Substrate ground	NO
AGND	H10	REFGND	Analog	I/O	Reference ground	NO
DGND	B8	DGND	Power	I/O	Digital ground	NO
IO.1P8	A10		Power	I	Supply for I/O buffers (VDDIO)	NO
BKBAT	G9	VBACKUP/AGND	Power	I	Not used. Must be grounded	NO
VDD1.IN	E9, E10, E11		Power	I	VDD1 DCDC input	NO
VDD1.GND	A11, B10, B11		Power	I/O	VDD1 DCDC power ground	NO
VDD1.L	C10, C11, D10		Power	O	VDD1 DCDC switched output	NO
VDD1.OUT	D11		Analog	I	VDD1 feedback voltage	PD
VDD2.IN	K10, L10		Power	I	VDD2 DCDC input	NO
VDD2.GND	J10, J11		Power	I/O	VDD2 DCDC power ground	NO
VDD2.L	K11, L11		Power	O	VDD2 DCDC switched output	NO
VDD2.OUT	H9		Analog	I	VDD2 feedback voltage	PD
VIO.IN	K2, L2		Power	I	VIO DCDC input	NO
VIO.GND	J1, J2		Power	I/O	VIO DCDC power ground	NO
VIO.L	K1, L1		Power	O	VIO DCDC switched output	NO
VIO.OUT	H1		Analog	I	VIO feedback voltage	PD
VAUX12S.IN	F1		Power	I	VAUX2 LDO input	NO
VAUX2.OUT	G1		Power	O	VAUX2 regulator output	PD
VPLLA3R.IN	A6		Power	I	VPLL1/VRTC LDO input	NO
VPLL1.OUT	A8		Power	O	VPLL1 LDO regulator output	PD

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Table 13. Terminal/Pin Functions (continued)

VRTC.OUT	B5		Power	O	VRTC internal LDO regulator output (internal use only)	PD
VINT.IN	A7		Power	I	VINTDIG LDO input	NO
VINTANA1.OUT	D1		Power	O	VINTANA1 internal LDO regulator output (internal use only)	PD
VINTANA2.OUT	A2		Power	O	VINTANA2 internal LDO regulator output (internal use only)	PD
VDAC.IN	C1		Power	I	VDAC/VINTANA1/VINTAN2 LDO input	NO
VDAC.OUT	E1		Power	O	VDAC LDO regulator output	PD
VINTDIG.OUT	B7		Power	O	VINTDIG internal LDO regulator output (internal use only)	PD
VMMC1.OUT	A1		Power	O	VMMC1 LDO regulator output	PD
VBAT.USB	K6		Power	I	VINTUSBiP5,VINTUSB1P8, VUSB.3P1 input regulator	NO
VUSB.3P1	L6		Power	O	VUSB.3P1 LDO regulator output	PD
VINTUSB1P8.OUT	J6		Power	O	VUSB1P8 LDO regulator output (internal use only)	PD
VINTUSB1P5.OUT	J5		Power	O	VUSB1P5 LDO regulator output (internal use only)	PD
TESTV1	H2		Analog	IO	Analog test pin 1	NO
TESTV2	C9		Analog	IO	Analog test pin 2	NO
TEST	D3	VDDIO/DGND	Digital	IO	Selection between JTAG mode and application mode	PD
AVSS1	F3	AGND	Power	I/O	Analog ground	NO
AVSS2	H6	AGND	Power	I/O	Analog ground	NO
AVSS3	F9	AGND	Power	I/O	Analog ground	NO
AVSS4	A4	AGND	Power	I/O	Analog ground	NO
VBUS	K5		Power		VBUS power rail	NO
DP/UART3.RXD	L7		Analog	I/O	USB differential data line	NO
DN/UART3.TXD	L8		Analog	I/O	USB differential data line	NO
ID	J7	VDDIO/DGND	Digital	I/O	USB ID	NO
UCLK	D6	VDDIO/DGND	Digital	I/O	HS USB Clock	NO
STP/GPIO.9	E6	VDDIO/DGND	Digital	I/O	HS USB Stop	NO
DIR/GPIO.10	A5	VDDIO/DGND	Digital	I/O	HS USB Direction	NO
NXT/GPIO.11	C5	VDDIO/DGND	Digital	I/O	HS USB Next	NO
DATA0/UART4.TXD	B6	VDDIO/DGND	Digital	I/O	HS USB Data0	NO
DATA1/UART4.RXD	C6	VDDIO/DGND	Digital	I/O	HS USB Data1	NO
DATA2/UART4.RTSI	C7	VDDIO/DGND	Digital	I/O	HS USB Data2	NO
DATA3/UART4.CTSO/ GPIO.12	D7	VDDIO/DGND	Digital	I/O	HS USB Data3	NO
DATA4/GPIO.14	F8	VDDIO/DGND	Digital	I/O	HS USB Data4	NO
DATA5/GPIO.3	F11	VDDIO/DGND	Digital	I/O	HS USB Data5	NO
DATA6/GPIO.4	E8	VDDIO/DGND	Digital	I/O	HS USB Data6	NO
DATA7/GPIO.5	D9	VDDIO/DGND	Digital	I/O	HS USB Data7	NO
CP.IN	L4		Power	I/O	Charge pump input voltage	NO
CP.GND	J3		Power Gnd	I/O	Charge pump ground	NO

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Table 13. Terminal/Pin Functions (continued)

CP.CAPP	L5		Analog	I/O	Charge pump flying capacitor P	NO
CP.CAPM	L3		Analog	I/O	Charge pump flying capacitor M	NO
KPD.C0	B4	VDDIO/DGND	Open Drain	O	Keypad column 0	PU
KPD.C1	D2	VDDIO/DGND	Open Drain	O	Keypad column 1	PU
KPD.C2	E2	VDDIO/DGND	Open Drain	O	Keypad column 2	PU
KPD.C3	B2	VDDIO/DGND	Open Drain	O	Keypad column 3	PU
KPD.C4	C2	VDDIO/DGND	Open Drain	O	Keypad column 4	PU
KPD.C5	E4	VDDIO/DGND	Open Drain	O	Keypad column 5	PU
KPD.C6	E3	VDDIO/DGND	Open Drain	O	Keypad column 6	PU
KPD.C7	F4	VDDIO/DGND	Open Drain	O	Keypad column 7	PU
KPD.R0	H5	VDDIO/DGND	Digital	I	Keypad row 0	PU
KPD.R1	G4	VDDIO/DGND	Digital	I	Keypad row 1	PU
KPD.R2	H4	VDDIO/DGND	Digital	I	Keypad row 2	PU
KPD.R3	G5	VDDIO/DGND	Digital	I	Keypad row 3	PU
KPD.R4	J4	VDDIO/DGND	Digital	I	Keypad row 4	PU
KPD.R5	J8	VDDIO/DGND	Digital	I	Keypad row 5	PU
KPD.R6	G7	VDDIO/DGND	Digital	I	Keypad row 6	PU
KPD.R7	F5	VDDIO/DGND	Digital	I	Keypad row 7	PU
VBAT	K3		Power	I/O	Battery input voltage (Sense)	NO
CLKREQ	D8	VDDIO/DGND	Digital	I	Clock request line	PD
TEST.RESET	J9	VBAT/GND	Digital	I	Reset the device (except the state-machine)	PD
VPROG	H3		Analog	I	Reserved. Must be grounded.	NO
JTAG/TCK/BERCLK	F7	VDDIO/DGND	Digital	I	JTAG clock input	NO
GPIO.0/CD1/JTAG.TDO	L9	VDDIO/DGND	Digital	I/O	JTAG test output or GPIO0/card detection 1	PD
GPIO.1/CD2/JTAG.TMS	K9	VDDIO/DGND	Digital	I/O	JTAG test mode state or GPIO1/card detection 2	PD
GPIO.2/TEST1	G2	VDDIO/DGND	Digital	I	GPIO/Digital test pin	Programmable PD
VMMC1.IN	B1		Power	I	VMMC1 input LDO	NO
N/A	C3	N/A	N/A	N/A	N/A	N/A

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	1	2	3	4	5	6	7	8	9	10	11	
A	VMMC1.OUT	VINTANA2. OUT	VMODE2/ I2C.SR.SCL	AVSS4	DIR/GPIO.10	VPLLA3R.IN	VINT.IN	VPLL1.OUT	INT1	IO.1P8	VDD1.GND	A
B	VMMC1.IN	KPD.C3	I2C.CNTL. SCL	KPD.C0	VRTC.OUT	DATA0/ UART4.TXD	VINTDIG. OUT	DGND	SYSEN	VDD1.GND	VDD1.GND	B
C	VDAC.IN	KPD.C4	#N/A	I2C.CNTL. SDA	NXT/GPIO.11	DATA1/ UART4.RXD	DATA2/ UART4.RTSI	HFCLKIN	TESTV2	VDD1.L	VDD1.L	C
D	VINTANA1. OUT	KPD.C1	TEST	PWROK2/ 12C.SR.SDA	PWRON	UCLK	DATA3/ UART4. CTSO/ GPIO.12	CLKREQ	DATA7/ GPIO.5	VDD1.L	VDD1.OUT	D
E	VDAC.OUT	KPD.C2	KPD.C6	KPD.C5	BOOT0	STP/GPIO.9	NRESPWRON	DATA6/ GPIO.4	VDD1.IN	VDD1.IN	VDD1.IN	E
F	VAUX12S.IN	ADCIN0	AVSS1	KPD.C7	KPD.R7	BOOT1	JTAG.TCK/ BERCLK	DATA4/ GPIO.14	AVSS3	CLKEN	DATA5/ GPIO.3	F
G	VAUX2.OUT	GPIO.2/ TEST1	REGEN	KPD.R1	KPD.R3	32KCLKOUT	KPD.R6	MSECURE	BKBAT	VREF	32KXOUT	G
H	VIO.OUT	TESTV1	VPROG	KPD.R2	KPD.R0	AVSS2	STARTADC	NRESWARM	VDD2.OUT	AGND	32KXIN	H
J	VIO.GND	VIO.GND	CP.GND	KPD.R4	VINTUSB1P5. OUT	VINTUSB1P8. OUT	ID	KPD.R5	TEST.RESET	VDD2.GND	VDD2.GND	J
K	VIO.L	VIO.IN	VBAT	NSLEEP1	VBUS	VBAT.USB	GND_AGND	HFCLKOUT	GPIO.1/CD2/ JTAG.TMS	VDD2.IN	VDD2.L	K
L	VIO.L	VIO.IN	CP.CAPM	CP.IN	CP.CAPP	VUSB.3P1	DP/UART3. RXD	DN/UART3. TXD	GPIO.0/CD1/ JTAG.TD0	VDD2.IN	VDD2.L	L
	1	2	3	4	5	6	7	8	9	10	11	

SWCS048-009

Figure 9. Ball Placement (Top View)

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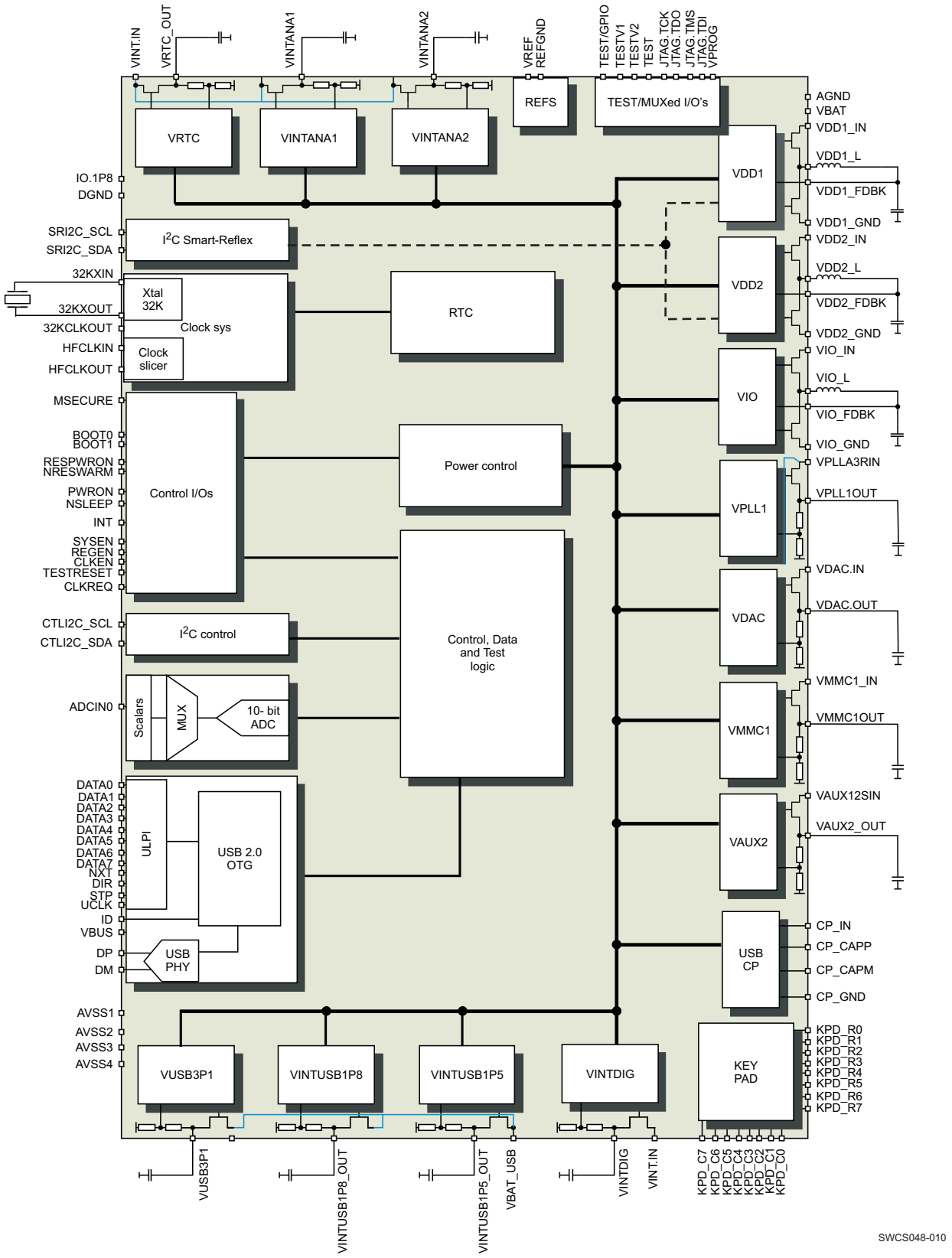

Figure 10. Functional Block Diagram

DETAILED DESCRIPTION

CLOCK SYSTEM

Figure 11 shows the TPS65921 clock overview.

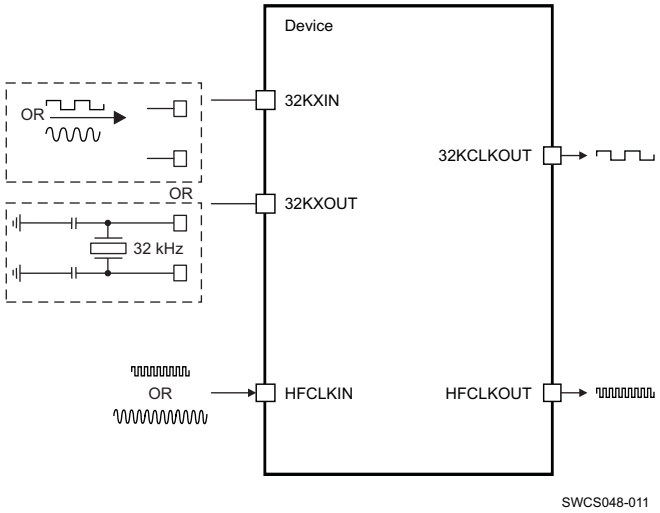

Figure 11. TPS65921 Clock Overview

The TPS65921 accepts two sources of high-stability clock signals:

- 32KXIN/32KXOUT: on-board 32-kHz crystal oscillator (optionally, an external 32-kHz input clock can be provided)
- HFCLKIN: an external high-frequency clock (19.2, 26, or 38.4 MHz)

The TPS65921 has the capability to provide:

- 32KCLKOUT digital output clock
- HFCLKOUT digital output clock with the same frequency as HFCLKIN input clock

32-kHz OSCILLATOR

It is possible to use the 32-kHz input clock with either an external crystal or clock source. There are four configuration, one with the external crystal and three without.

- An external 32.768-kHz crystal connected on the 32KXIN / 32KXOUT balls. This configuration is available for the master mode only.
- A square- or sine-wave input can be applied to the 32KXIN pin with amplitude of 1.85 or 1.8 V. The 32KXOUT pin can be driven to a dc value of the square- or sine-wave amplitude divided by 2. This configuration is recommended if a large load is applied on the 32KXOUT pin.
- A square- or sine-wave input can be applied to the 32KXIN pin with amplitude of 1.85 or 1.8 V. The 32KXOUT pin can be left floating. This configuration is used if no charge is applied on the 32KXOUT pin.
- The oscillator is in bypass mode and a square-wave input can be applied to the 32KXIN pin with amplitude of 1.8 V. The 32KXOUT pin can be left floating. This configuration is used if the oscillator is in bypass mode (default configuration in Slave mode).

Figure 12 shows the block diagram for the 32.768-kHz clock output.

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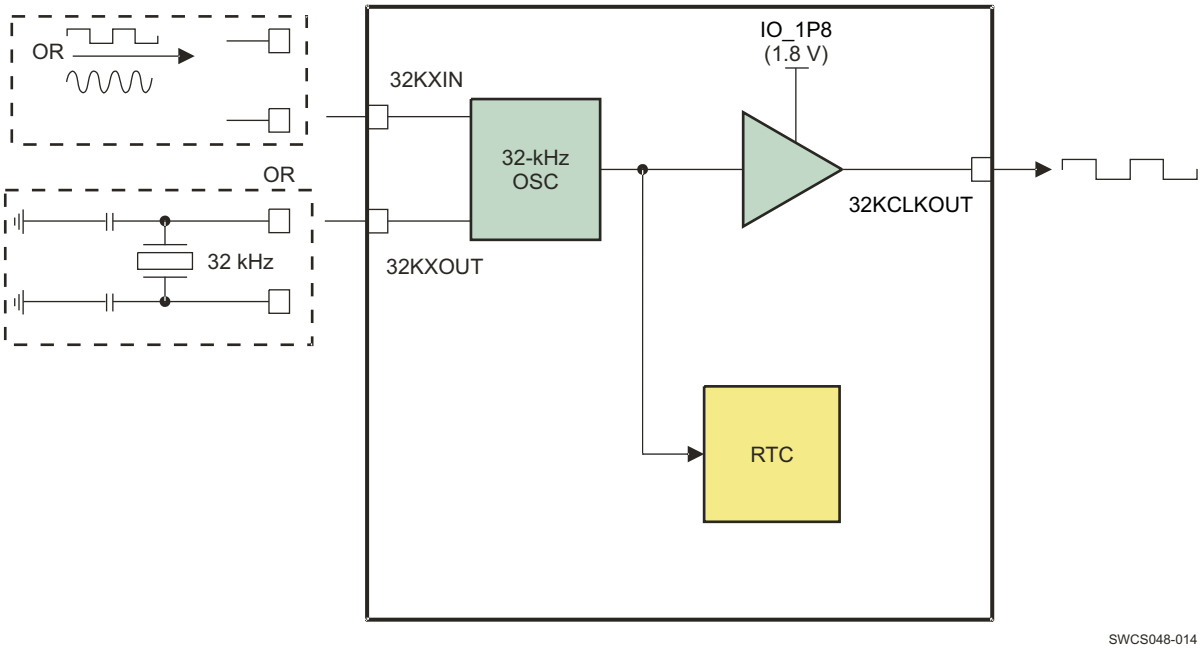

Figure 12. 32.768-kHz Clock Output Block Diagram

The TPS65921 device has an internal 32.768-kHz oscillator connected to an external 32.768-kHz crystal through the 32KXIN/32KXOUT balls or an external digital 32.768-kHz clock through the 32KXIN input (see Figure 12). The TPS65921 device also generates a 32.768-kHz digital clock through the 32KCLKOUT pin and can broadcast it externally to the application processor or any other devices. The 32KCLKOUT clock is broadcast by default in the TPS65921 active mode but can be disabled if it is not used.

The 32.768-kHz clock (or signal) is also used to clock the RTC (real-time clock) embedded in the TPS65921. The RTC is not enabled by default. It is up to the host processor to set the correct date and time and to enable the RTC functionality.

The 32KCLKOUT output buffer can drive several devices (up to 40-pF load). At start-up, the 32.768-kHz output clock (32KCLKOUT) must be stabilized (frequency/duty cycle) prior to the signal output. Depending on the start-up condition, this may delay the start-up sequence.

CLOCK SLICER

Figure 13 shows the clock slicer block diagram.

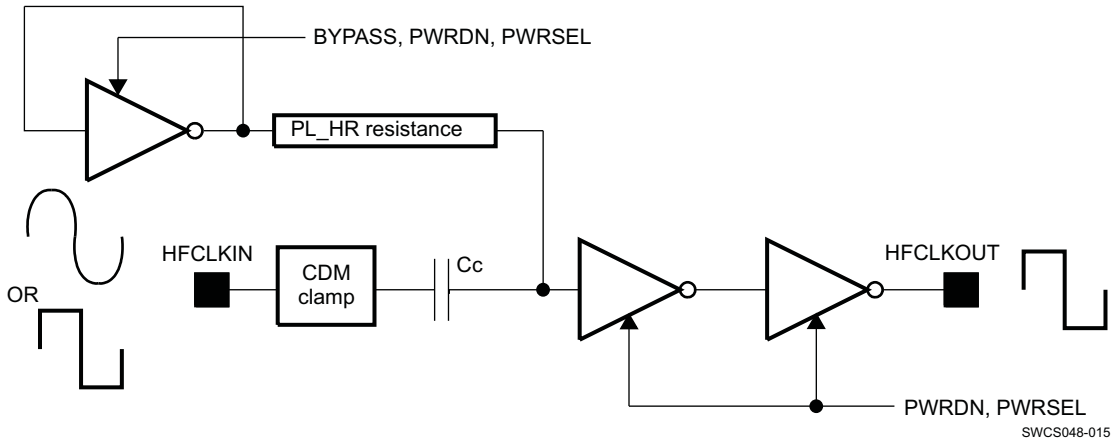

Figure 13. Clock Slicer Block Diagram

The clock slicer is disabled by default and enabled when the CLKEN pad is high. The slicer transforms the HFCLKIN clock input signal into a squared clock signal used internally by the TPS65921 device and also outputs it for external use. The HFCLKIN input signal can be:

- A sinusoid with peak-to-peak amplitude varying from 0.3 to 1.45 V
- A square clock signal of amplitude 1.85 V maximum. In the case of a square clock signal, the slicer is configured in bypass or power-down mode. If a square-wave input clock is provided, it is recommended to switch the block to bypass mode when possible to avoid loading the clock.

The HFCLKIN input clock frequency must be 19.2, 26, or 38.4 MHz.

Four different modes are programmable by register. By default, the slicer is in high-performance application mode:

- Bypass mode (BP): In BP mode, which overrides all the other modes, the input signal is directly connected to the output through some buffers. The input is a rail-to-rail square wave.
- Power-down mode (PD): During PD mode, the cell does not consume any current if bypass mode is not active.
- Low-power application mode (LP): In LP mode, the input sine wave is converted to a CMOS signal (square wave) with low power consumption.
- High-performance application mode (HP): In HP mode, the input sine wave is converted to a CMOS signal (square wave). It has lower duty cycle degradation and lower input-to-output delay in comparison to the low-power mode, but it consumes more current. The drive of the squaring inverter is increased by connecting additional inverters in parallel. Details can be found in the clock slicer electrical characteristics table.

Figure 14 shows the HFCLKIN clock distribution.

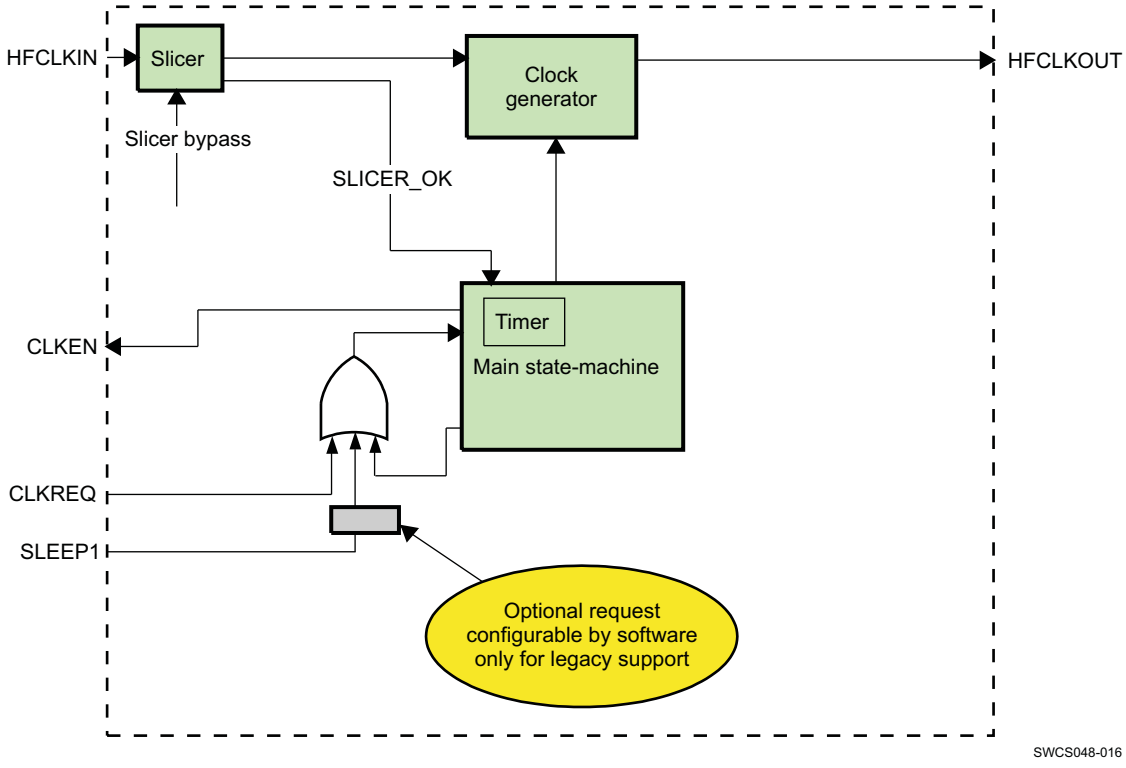

Figure 14. HFCLKIN Clock Distribution

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When a device needs a clock signal other than 32.768 kHz, it makes a clock request and activates the CLKREQ pin. As a result, the TPS65921 device immediately sets CLKEN to 1 to warn the clock provider in the system about the clock request and starts a timer (maximum of 10 ms and uses the 32.768-kHz clock). Once the timer expires, the TPS65921 device opens a gated clock, the timer automatically reloads the defined value and a high-frequency output clock signal is available through the HFCLKOUT pin. The output drive of HFCLKOUT is programmable (low drive (MISC_CFG[CLK_HF_DRV] = 0) maximum load 20 pF, high drive (MISC_CFG[CLK_HF_DRV] = 1) maximum load 30 pF), by default it is programmed to support Low Drive.

CLKREQ, when enabled, has a weak pulldown resistor to support the wired-OR clock request.

Figure 15 shows an example of the wired-OR clock request.

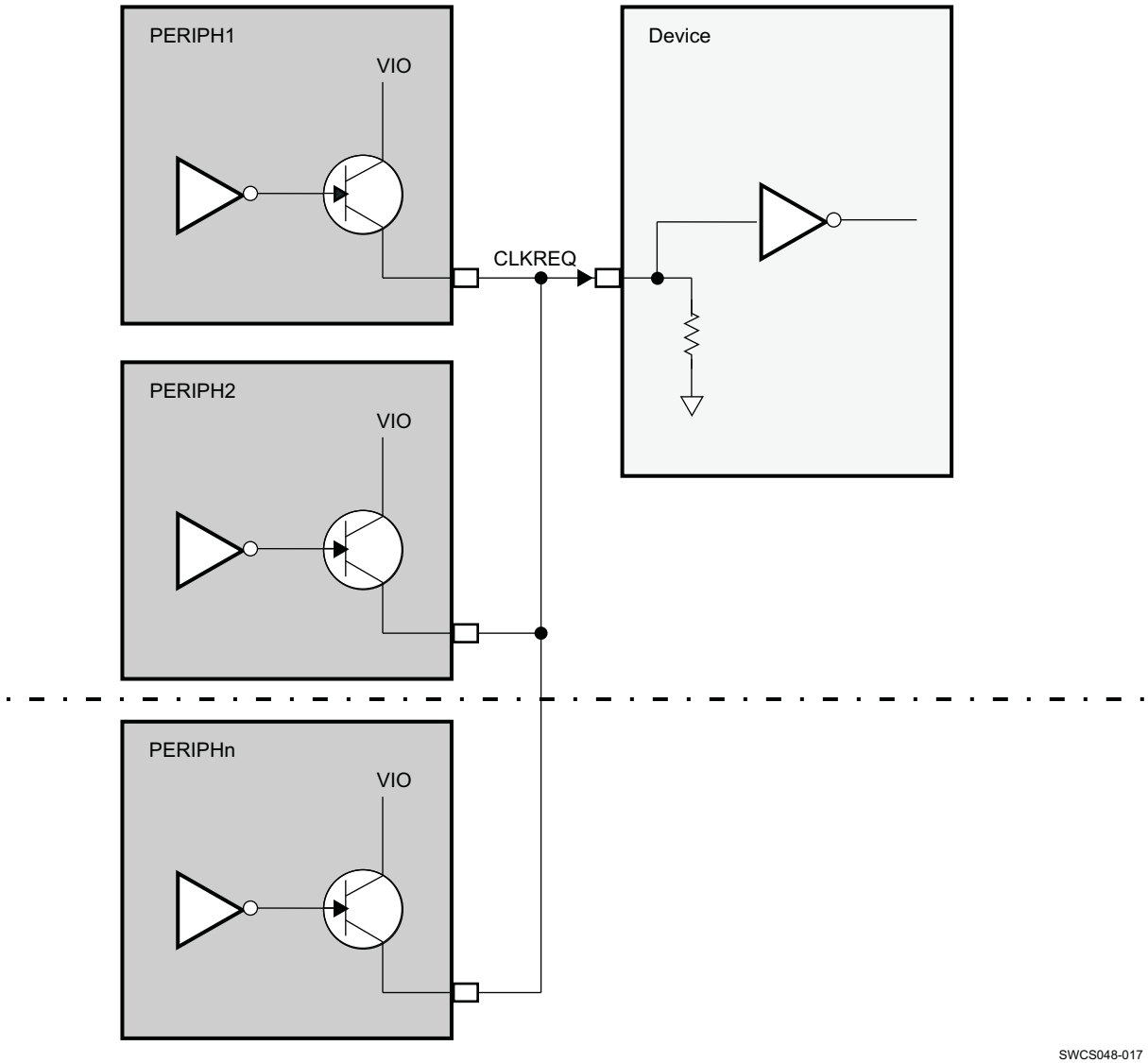

Figure 15. Example of Wired-OR Clock Request

The timer default value must be the worst case (10 ms) for the clock providers. For legacy or workaround support, the NSLEEP1 signal can also be used as a clock request even if it is not its primary goal. By default, this feature is disabled and must be enabled individually by setting the register bits associated with each signal.

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POWER PATH

Step-Down Converters

Depending on the system requirements, and also to optimize mean consumption, three operating modes are allowed for each step-down converter:

- Off/power-down mode: Output voltage is not maintained, and power consumption is null
- Active: DCDC can deliver its nominal output voltage with a full load current capability.
- Sleep: The nominal output voltage is maintained with low power consumption, but also with a low load-current capability.

The SMPS operates with three modulation schemes:

- Light pulse frequency modulation (PFM)
- Pulse skipping mode (PSM)
- Continuous pulse-width modulation (PWM)

Each DCDC, all of which have the same electrical characteristics, has an integrated RC oscillator. The use of these RC oscillators is configurable through register bits, and by default the RC oscillator of VDD1 is used for all DCDC.

LDO

The VPLL1 programmable LDO regulator is high-PSRR, low-noise, linear regulator used for the host processor PLL supply.

The VDAC programmable LDO regulator is a high-PSRR, low-noise, linear regulator that powers the host processor dual-video DAC. It is controllable with registers through I^2C and can be powered down.

The VMMC1 LDO regulator is a programmable linear voltage converter that powers the MMC slot. It includes a discharge resistor and over-current protection (short circuit). This LDO regulator can also be turned off automatically when the MMC card extraction is detected (through one dedicated GPIO). The VMMC1 LDO can be powered through an independent supply other than the battery; for example, a charge pump. In this case, the input from the VMMC1 LDO can possibly be higher than the battery voltage.

The VAUX2 general-purpose LDO regulator powers the auxiliary devices.

The VRRTC voltage regulator is a programmable, LDO, linear voltage regulator supplying (1.5 V) the embedded RTC (32.768-kHz oscillator) and dedicated I/Os of the digital host counterpart. The VRRTC regulator is also the supply voltage of the power-management digital state-machine. The VRRTC regulator is supplied from the UPR line, switched on by the main battery. The VRRTC output is present as long as a valid energy source is present. The VRRTC line is supplied by an LDO when VBAT > 2.7 V, and a clamp circuit when VBAT < 2.7 V.

The VINTDIG LDO regulator supplies the TPS65921 digital blocks.

To supply the TPS65921 analog blocks, there are two LDOs: VINTANA1 (1.5 V) and VINTANA2 (2.75 V/2.5 V). The 2.5-V setting is selected when the battery voltage falls below 3.0 V.

The VUSB3V1 internal LDO regulator powers the USB PHY, charger detection, and OTG of the USB subchip inside the TPS65921 device.

It can take its power from two possible sources:

- VBAT.USB (only for high battery voltages)
- VBUS (only in low-power mode)

See Charge-pump section for more details.

The USB standard requires data lines to be biased with pullups biased from a > 3.0 V supply, USB PHY cannot directly operate from VBAT.USB for battery voltages lower than 3.3 V.

In such case, VBUS should be supplied by a boosted voltage to ensure enough overhead for USB LDO operation. An internal charge pump (whose output is connected to VBUS) can be used for this purpose.

To select between these two power sources, a power mux is connected to the VUSB3V1 LDO supply.

The VUSB1V8 and VUSB1V5 internal LDO regulators power the USB subchip inside the TPS65921 device.

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The short-circuit current for the LDOs and DCDCs in the TPS65921 device is approximately twice the maximum load current. In certain cases when the output of the block is shorted to ground, the power dissipation can exceed the 1.2 W requirement if no action is taken. A short-circuit protection scheme is included in the TPS65921 device to ensure that if the output of an LDO or DCDC is short-circuited, then the power dissipation does not exceed the 1.2 W level.

The three USB LDOs VUSB3V1, VUSB1V8, and VUSB1V5 are included in this short circuit protection scheme which monitors the LDO output voltage at a frequency of 1 Hz, and generates an interrupt when a short circuit is detected.

The scheme compares the LDO output voltage to a reference voltage and detects a short circuit if the LDO voltage drops below this reference value (0.5 V or 0.75 V programmable). In the case of the VUSB3V1 and VUSB1V8 LDOs, the reference is compared with a divided down voltage (1.5 V typical).

If a short circuit is detected on VUSB3V1, then the power subchip FSM switches this LDO to sleep-mode.

If a short circuit is detected on VUSB1V8 or VUSB1V5, then the power subchip FSM switches the relevant LDO off.

Power Reference

The bandgap voltage reference is filtered (RC filter), using an external capacitor connected across the VREF output and an analog ground (REFGND). The VREF voltage is scaled, distributed, and buffered inside the device. The bandgap is started in fast mode (not filtered) and is set automatically by the power state-machine in slow mode (filtered, less noisy) after switch on.

Power Use Cases

The TPS65921 device has two modes:

- Master: The TPS65921 device decides to power up or down the system and control the other power ICs in the system with the SYSEN output.
- Slave: The TPS65921 device is controlled by another power IC with a digital signal on the PWRON input. There is no battery management in slave mode.

The modes corresponding to BOOT0–BOOT1 combination value are:

NAME	DESCRIPTION	BOOT0	BOOT1
MC021(1)	Master_C021_Generic 10	1	0
SC021	Slave_C021_Generic 11	1	1

(1) Boot mode for OMAP3430 is c021 Master boot mode.

Process modes define:

- The boot voltage for the host core
- The boot sequence associated with the process
- The DVFS protocol associated with the process

MODE	C021.M
Boot core voltage	1.2 V
Power sequence	VIO followed by VPLL1, VDD2, VDD1
DVFS protocol	SmartReflex interface (I^2C high speed)

Regulator states depending on use cases:

REGULATOR	MODE: C021 (MASTER/SLAVE)			
	BACKUP	WAIT ON	SLEEP NO LOAD	ACTIVE NO LOAD
VAUX2	OFF	OFF	OFF	OFF
VMMC1	OFF	OFF	OFF	OFF
VPLL1	OFF	OFF	SLEEP	ON
VDAC	OFF	OFF	OFF	OFF

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VINTANA1	OFF	OFF	SLEEP	ON
VINTANA2	OFF	OFF	SLEEP	ON
VINTDIG	OFF	OFF	SLEEP	ON
VIO	OFF	OFF	SLEEP	ON
VDD1	OFF	OFF	SLEEP	ON
VDD2	OFF	OFF	SLEEP	ON
VUSB1V5	OFF	OFF	OFF	OFF
VUSB1V8	OFF	OFF	OFF	OFF
VUSB3V1	OFF	OFF	SLEEP	ON

Power Timing

Sequence start is a symbolic internal signal to ease the description of the power sequences and occurs according to the different events detailed in Figure 16.

Sequence start timing depends on the TPS65921 starting event. If the starting event is:

- Main battery insertion, event time is 1.126 ms (time to set up internal LDO and relax internal reset)
- VBUS insertion, event time is 25 cycles of 32k

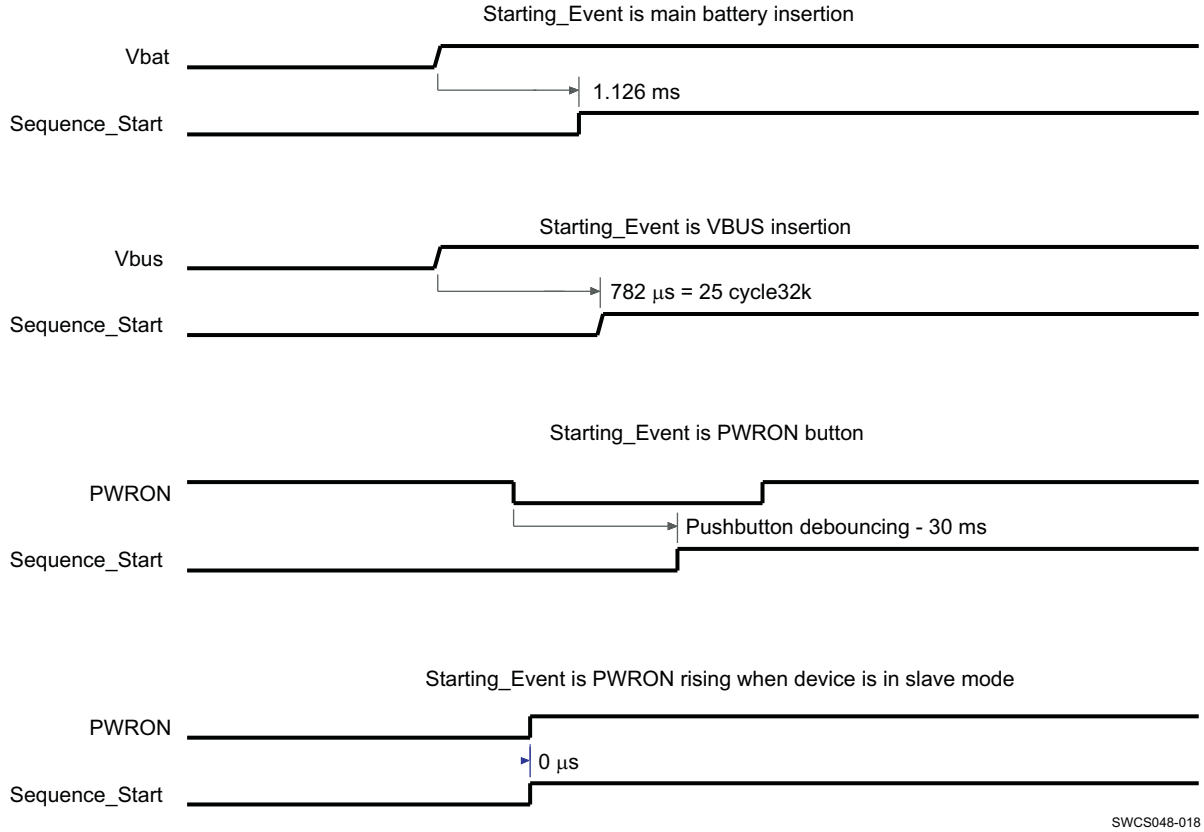

Figure 16. Timings Before Sequence Start

Switch On In MASTER_C021_GENERIC Mode

Figure 17 describes the timing and control that must occur in Master_C021_Generic mode. Sequence_Start is a symbolic internal signal to ease the description of the power sequences and occurs according to the different events detailed in Figure 16.

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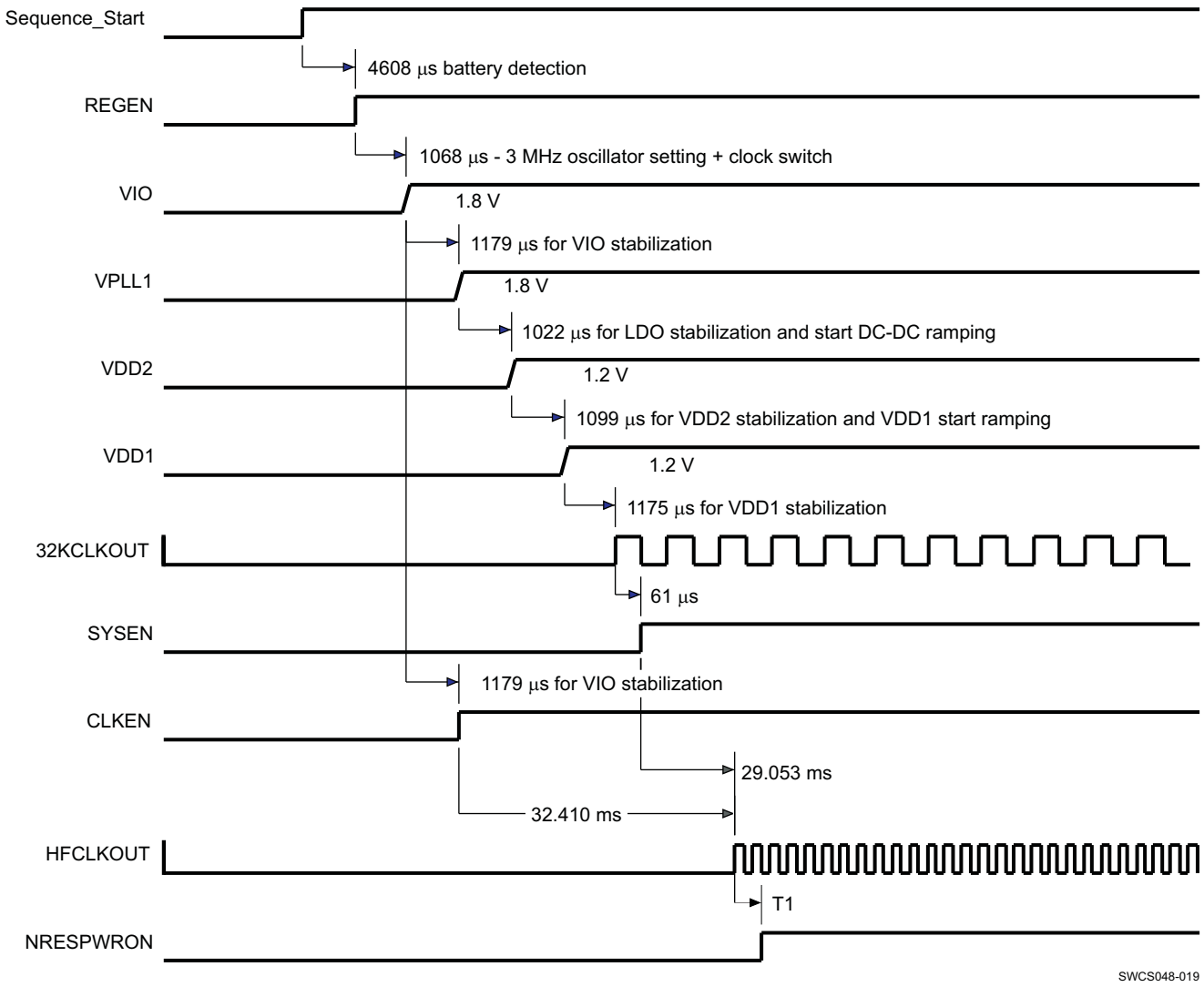

Figure 17. Timings—Switch On in Master_C021_Generic Mode

PARAMETER		MIN	MAX	UNIT
T1		10	11	32k clock cycles

Switch On In SLAVE_C021_GENERIC Mode

Figure 18 describes the timing and control that must occur in Slave_C021_Generic mode. Sequence_Start is a symbolic internal signal to ease the description of the power sequences and occurs according to the different events detailed in Figure 16.

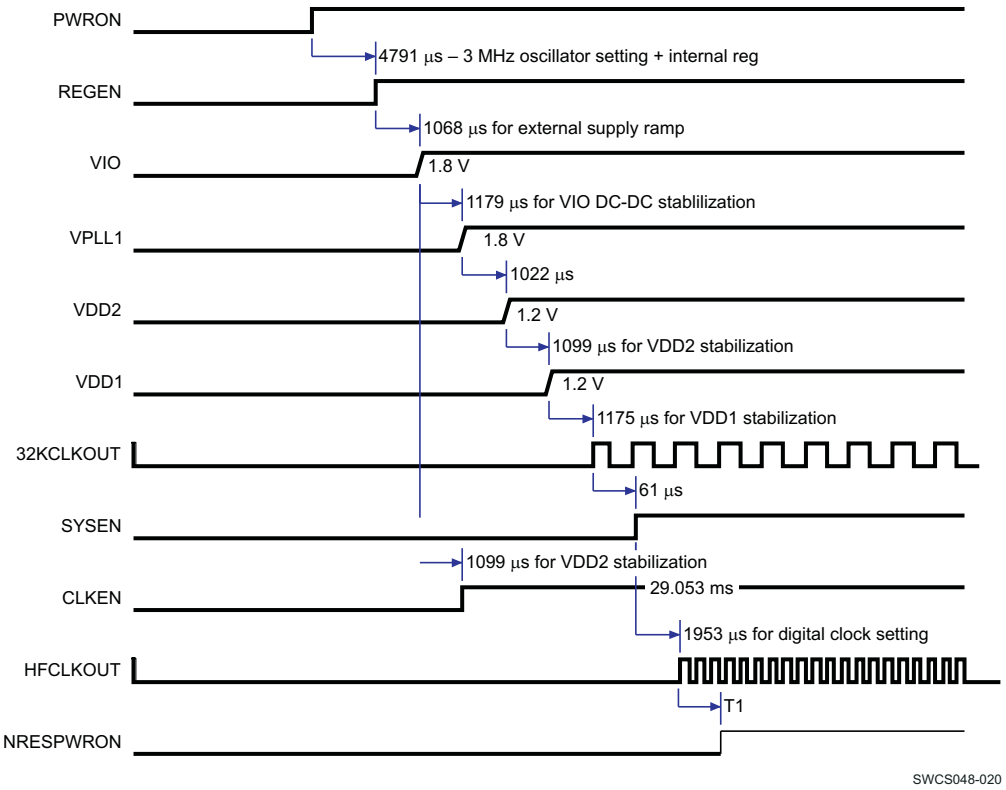

Figure 18. Timings—Switch On in Slave_C021_Generic Model

PARAMETER		MIN	MAX	UNIT
T1		10	11	32k clock cycles

Switch-Off Sequence

This section describes the signal behavior required to switch off the system.

Switch-Off Sequence In Master Modes

Figure 19 describes the timing and control that occur during the switch-off sequence in master modes.

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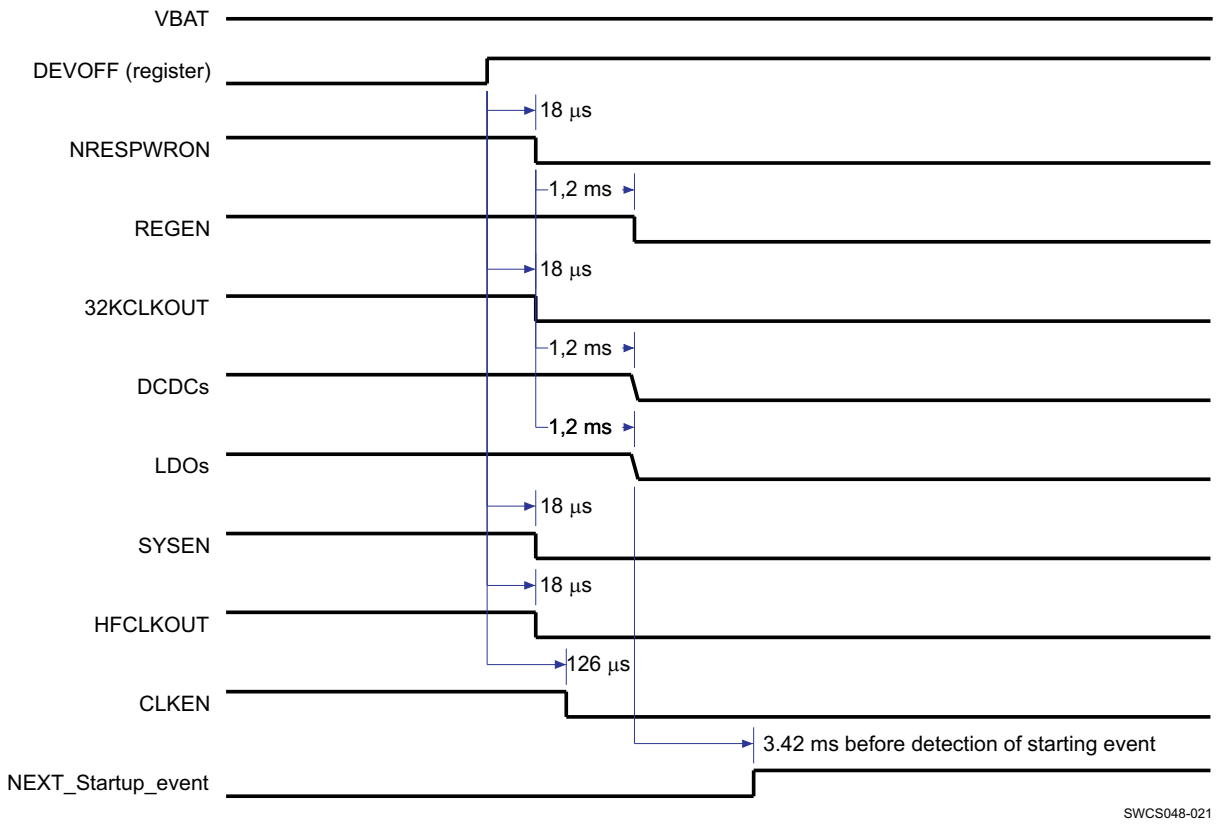

NOTE: All of the above timings are the typical values with the default setup (depending on the resynchronization between power domains, state machinery priority, etc.).

Figure 19. Switch-Off Sequence in Master Modes

In case the value of the HF clock is different from 19.2 MHz (with HFCLK_FREQ bit field values set accordingly inside the CFG_BOOT register), then the delay between DEVOFF and NRESPWRON/CLK32KOUT/SYSEN/HFCLKOUT is divided by 2 (meaning around 9 µs). This is due to the internal frequency used by POWER STM switching from 3 MHz to 1.5 MHz in case the value of the HF clock is 19.2 MHz.

The DEVOFF event is the PWRON falling edge in slave mode and the DEVOFF internal register write in master mode.

Switch-Off Sequence in Slave Mode

Figure 20 describes the timing and control that occur during the switch off-sequence in slave mode.

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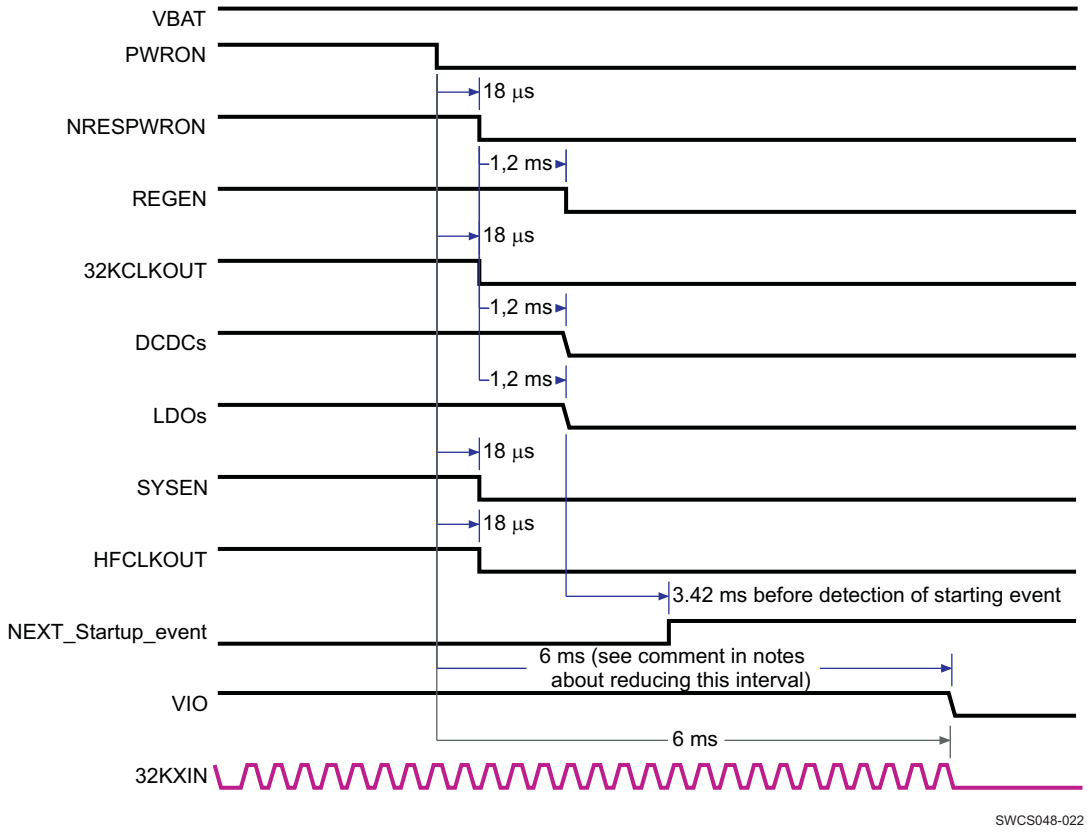

NOTE: All of the above timings are the typical values with the default setup (depending on the resynchronization between power domains, state machinery priority, etc.). If necessary, the 6-ms period to maintain VIO and 32KXIN after PWRON goes low can be reduced to 150 µs.

Figure 20. Switch-Off Sequence in Slave Mode

In case the value of the HF clock is different from 19.2 MHz (with HFCLK_FREQ bit field values set accordingly inside the CFG_BOOT register), then the delay between DEVOFF and NRESPWRON/CLK32KOUT/SYSEN/HFCLKOUT is divided by 2 (meaning around 9 µs). This is due to the internal frequency used by POWER STM switching from 3 MHz into 1.5 MHz in case the value of the HF clock is 19.2 MHz.

Charge Pump

The charge pump generates a 5.0-V (nominal) power supply voltage from battery to the VBUS CP.OUT/VUSB.IN pin. The input voltage range is 2.7 to 4.5 V for the battery voltage. The charge pump operating frequency is 1 MHz.

The charge pump tolerates 6 V on VBUS when it is in power down mode. The charge pump integrates a short-circuit current limitation at 450 mA.

Figure 21 shows the charge pump.

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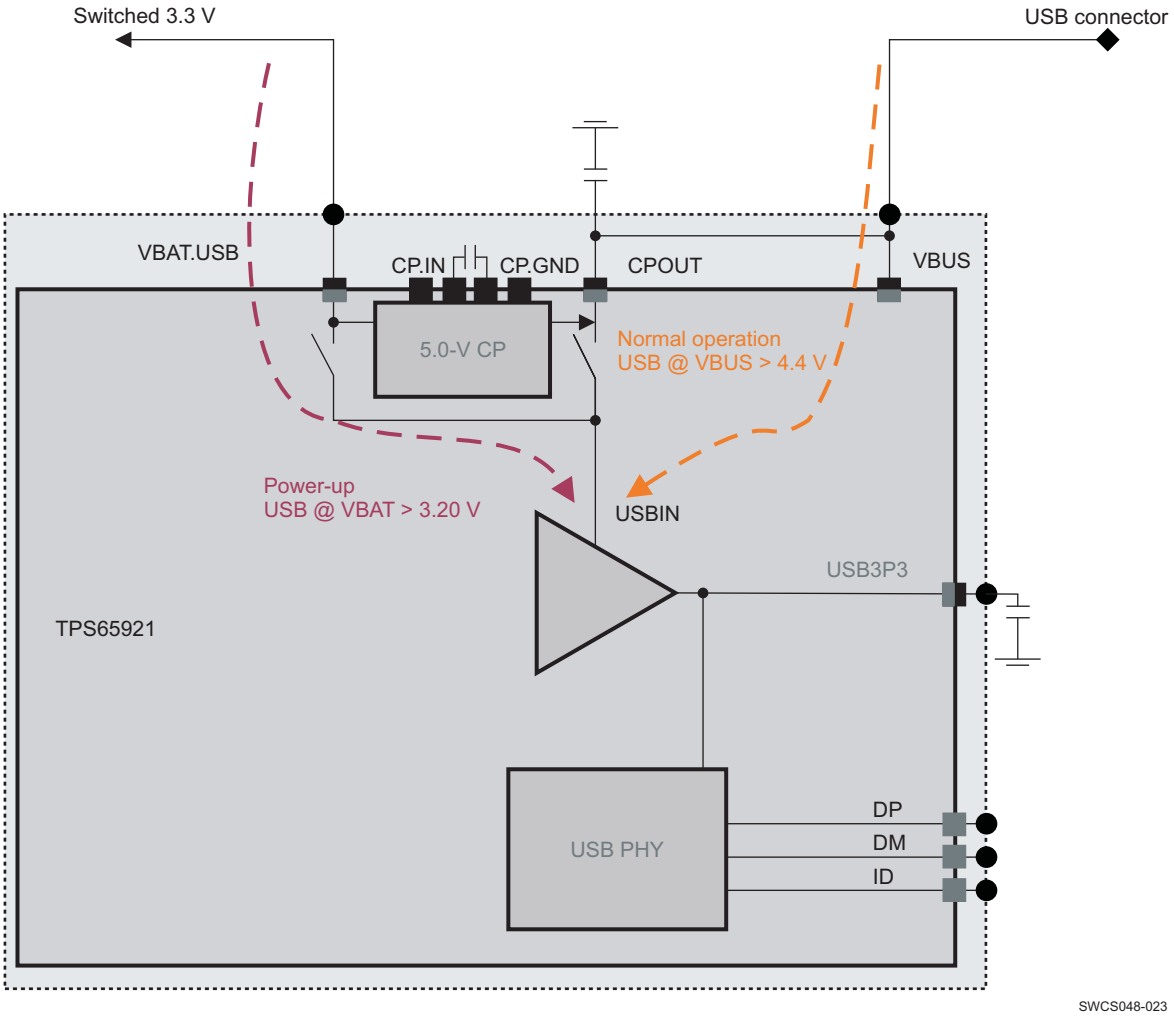

Figure 21. General Overview of the Charge Pump and Its Interfaces

It can be used to supply USB 3.1 V LDO when battery voltage is lower than this LDO VBATmin voltage (see electrical characteristics).

USB Transceiver

The TPS65921 device includes a USB OTG transceiver that support USB 480 Mbps HS, 12 Mbps FS, and USB 1.5 Mbps LS through a 4-pin UTMI+ ULPI.

It also includes a module covering Battery Charging Specification v1.0. Figure 22 shows the USB 2.0 PHY highlight block diagram.

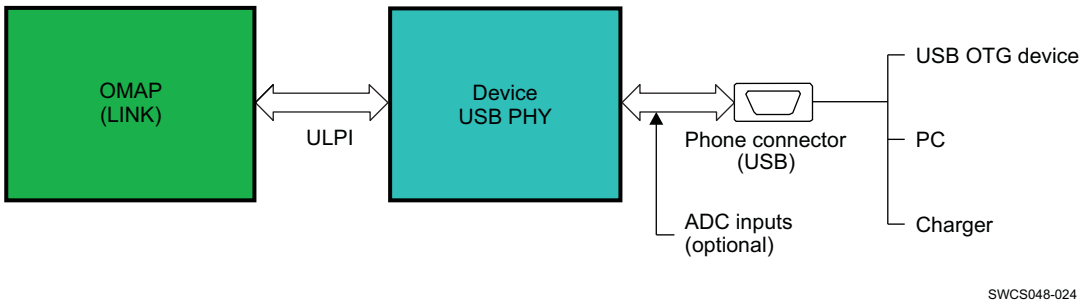

Figure 22. USB 2.0 PHY Highlight

Figure 23 shows the USB system application schematic.

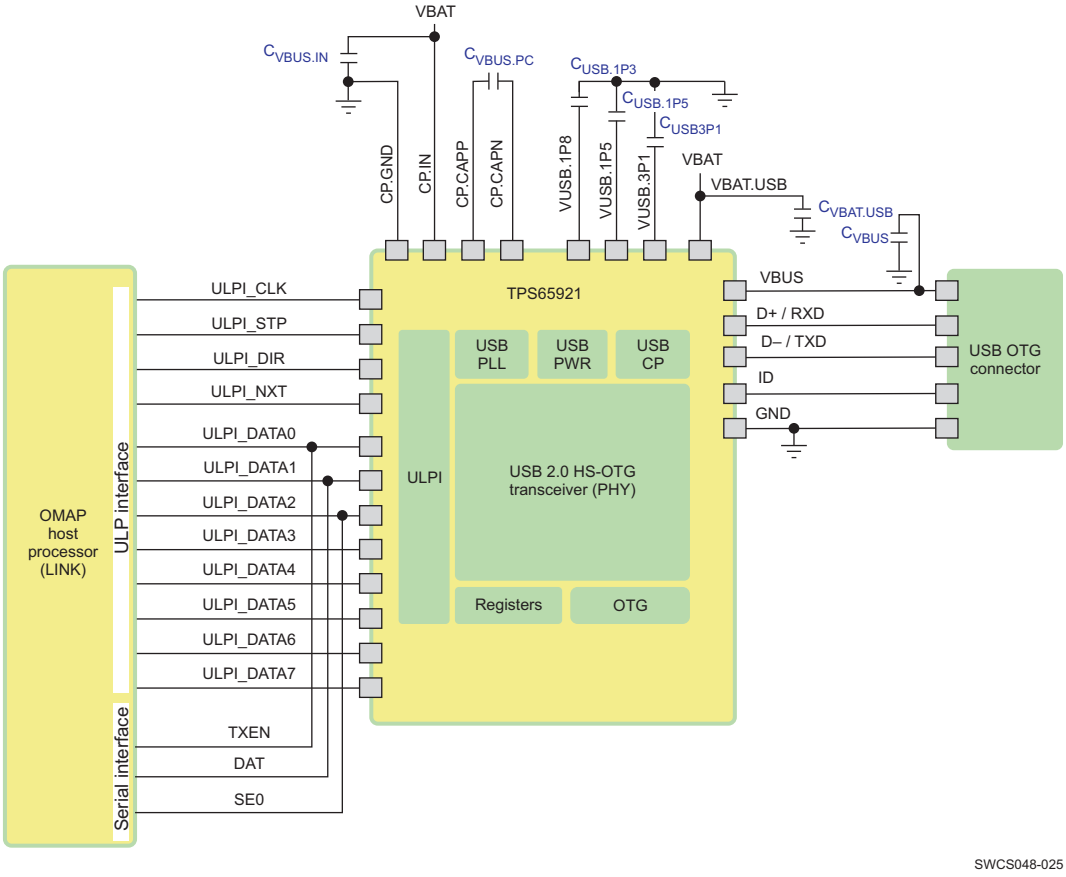

Figure 23. USB System Application Schematic

PHY

The PHY is the physical signaling layer of the USB 2.0. It contains all the drivers and receivers required for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through a standard digital interface called the universal transceiver macro cell interface (UTMI).

The transmitters and receivers inside the PHY are classified into two main classes:

- The FS and LS transceivers. These are the legacy USB1.x transceivers.
- The HS transceivers

To bias the transistors and run the logic, the PHY also contains reference generation circuitry consisting of:

- A DPLL, which does a frequency multiplication to achieve the 480-MHz low-jitter lock necessary for USB, and also the clock required for the switched capacitor resistance block.
- A switched capacitor resistance block used to replicate an external resistor on chip.

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

Apart from this, the PHY also contains circuitry that protects it from an accidental 5 V short on the DP and DM lines.

LS/FS Single-Ended Receivers

In addition to the differential receiver, there is a single-ended receiver (SE–, SE+) for each of the two data lines D+/–. The main purpose of the single-ended receivers is to qualify the D+ and D– signals in the FS/LS modes of operation.

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LS/FS Differential Receiver

A differential input receiver (RX) retrieves the LS/FS differential data signaling. The differential voltage on the line is converted into digital data by a differential comparator on DP/DM. This data is then sent to a clock and data recovery circuit, which recovers the clock from the data. In an additional serial mode, the differential data is directly output on the RXRCV pin.

LS/FS Transmitter

The USB transceiver (TX) uses a differential output driver to drive the USB data signal D+/– onto the USB cable. The outputs of the driver support 3-state operation to achieve bidirectional half-duplex transactions.

HS Differential Receiver

The HS receiver consists of the following blocks:

- A differential input comparator to receive the serial data
- A squelch detector to qualify the received data
- An oversampler-based clock data recovery scheme followed by a NRZI decoder, bit unstuffing, and serial-to-parallel converter to generate the UTMI DATAOUT

HS Differential Transmitter

The HS transmitter is always operated on the UTMI parallel interface. The parallel data on the interface is serialized, bit-stuffed, NRZI-encoded, and transmitted as a DC output current on DP or DM depending on the data. Each line has an effective 22.5-Ω load to ground, which generates the voltage levels for signaling.

A disconnect detector is also part of the HS transmitter. A disconnect on the far end of the cable causes the impedance seen by the transmitter to double, thereby doubling the differential amplitude seen on the DP and DM lines.

UART Transceiver

In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver.

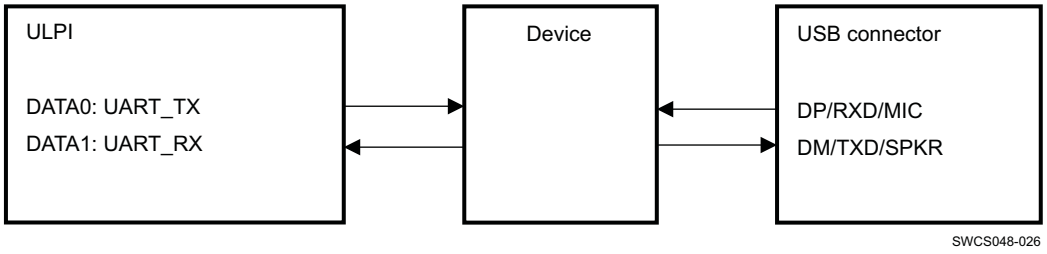

Figure 24. USB UART Data Flow

The OTG block integrates three main functions:

- The USB plug detection function on VBUS and ID
- The ID resistor detection
- The VBUS level detection

CHARGER DETECTION

To support Battery Charging Specification v1.1 [BCS v1.1], a charger detection module is included in the TPS65921 USB module.

The detection mechanism aims distinguishing several types of power sources that can be connected on VBUS line:

- Dedicated charger port
- Standard host port
- Charging host port

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The hardware includes:

- A dedicated voltage referenced pullup on DP line
- A dedicated current controlled pulldown on DM line
- A detection comparator on DM line
- A control/detection state-machine including timers

Additional circuitry is added on DP/DM respectively for data line symmetry (required for HS operation) and for possible future extension

ID pin status detection (as defined per OTG v1.3 standard) and DP/DM single-ended receivers (as defined per USB v2.0 standard) are also used to determine the type of device plugged on the USB connector.

For details on the detection mechanism, refer to [BCS v1.1] (1).

The charging detection feature has two modes (description of each mode follows):

1. Software CTL mode: Software has direct control of current source and USB charger detection comparator on DP/DM (enabled when USB_SW_CTRL_EN=1) using USB_CHRG_CTRL registers bits.
2. Software FSM mode: Software can start and stop USB charger detection state-machine.

For both modes, DPPULLDOWN and DMPULLDOWN bits in OTG_CTRL register are 1 by default. This can cause errors in charger detection. Therefore, both bits must be cleared to 0 before software begins charger detection sequence.

1- Software CTL Mode (Manual detection):

When in this mode the charger detection circuitry is fully under control of software. Refer to POWER_CONTROL register bits as to how to control the detection circuitry.
Conditions:

- The TPS65921 device is powered and is in active mode.
- USB_SW_CHRG_CTRL_EN = 1, register bit set by the software
- USB_CHG_DET_EN_SW = 1, register bit set by the software

Control the USB_SW_CHRF_CTRL register to achieve charger detection.

2- Software FSM Mode (Automatic detection):

The TPS65921 also supports automated battery charger detection through the USB battery charger detection FSM in Figure 25 while the chip is in active mode. This mode is set by software using the SW_USB_DET bit. When in this mode, the automated charger detection finite state-machine (FSM) is enabled. Refer to the state-machine diagram for details.
Conditions:

- The TPS65921 device is powered and is in active mode.
- USB_HW_CHRG_DET_EN = 1

See the Register Map for more details.

The TPS65921 device also supports automated data contact detection in the FSM through the DATA_CONTACT_DET_EN bit which should be set at the same time as SW_USB_DET above, before setting SW_CONTROL bit. This enables a block of the FSM, which performs data contact detect for a maximum of DCD_TIMEOUT before automatically skipping to charger detection.

See Figure 25,USB Battery Charger FSM, for details of how context is stored if SW_CONTROL bit is set while in software FSM mode.

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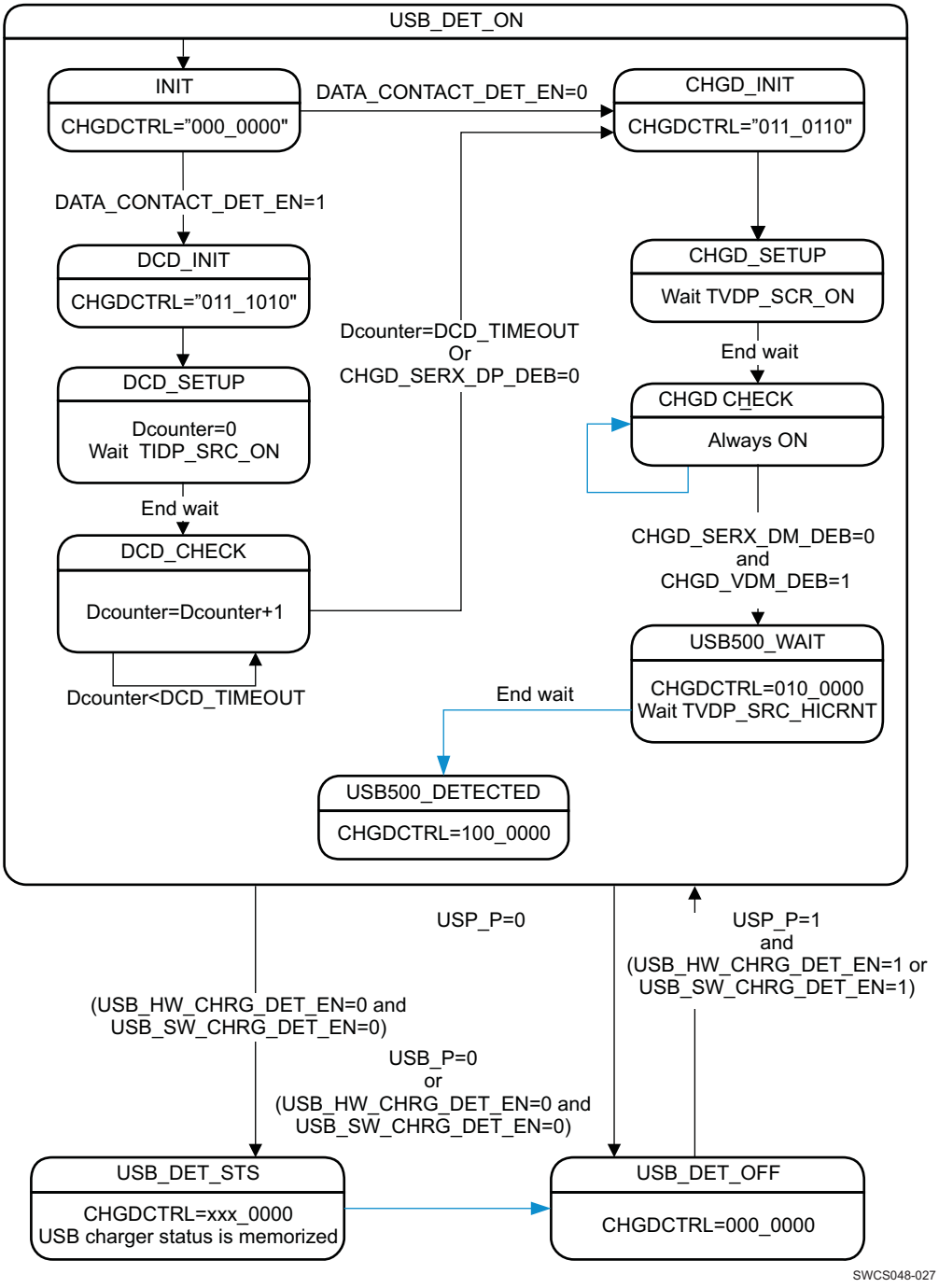

Figure 25. USB Battery Charger Detection FSM

USB charger detection status bit definition:

- USBVBUS_PRES: Detect presence of valid VBUS. Comparator output is debounced for DEBVBUS_TIME (minimum 10 ms) on CKCHG and generates a USB_P signal. USB_P is computed only if a battery presence is detected.
- USBCHRG_PRES: Detect presence of USB charger on DP/DM. The feature is enabled through the USB_DET_EN signal, then USBPHY performs checks on DP/DM and return status USB_DET_RESULT:
  - 1 : USB 500-mA charger is detected.
  - 0 : USB 100-mA charger is detected.

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- USB_DET_STATUS: 500-mA/100-mA USB charger detect presence comparator output is debounced during DEBUSBCHG_TIME (minimum 20 ms) on CKCHG, debounced signal is USB_DET_RESULT (set to 1 in case of 500-mA charger)
- Two signals are the result of the charger detection state machine:
  - USB100_P: Valid 100-mA charger (VBUS supplier) is detected.
  - USB500_P: Valid 500-mA charger (USB charger) is detected.

USB Battery Charger FSM

The FSM uses the control signals CHGDCTRL[6:0] described below to control and observe battery charger detection.

When the SW_CONTROL bit is set to 1, the current context of the FSM and the state of charger detection is latched in POWER_CONTROL register bits HWDETECT, DP_VSRC_EN, VDAT_DET, and DET_COMP, after which FSM control signals CHGDCTRL[6:0] are ignored, and charger detection hardware and the CHGR_DET pin are controlled by the software.

The CHGD_IDP_SRC_EN bit is not latched when the SW_CONTROL bit is set (for example, if the FSM is performing data-contact detection at the time the SW_CONTROL is set to 1, the CHGD_IDP_SRC_EN bit is unchanged — its default value is 0).

FSM Control Signals

Table 14. USB Charger Detect FSM I/O Control Signals

CONTROL SIGNAL	CONTROL SIGNAL	DESCRIPTION	TYPE
Bit(6)	USB500_P	500-mA USB charging can be enabled	Input
Bit(5)	USB100_P	100-mA USB charging can be enabled	Input
Bit(4)	CHGD_DET_EN	Enable charger detection (used to enable CHGD IBIAS block)	Output
Bit(3)	CHGD_IDP_SRC_EN	Enable IDP_SRC and RDM_DWN	Output
Bit(2)	CHGD_VDP_SRC_EN	Enable VDP_SRC buffer, IDM_SINK, and VDAT_REF_DM comp	Output
Bit(1)	CHGD_SERX_EN	Enable SERX comparators on DP and DM	Output
Bit(0)	Reserved	Reserved	Output

Table 14 shows control signals used to control the charger detection analog block from the FSM. The bit number in the left-handed column indicates control bit position used in the charger detection state-machine. Both SERX comparator outputs (CHGD_SERX_DP, CHGD_SERX_DM) are available for register read in the VENDOR_SPECIFIC3 register.

Example:

State:			DCD_INIT
Control:	CHGDCTRL[6:0]	=	011_1010
Bit(6):	USB500_P	=	0
Bit(5):	USB100_P	=	1
Bit(4):	CHGD_DET_EN	=	1
Bit(3):	CHGD_IDP_SRC_EN	=	1
Bit(2):	CHGD_VDP_SRC_EN	=	0
Bit(1):	CHGD_SERX_EN	=	1

Bit(0): Reserved = 0

MADC

The Monitoring Analog-to-Digital Convertor (MADC) enables the host processors to monitor analog signals using Analog-to-Digital Conversion (ADC). After the conversion is complete, the host processor reads the results of the conversion through the inter-integrated circuit (I^2C) interface.

The MADC has the following features:

- 10-bit ADC
- External input (ADCIN0)

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- Internal inputs (VBUS and battery voltage)
- MADC resource shared among multiple users, including system host processors and the internal USB
- Four ways of starting analog-to-digital (ADC) conversion
- Quarter-bit accuracy if the averaging function is used for modem-initiated real-time (RT) conversion requests
- Management of potential concurrent conversion requests and priority between different resource users
- Interrupt signal to the primary interrupt handler (PIH) module at the end-of-sequence of conversions
- Averaging feature to sample the input channel on four consecutive conversion cycles instead of once, and to provide the average value of four conversions

Because the MADC is shared by users, there are four ways to start the ADC conversion. Three of these requests can be triggered by external host processors, and one request is issued by USB:

- Hardware or RT conversion request: This request is initiated by the external host processor to request RT signal conversion. This conversion request is most useful when tied to a modem processor request for battery voltage level, in synchronization with a signal frame boundary. The host processor can request conversion on all ADC input channels using this conversion request.
- SW1 software conversion request: This request can be initiated by the first external host processor to request non-RT conversions. This request is also called an asynchronous or GP conversion (GPC) request.
- SW2 software conversion request: This request can be initiated by the second external host processor to request non-RT conversions. This request is also called an asynchronous or GPC request.
- USB conversion request: This is a GPC request triggered by the USB through TPS65921 internal signals. This conversion request is for the ADCIN12 channel.

It is possible to delay the conversion by programming the acquisition time (ACQUISITION register).

JTAG INTERFACES

The TPS65921 JTAG TAP controller handles standard IEEE JTAG interfaces. This section describes the timing requirements for the tools used to test the TPS65921 power management.

The JTAG/TAP module provides a JTAG interface according to IEEE Std1149.1a. This interface uses the four I/O pins TMS, TCK, TDI, and TDO. The TMS, TCK, and TDI inputs contain a pullup device, which makes their state high when they are not driven. The output TDO is a 3-state output, which is high impedance except when data are shifted between TDI and TDO.

- TCK is the test clock signal.
- TMS is the test mode select signal.
- TDI is the scan path input.
- TDO is the scan path output.

TMS and TDO are multiplexed at the top level with the CPIO0 and CPIO1 pins. The dedicated external TEST pin switches from functional mode (GPIO0/GPIO1) to JTAG mode (TMS/TDO). The JTAG operations are controlled by a state-machine that follows the IEEE Std1149.1a state diagram. This state-machine is reset by the TPS65921 internal power-on reset. A test mode is selected by writing a 6-bit word (instruction) into the instruction register and then accessing the related data register.

Keyboard

The keyboard is connected to the chip using:

- KBR (7:0) input pins for row lines
- KBC (7:0) output pins for column lines

Figure 26 shows the keyboard connection.

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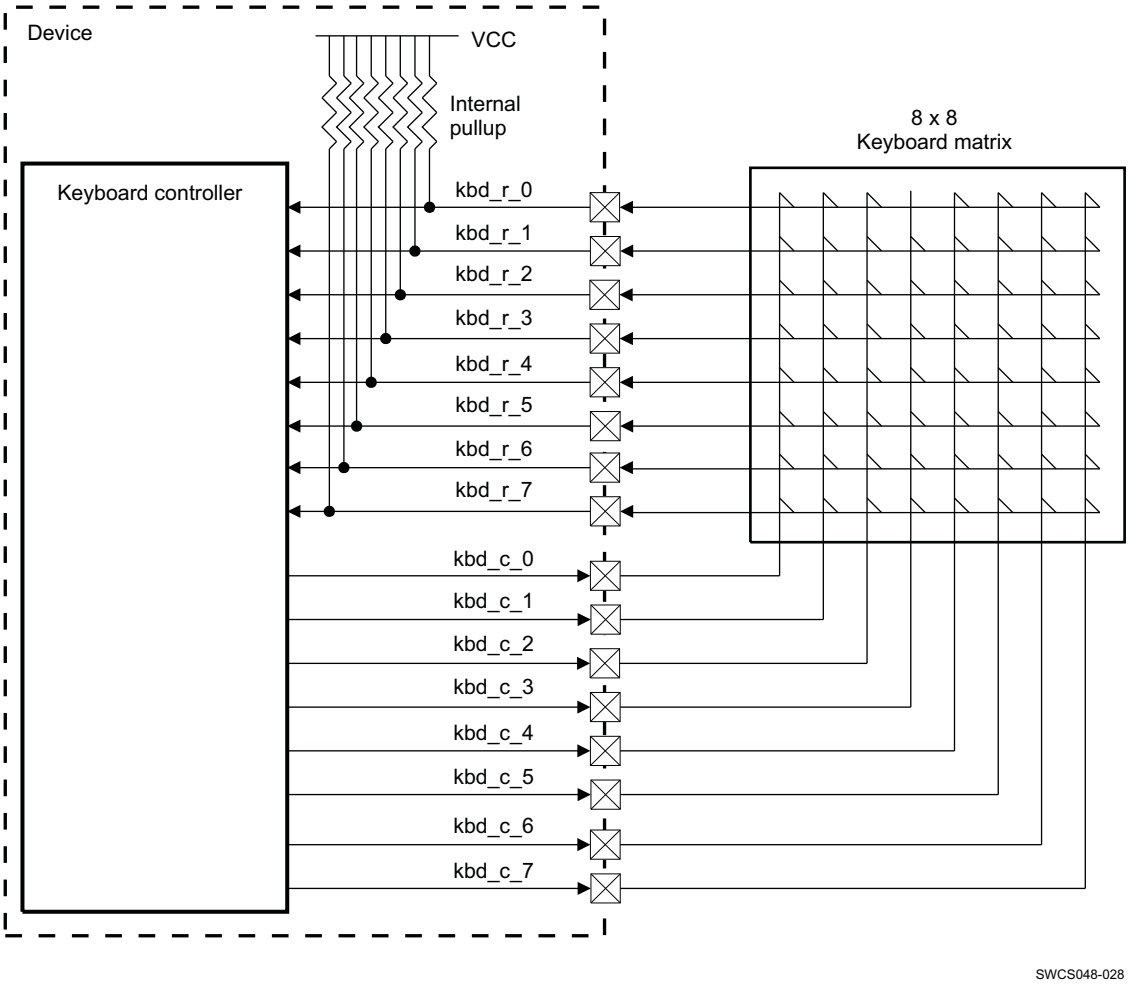

Figure 26. Keyboard Connection

When a key button of the keyboard matrix is pressed, the corresponding row and column lines are shorted together. To allow key press detection, all input pins (KBR) are pulled up to VCC and all output pins (KBC) driven to a low level.

Any action on a button generates an interrupt to the sequencer.

The decoding sequence is written to allow detection of simultaneous press actions on several key buttons.

The keyboard interface can be used with a smaller keyboard area than 8 × 8. To use a 6 × 6 keyboard, KBR(6) and KBR(7) must be tied high to prevent any scanning process distribution.

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PACKAGING INFORMATION

Table 15. TPS65921 Nomenclature Description

FIELDS	MEANING
P	Marking used to note prototype (X), preproduction (P), or qualified/production device (Blank)(1)
A	Mask set version descriptor (initial silicon = BLANK, first silicon revision = A, second silicon revision = B,...)(2)
YM	Year month
LLLLS	Lot code
$	Fab planning code

(1) Blank in the symbol or part number are collapsed so there are no gaps between characters.
(2) Initial silicon version is ES1.0; first revision can be named ES2.0, ES1.1, or ES1.01 depending on the level of change.
NOTE: Device name maximum is 10 characters.

Thermal Characteristics

Table 16. TPS65921 Thermal Resistance Characteristics

Package	θ_{JA}(°C/W)	θ_{JB}(°C/W)	$\theta_{JC(top)}$(°C/W)	Board Type
TPS65921ZQZ	46	17	20	2S2P(1)

(1) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Area Array Surface Mount Package Thermal Measurements).

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Revision History

Table 17. REVISION HISTORY

Version	Literature Number	Date	Notes
F	SWCS048	March 2012	See (1).

(1) *TPS65921 Data Manual*, SWCS048F - Table 13: Swapped REFGND and AGND descriptions.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65921B1ZQZ	ACTIVE	BGA MICROSTAR JUNIOR	ZQZ	120	1	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TPS65921B1ZQZR	ACTIVE	BGA MICROSTAR JUNIOR	ZQZ	120	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TPS65921BZQZ	ACTIVE	BGA MICROSTAR JUNIOR	ZQZ	120	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TPS65921BZQZR	ACTIVE	BGA MICROSTAR JUNIOR	ZQZ	120	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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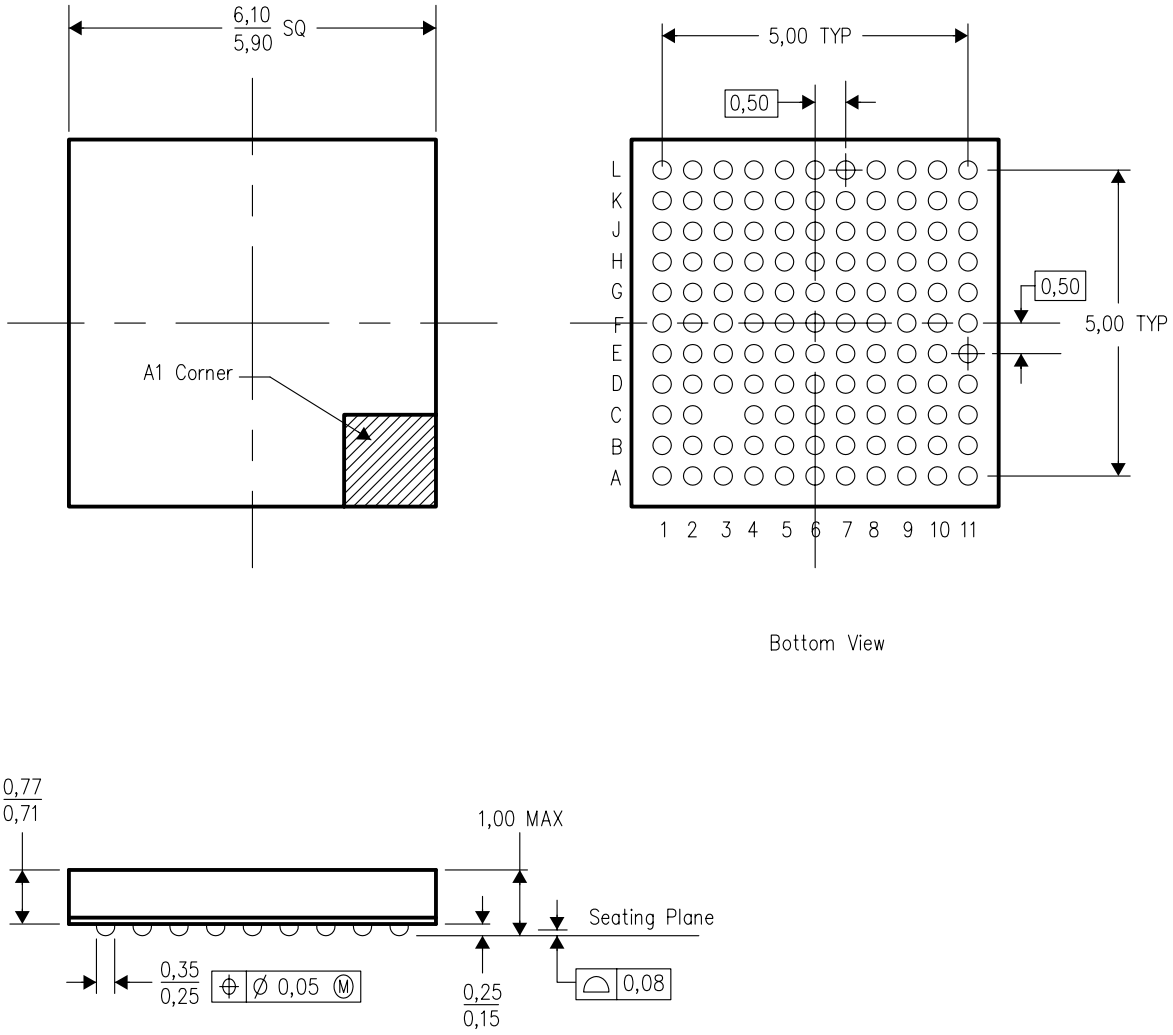
ZQZ (S–PBGA–N120) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This package is lead–free.

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