Single-chip Type with Built-in FET Switching Regulator Series

2-output High-efficiency Step-down Switching Regulators with Built-in Power MOSFET

BD9302FP

● Description

The BD9302FP is a 2-channel step-down switching regulator controller with a 2.5-MHz, 2-A power switch and available for 2.5-MHz high speed switching operation, which facilitates settings of switching frequency with external resistance, supporting for a wide input voltage range of 6 to 18 V. Furthermore, due to a low reference voltage of 0.6 V, this BD9302FP is an L/C best suited to high-voltage input/low-voltage output applications, for example, to step down a voltage from 12 V to 1.2 V.

● Features

1) A wide input voltage range of 6 V to 18 V
2) Easy switching frequency setting in the range of 200 k to 2.5 MHz.
3) Two built-in power switches of 0.4 Ω, 2 A.
4) 180˚ phase shift
5) Built-in Under Voltage Lock Out circuit
6) Built-in overcurrent protection circuit
7) Built-in Thermal Shutdown circuit

● Use

Power supply for DPS requiring two power sources
ADSL modem/plasma display
Audio devices

● Absolute maximum ratings (Ta=25˚C)

Item	Symbol	Rating	Unit
Power supply voltage	Vcc	20	V
Power dissipation	Pd	1450*	mW
Operating temperature	Topr	–40 ~ +85	˚C
Storage temperature	Tstg	–55 ~ +150	˚C
Output current	Io	2**	A
Maximum junction temperature	Tjmax	150	˚C

* Should be derated by 11.6 mW/˚C at Ta=25˚C or more. When mounted on a glass epoxy PCB of 70¥70¥1.6 mm)

** Should not exceed Pd-value.

● Recommended operating range (Ta=25˚C)

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Power supply voltage	Vcc	6	12	18	V
Output current	Io	–	–	1.8	A
Timing resistance	RT	10	–	100	kΩ
Oscillation frequency	Fosc	100	–	2500	kHz

● Electrical characteristics

○ Electrical characteristics (Unless otherwise specified, Ta=25˚C, Vcc=12 V, RT=10 kΩ)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Triangular wave oscillator block]						
Oscillation frequency	FOSC	1800	2000	2200	kHz	RT=10kΩ
Frequency variation	FDVO	–	1	–	%	~ 18V
[Overcurrent protection circuit block]						
Overcurrent limit	Isw	2	4	6	A	*
[Under-voltage malfunction prevention circuit block]						
Upper limit threshold voltage	VtH	3.0	3.3	3.6	V	
Lower limit threshold voltage	VtL	2.7	3.0	3.3	V	
[Soft start circuit block]						
Source current	Isso	6	10	14	uA	Vss=1V
Sink current	ISSI	0.6	1.7	5	mA	Vss=1V, Vcc=3V
Clamp voltage	Vcl	1.75	1.95	2.15	V	
Shutdown voltage	VSDWN	–	–	0.3	V	Vcc=3V

○Not designed for radiation resistance.

* Design guarantee (No 100% pre-shipment inspections are conducted.)

● Electrical characteristics

○Electrical characteristics (Unless otherwise specified, Ta=25˚C, Vcc=12 V, R_T=10 kΩ)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Error amplifier block]						
Input bias current	I_{IB}	–	0.4	1	uA	
Voltage gain	AV	–	200	–	V/V	
COMP maximum output voltage	V_{OH}	1.75	1.95	–	V	I_{COMP}= –0.1mA
COMP minimum output voltage	V_{OL}	–	0.8	1.0	V	I_{COMP}=0.1mA
Output sink current	I_{OI}	1	2	4	mA	V_{FB}=0.8V
Output source current	I_{OO}	– 8	– 4	– 1	mA	V_{FB}=0.4V
Feedback voltage	V_{FB}	0.588	0.600	0.612	V	Buffer
[Output block]						
Upper-side ON resistance	Ronh	–	0.4	0.6	Ω	Io=1A*
Low-side ON resistance	Ronl	–	2	3	Ω	Io=20mA*
OFF current	I_{OFF}	0.1	0.2	0.4	mA	SW=0V
[Total device]						
Average supply current	I_{CC}	–	5	–	mA	R_T=1.0V

○Not designed for radiation resistance.
* Design guarantee (No 100% pre-shipment inspections are conducted.)

● Measurement circuit diagram

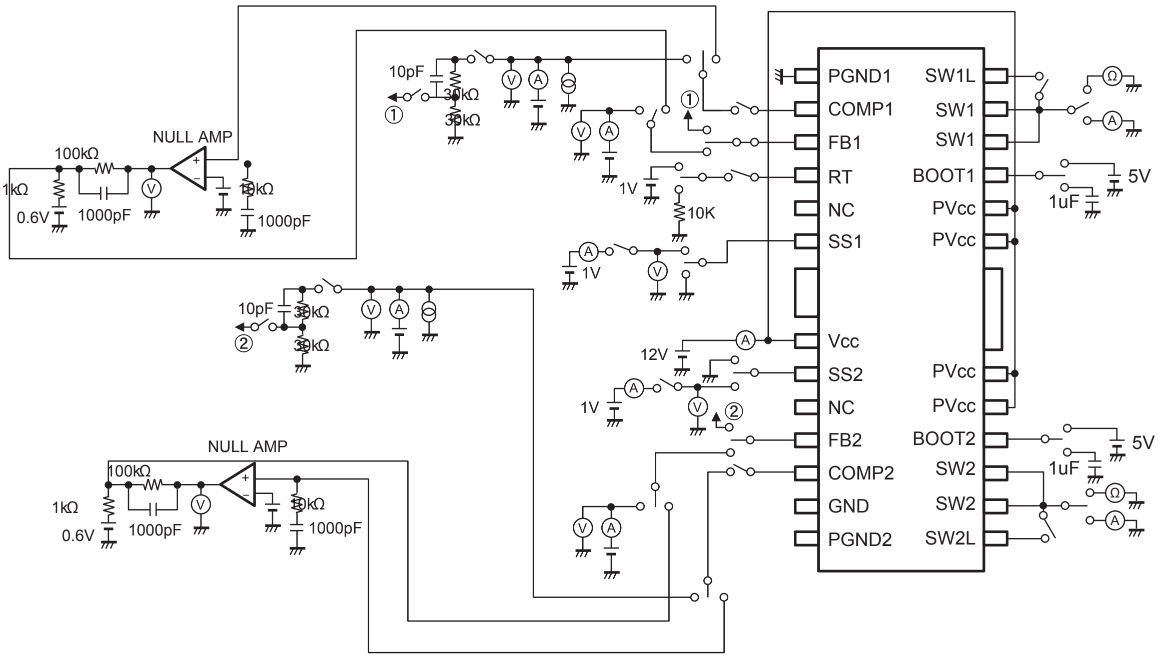


Fig. 1 Typical measurement circuit

● Reference characteristics data

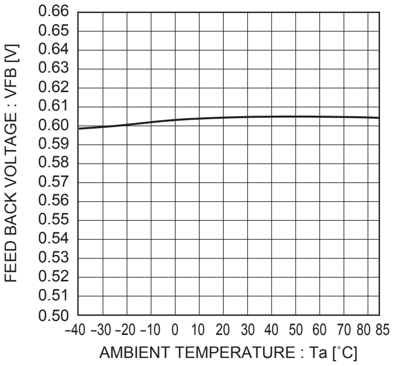


Fig.2
Feedback voltage –
Ambient temperature

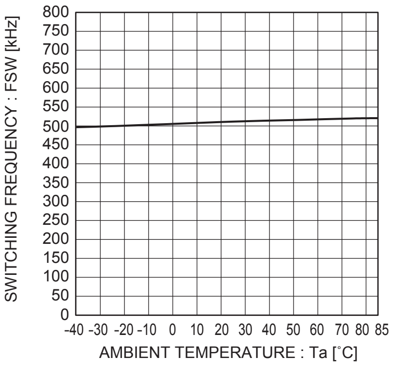


Fig.3
Switching frequency –
Ambient temperature

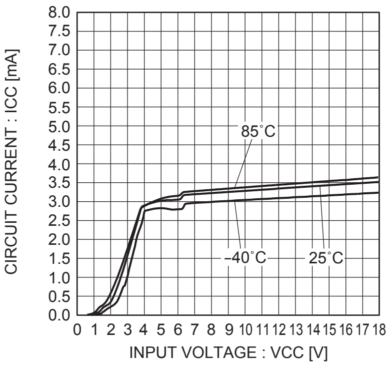


Fig.4
Power supply voltage –
Circuit current

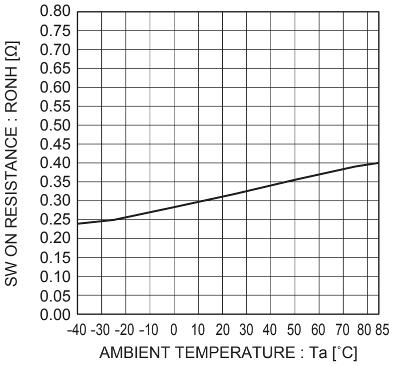


Fig.5
SW ON resistance –
Ambient temperature

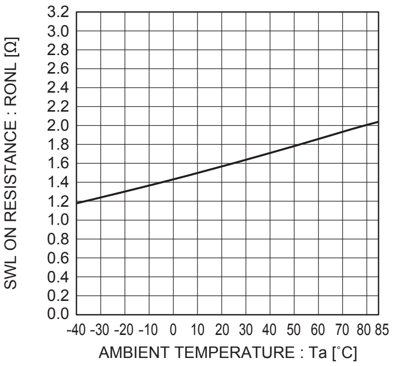


Fig.6
SWL ON resistance –
Ambient temperature

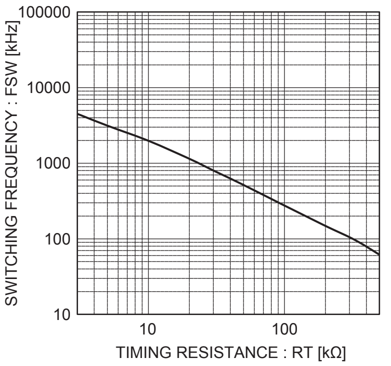


Fig.7
Setting resistance –
Switching frequency

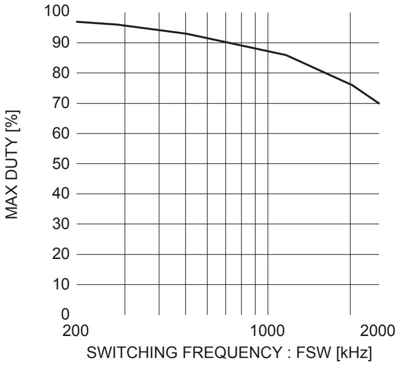


Fig.8
Switching frequency – MAX Duty

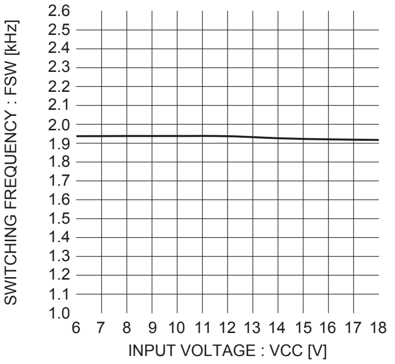


Fig.9
Switching frequency – Power supply voltage

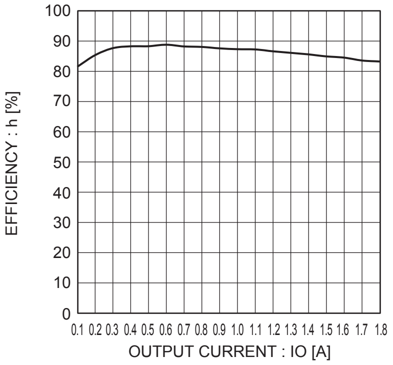


Fig.10
Output current – Efficiency

(*) The data shown above represent real values sampled but not guarantee values.

● Reference characteristics data

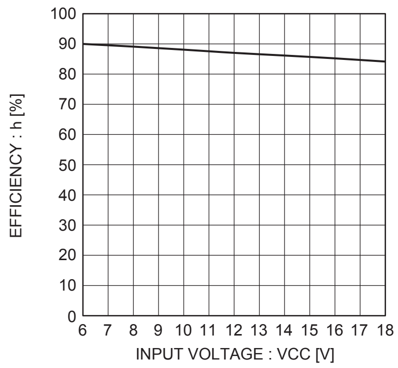


Fig.11
Power supply voltage – Efficiency

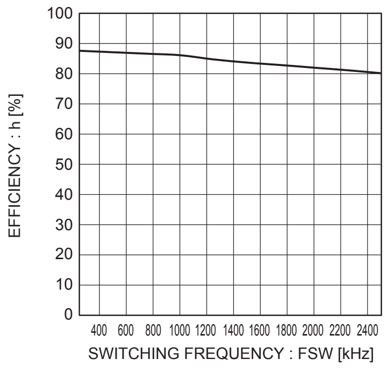


Fig.12
Switching frequency – Efficiency

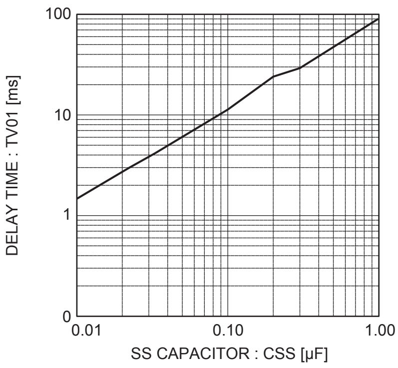


Fig.13
Set capacitance – Delay time

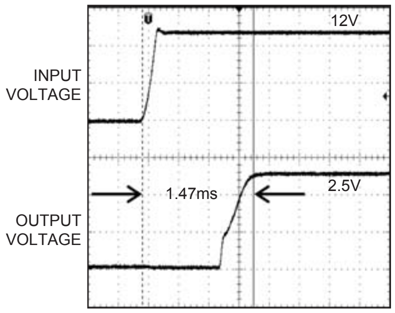


Fig.14
Startup waveform

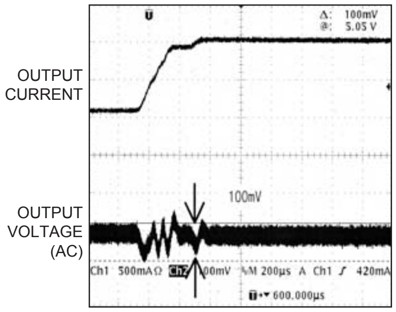


Fig.15
Load transient response No. 1

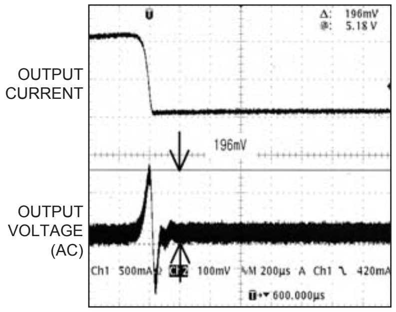


Fig.16
Load transient response No. 2

● Application measurement circuit diagram

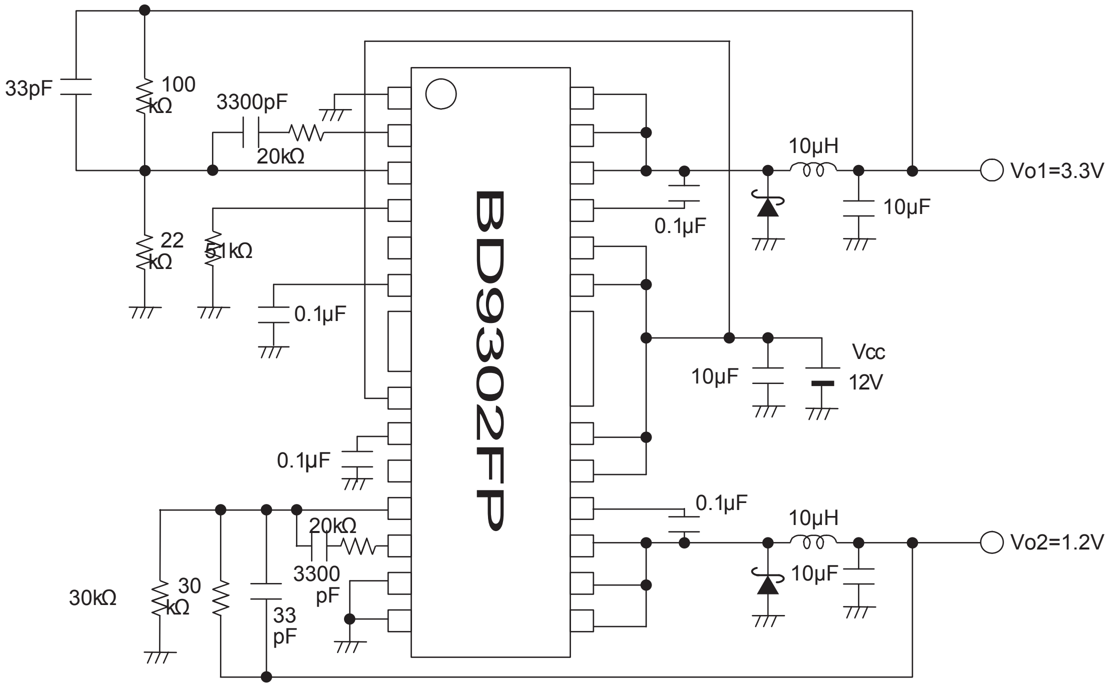
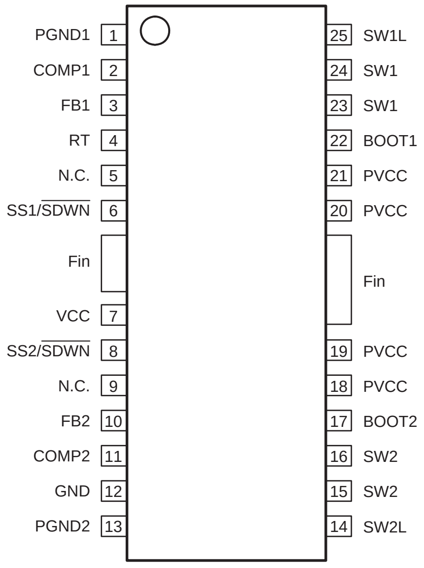


Fig.17 Application measurement circuit diagram

(*) The data shown above represent real values sampled but not guarantee values.

● Pin assignment



● Block diagram

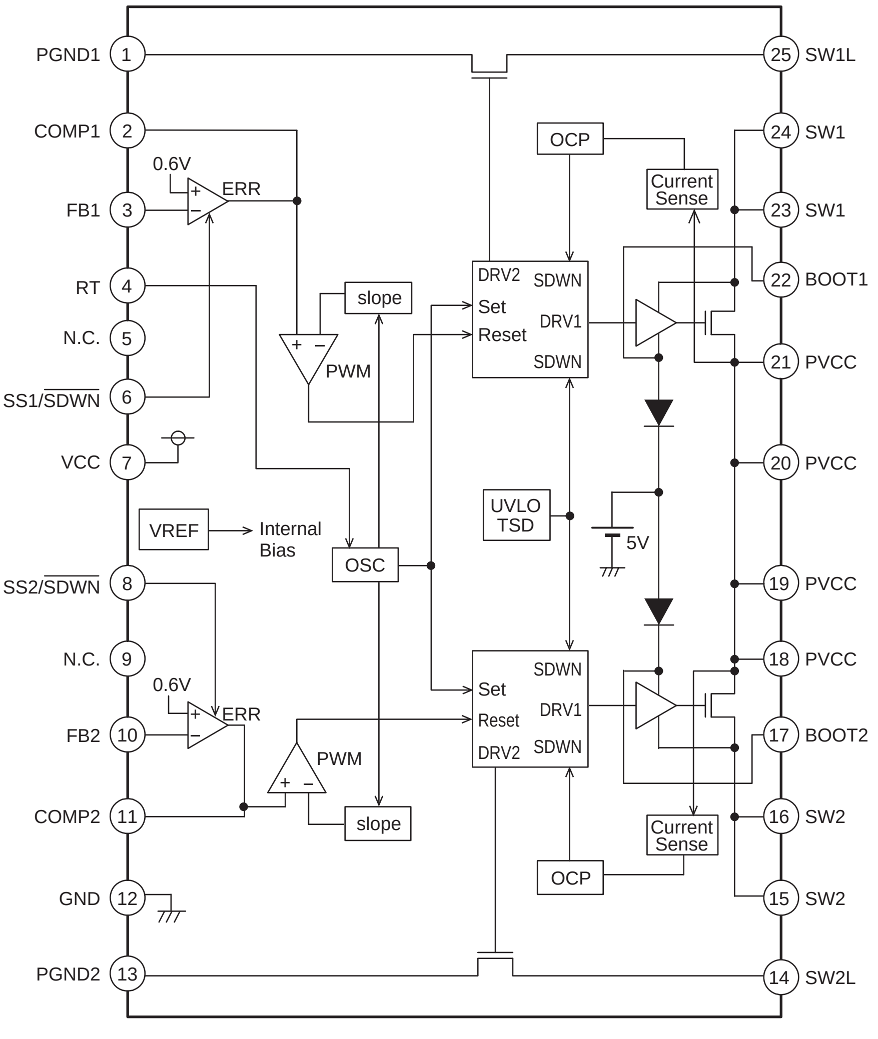


Fig.18 Pin assignment / Block diagram

● Pin assignment / functions

Pin No.	Pin name	Function
1	PGND1	Ground
2	COMP1	Error amplifier output
3	FB1	Error amplifier inverting input
4	RT	Frequency setting resistor connection
5	–	N.C.
6	SS1/SDWN	Soft start capacitor connection (Shutdown at Low)
7	VCC	Power supply input
8	SS2/SDWN	Soft start capacitor connection (Shutdown at Low)
9	–	N.C.
10	FB2	Error amplifier inverting input
11	COMP2	Error amplifier output
12	GND	Ground

Pin No.	Pin name	Function
13	PGND2	Ground
14	SW2L	Switching output 2 (Low side)
15	SW2	Switching output 2
16	SW2	Switching output 2
17	BOOT2	Boot capacitor connection
18	Pvcc	Power supply input
19	Pvcc	Power supply input
20	Pvcc	Power supply input
21	Pvcc	Power supply input
22	BOOT1	Boot capacitor connection
23	SW1	Switching output 1
24	SW1	Switching output 1
25	SW1L	Switching output 1 (Low side)

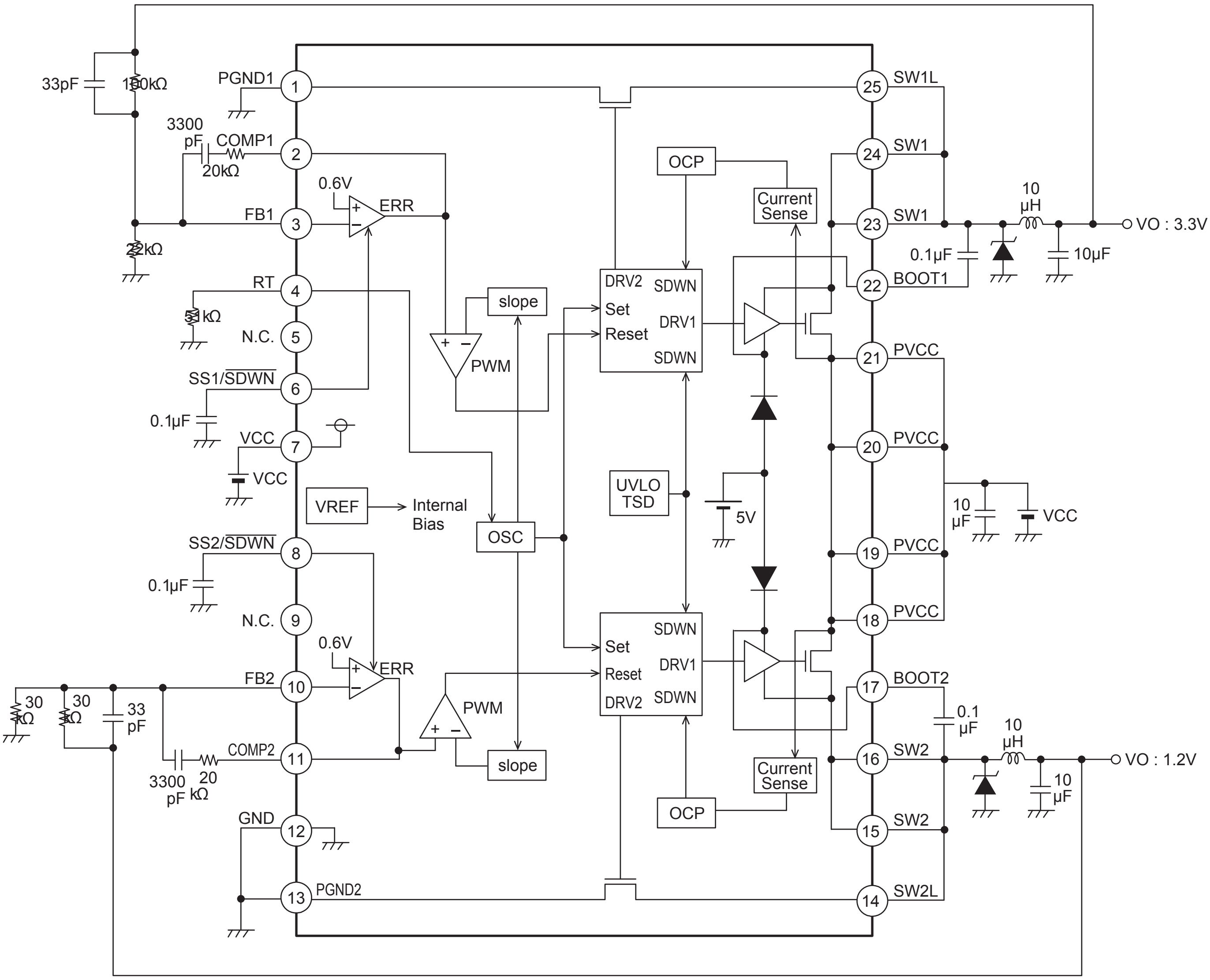


Fig.19 Typical application circuit

ü Error amplifier (ERR) block

The ERR block is a circuit used to compare between the 0.6-V reference voltage and the feedback voltage of output voltage. The COMP voltage, a result of this comparison, determines the switching Duty. Furthermore, soft start function is activated with the SS voltage while in startup operation. Consequently, the COMP voltage is limited to the SS voltage.

ü Oscillator (OSC) block

The OSC block is a block to determine the switching frequency through the RT pin, which is settable in the range of 100 kHz to 2500 kHz.

ü SLOPE block

The SLOPE block is a block to generate a triangular wave from the clock generated with the OSC and then to transmit the triangular wave to the PWM comparator.

ü PWM block

The PWM block is used to make comparison between the output COMP voltage of the error amplifier block and the triangular wave of the SLOPE block, thus determining the switching Duty. The switching duty is limited with the maximum duty ratio, which is internally determined, and will not reach 100%.

ü Reference voltage (UREF) block

The UREF block is a block to generate a 2.9-V internal reference voltage.

ü Protection circuit (UVLO/TSD) block

The UVLO (Under Voltage Lock Out) circuit is used to shut down the circuit when the voltage falls below approximately 3.3 V, while the TSD (Thermal Shutdown) circuit is used to shut down the circuit at a temperature of 175˚C and reset it at a temperature of 160˚C.

ü Overcurrent protection circuit (OCP)

This function is used to detect a current passing through the power transistor FET with the CURRENT SENSE and activate the overcurrent protection when the current reaches approximately 4 A. If the overcurrent protection is activated, switching will be turned OFF to discharge the SS pin capacitance.

● Timing chart

Startup sequence

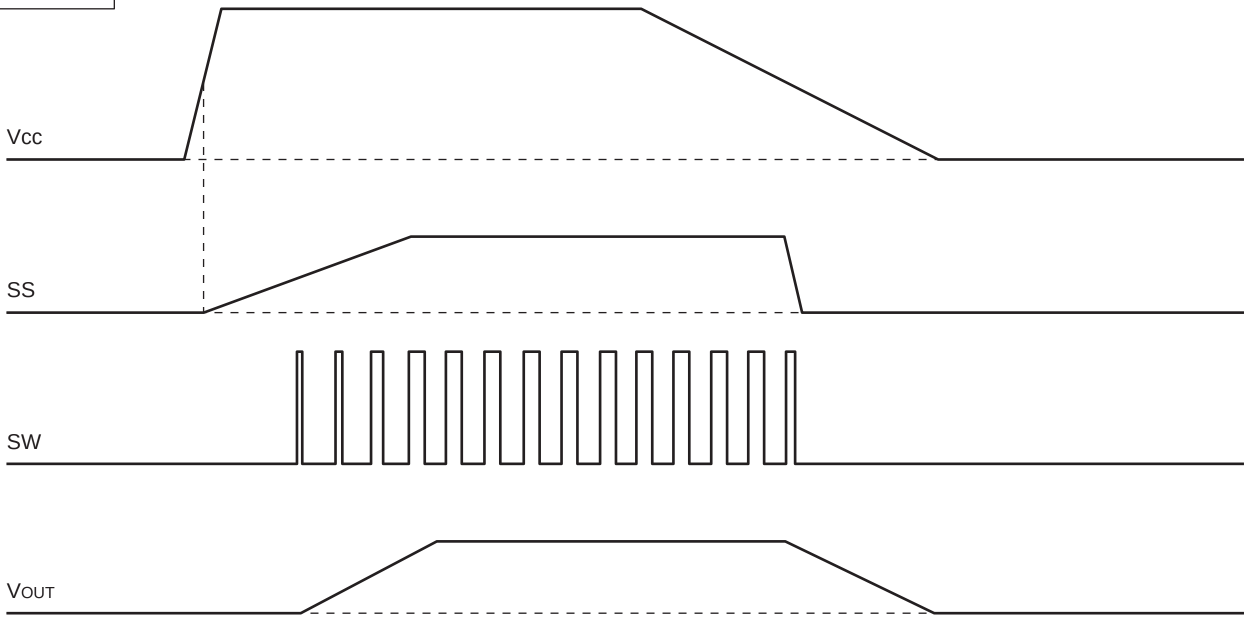


Fig.20 Startup sequence

Normal operation

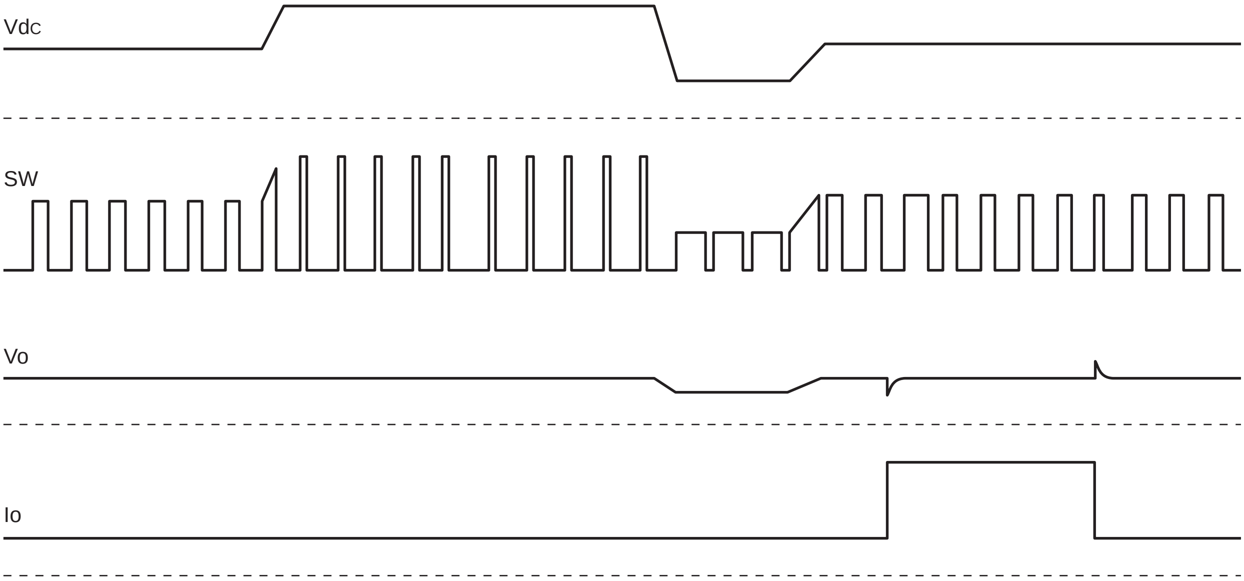


Fig.21 While in normal operation

● External component setting procedure

(1) Setting of output L constant

The coil L used for output is determined according to the rated current I_{LR} and the maximum load current value I_{OMAX} of the coil.

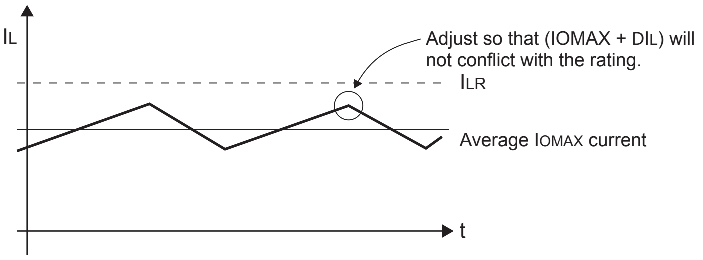


Fig.22

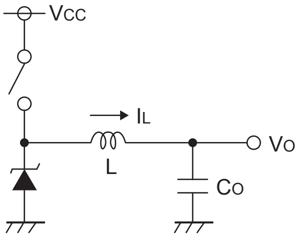


Fig.23

Adjust so that (I_{OMAX} + DI_L) will not conflict with the rating. At this time, DI_L can be obtained according to the formula shown below.

Step-down $$DI_L = \frac{1}{L}\ \text{¥}\ (V_{CC} - V_O)\ \text{¥}\ \frac{V_O}{V_{CC}}\ \text{¥}\ \frac{1}{f}\quad [A] \ldots (1.1)$$,where f: Switching frequency

Furthermore, since the coil L value may also vary by approximately ±30%, set this value with an adequate margin. If the coil current I_L exceeds the rated coil current I_{LR}, the internal IC element may be damaged. It is recommended to make setting of coil value in the range of 4.7 μF to 100 μF.

(2) Setting of output Co constant

For output capacitor, select the allowable ripple voltage V_{PP} or the allowable drop voltage at a sharp change of load, whichever larger for the capacitor. The output ripple voltage can be obtained according to the formula shown below.

Step-down $$DV_{PP} = DI_L\ \text{¥}\ R_{ESR} + \frac{DI_L}{2C_O}\ \text{¥}\ \frac{V_O}{V_{CC}}\ \text{¥}\ \frac{1}{f}\quad [V]$$,where f: Switching frequency

Design the component so that this constant will fall within the allowable ripple voltage.
Furthermore, estimate the drop voltage V_{DR} at a sharp change of load according to the formula shown below.

$$V_{DR} = \frac{DI}{C_O}\ \text{¥}\ 10\mu\text{sec}\qquad [V]$$

However, 10 μsec will be the estimated value of the DC/DC converter response speed.

Make setting of capacitance with thorough consideration given to the margin so that these two values will fall into the specified values. It is recommended to make setting of the capacitance in the range of 10 μF to 100 μF. if a short circuit occurs, an inverse current passes through the parasitic diode to cause damage to the internal circuits. To prevent that, insert a backflow prevention diode.

(3) Setting of feedback resistance constant

In order to make settings of feedback resistance, refer to the formula shown. It is recommended to make setting of resistance in the range of 10 kΩ to 330 kΩ. Setting the resistance to 10 kΩ or less will result in degraded power efficiency, while setting it to 330 kΩ or more will increase the offset voltage due to the input bias current of 0.4 μA (TYP) of the internal error amplifier.

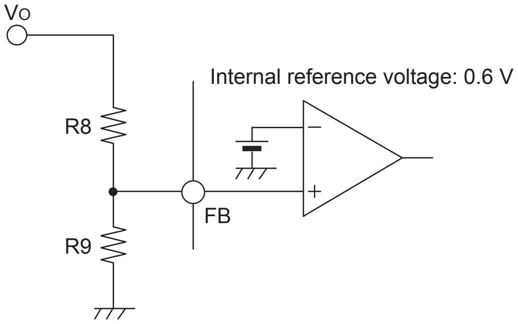


Fig.24

$$V_O = \frac{R8+R9}{R9} \text{ ¥ } 0.6 \text{ [V]}$$

(4) Setting of oscillation frequency

Connecting a resistor to the RT pin (pin 4) will allow for the setting of triangular wave oscillation frequency. The RT determines the charge/discharge current to the internal capacitor, with which the frequency varies. Referring to Figure shown below, make settings of the RT resistor. Recommended setting range is 10 to 100 kΩ. Be noted that any setting outside of this range may turn OFF switching, thus impairing the operation guarantee.

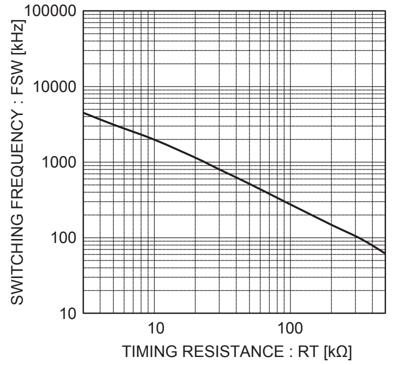


Fig.25 RT vs. Switching frequency

(5) Setting of soft start time

The soft start function will be required to prevent an excessive increase in the coil current and overshoot of the output voltage, while in startup operation. Figure below shows the relationship between the capacitor and the soft start time. Referring to this Figure, make the capacitor setting.

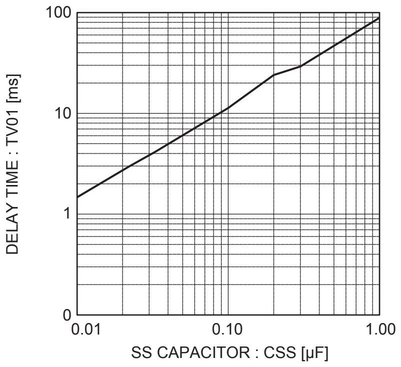


Fig.26 SS capacitance vs. Delay time

It is recommended to make setting of capacitance value in the range of 0.01 to 10 μF. Setting the capacitance value to 0.01 μF or less may cause overshoot to the output voltage. If any startup-related function (sequence) of other power supply is provided, use a high-accuracy product (e.g. ¥ 5R) or the like.

Furthermore, since the soft start time varies with the input voltage, output voltage, load, coil, output capacitor, or else, be sure to check to be sure this soft start time on the actual system.

(6) Phase compensation

Phase compensation setting procedure

The phase compensation setting procedure varies with the selection of capacitance used for DC/DC converter application. In this connection, the following section describes the procedure by classifying into the two types. Furthermore, the application stability conditions are described in the “Description” section.

1. Application stability conditions
2. For output capacitors having high ESR, such as electrolytic capacitor
3. For output capacitors having low ESR, such as ceramic capacitor or OS-CON

About application stability conditions

The following section shows the stability conditions of negative feedback system.

ü At a 1 (0-dB) gain, the phase delay is 150˚ or less (i.e., the phase margin is 30˚ or more).

Furthermore, since the DC/DC converter application is sampled according to the switching frequency, GBW of the overall system should be set to 1/10 or less of the switching frequency. The following section summarizes the targeted characteristics of this application.

ü At a 1 (0-dB) gain, the phase delay is 150˚ or less (i.e., the phase margin is 30˚ or more).
ü The GBW (i.e., frequency at 0-dB gain) for this occasion is 1/10 or less of the switching frequency.

Consequently, in order to upgrade the responsiveness, higher switching frequency should be provided.

A knack for ensuring the stability through the phase compensation is to cancel a secondary phase delay (-180˚) resulting from LC resonance with a secondary phase lead (i.e., through inserting two phase leads). Furthermore, the GBW (i.e., frequency at 0-dB gain) is determined according to phase compensation capacitance to be provided for the error amplifier. Consequently, in order to reduce the GBW, increase the capacitor capacitance.

(1) Typical (sun) integrator (Low pass filter)

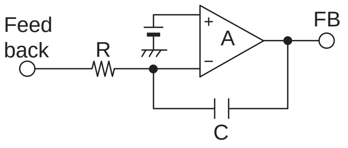


Fig.27

(2) Open loop characteristics of integrator

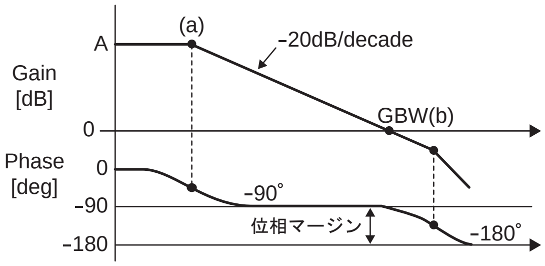


Fig.28

Point (a) $fa=\frac{1}{2pRCA}$1.25 [Hz]

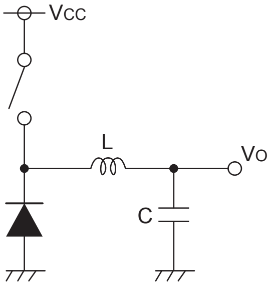
Point (b) $fa= GBW \ \frac{1}{2pRC}$ [Hz]

Since the error amplifier is provided with (1) or (2) phase compensation, the low pass filter is applied.
In the case of the DC/DC converter application, the R becomes a parallel resistance of the feedback resistance.

For output capacitors having high ESR, such as aluminum electrolytic capacitor

For output capacitors having high ESR (i.e., several ohms), the phase compensation setting procedure becomes comparatively simple. Since the DC/DC converter application has surely a LC resonant circuit attached to the output, a -180˚ phase-delay occurs in that area. If ESR component is present there, however, a +90˚ phase-lead occurs to shift the phase delay to -90˚. Since the phase delay is desired to set within 150˚, this is a very effective method but has a demerit to increase the ripple component of the output voltage.

(3) LC resonant circuit

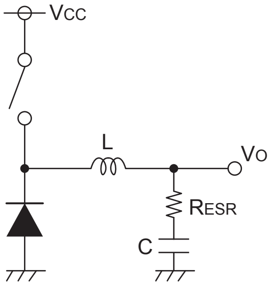


$f_r = \frac{1}{2p\sqrt{LC}}$ [Hz]

At this resonance point, a -180˚ phase-delay occurs.

Fig.29

(4) With ESR provided



$f_r = \frac{1}{2p\sqrt{LC}}$ [Hz]: Resonance point

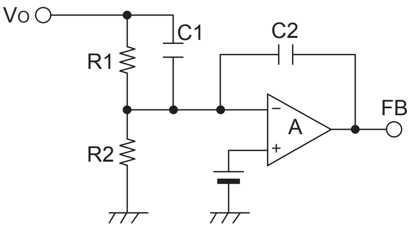
$f_{ESR} = \frac{1}{2pR_{ESR}C}$ [Hz]: Phase lead

A -90˚ phase-delay occurs.

Fig.30

According to changes in phase characteristics due to the ESR, only one phase lead should be inserted. For this phase lead, select either of the methods shows below.

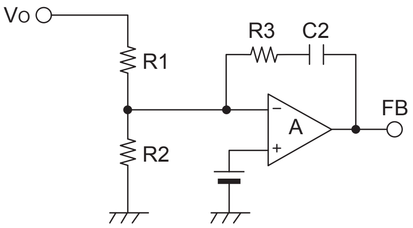
(5) Insert feedback resistance in the C.



Phase lead: $f_Z = \frac{1}{2pC1R1}$ [Hz]

Fig.31

(6) Insert the R3 in integrator.



Phase lead: $f_Z = \frac{1}{2pC2R3}$ [Hz]

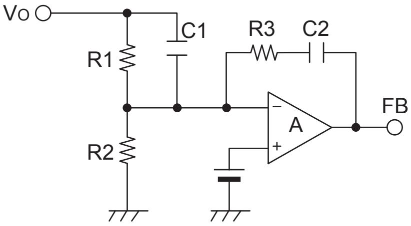
Fig.32

For the purpose of canceling the LC resonance, the frequency to insert the phase lead should be set close to the LC resonant frequency.

For output capacitors having low ESR, such as ceramic capacitor or OS-CON

Unlike the section above, in order to use capacitors having low ESR (i.e., several tens of mW), two phase-leads should be inserted so that a -180∞ phase-delay due to LC resonance will be observed. Example (7) blow shows a typical phase compensation procedure.

(7) Phase compensation with secondary phase lead



Phase lead: $f_{Z1} = \frac{1}{2pR1C1}$ [Hz]

Phase lead: $f_{Z2} = \frac{1}{2pR3C2}$ [Hz]

LC resonant frequency: $f_r = \frac{1}{2p\sqrt{LC}}$ [Hz]

Fig.33

For the settings of phase lead frequency, insert both of the phase leads close to the LC resonant frequency.

● Equivalent circuit

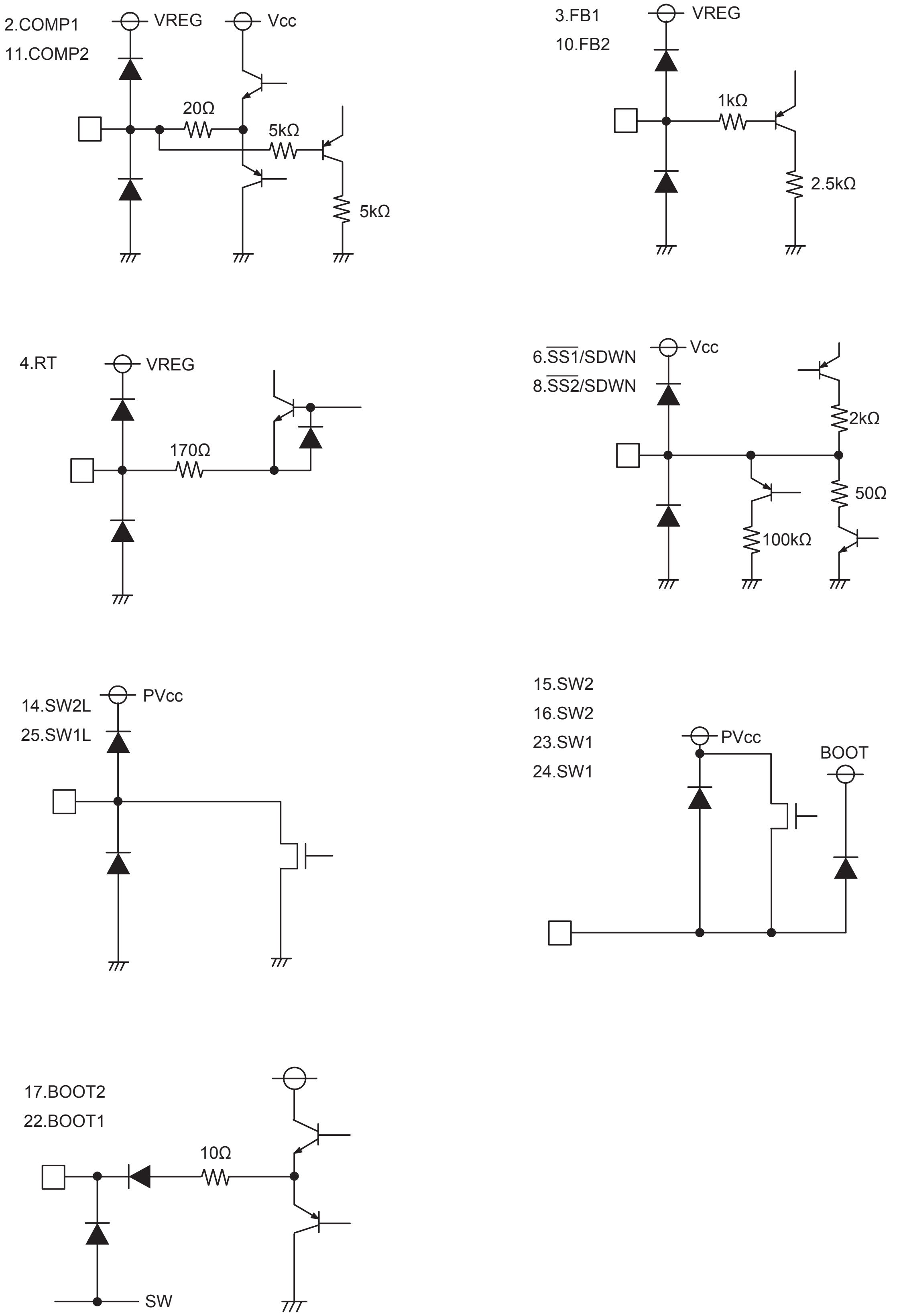


Fig.34 Equivalent circuit

● Cautions on use

1) Absolute maximum ratings
Even though thorough attention is exerted to the quality control of this IC, exceeding the absolute maximum ratings, such as applied voltage, operating temperature range, etc., can break down the IC. Should the IC break down, it will be impossible to identify breaking mode such as short circuit mode or an open mode. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including use of fuses, etc.

2) GND potential
GNDMake setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state.

3) Thermal design
With consideration given to power dissipation (Pd) in the actual use state, provide the thermal design with an adequate margin.

4) Short circuit between pins and erroneous mounting
In order to mount ICs on a set printed circuit board, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the GND pin, the ICs can break down.

5) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

6) Inspection with set printed circuit board
On the inspection with the set printed circuit board, if a capacitor is connected to a low-impedance pin, the IC can suffer stress. Therefore, be sure to discharge from the set printed circuit board by each process. For protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set printed circuit board. Furthermore, in order to connect the jig for the inspection process, be sure to turn OFF the power supply and then mount the set printed circuit board to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount the set printed circuit board from the jig.

7) IC pin input
This IC is a monolithic IC, which has P+ isolation and P layer between elements to isolate the elements. P-N junction is formed with this P layer and the N layer of each element, thus composing a variety of parasitic elements.
For example, as shown in Fig. 35, if the resistor and the transistor is connected with the pin respectively,
○When GND>(Pin A) for the resistor or GND>(Pin B) for the transistor (NPN), P-N junction will operate as a parasitic diode.
○For the transistor (NPN), when GND>(Pin B), the parasitic NPN transistor will operate with the N layer of other element in the proximity of the said parasitic diode.

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the IC. Therefore, pay thorough attention not to handle the input pins such as to apply to the input pins a voltage lower than the GND (P layer) so that any parasitic element will operate.

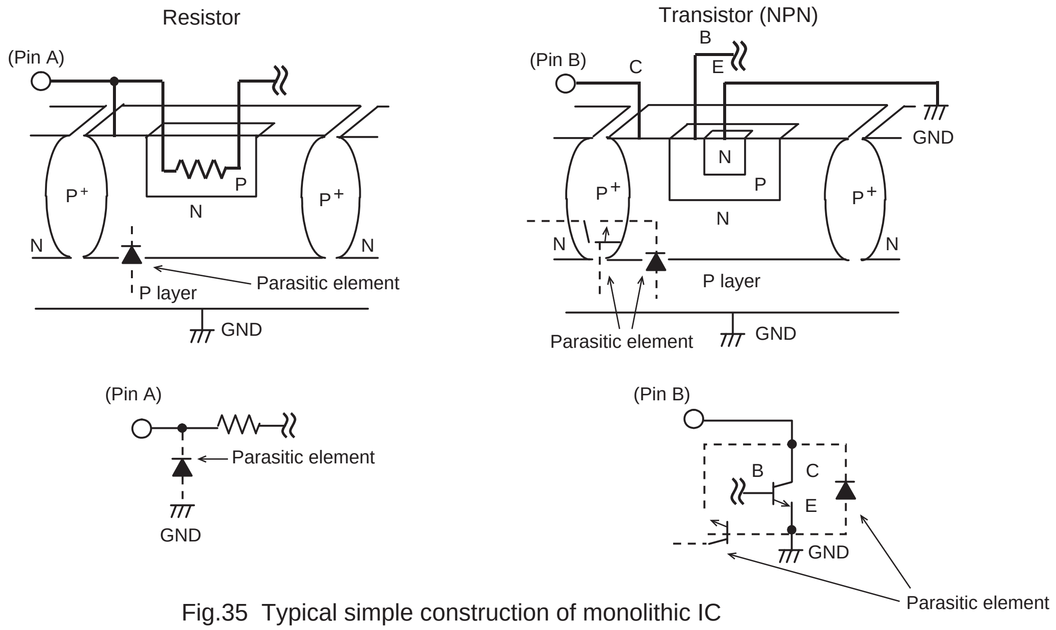


Fig.35 Typical simple construction of monolithic IC

8) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

9) On the application shown on the right, if the VCC and each output voltage are inverted, for example, if the VCC is short-circuited to the Ground with external diode charged, internal circuits or elements may be damaged. To avoid that, use the output pin capacitor in the range of 10 to 100 µF. Furthermore, in order to use a capacitor of 100 µF or more, it is recommended to insert a backflow prevention diode or a bypass diode between the output and VCC.

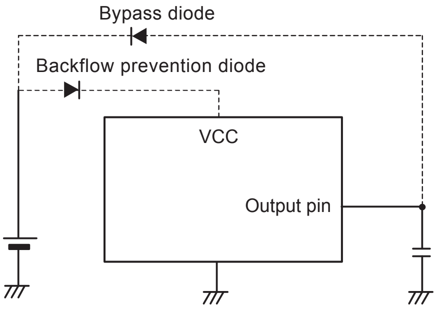


Fig.36 Typical bypass diode application

10) Overcurrent protection circuit
Output has a built-in overcurrent protection circuit according to the current capability, which prevents the destruction of the IC at short-circuiting of load. However, this protection circuit is only effective to prevent destruction due to a sudden accident but does not support for the continuous operation of the protection circuit or use in transition. Furthermore, since the current capability has characteristic negative to temperature, give consideration to the thermal design.

11) Temperature protection circuit
This IC has a built-in temperature protection circuit to prevent the thermal destruction of the IC. As described above, be sure to use this IC within the power dissipation range. Should a condition exceeding the power dissipation range continues, the chip temperature Tj will rise to activate the temperature protection circuit, thus turning OFF the output power element. Then, when the tip temperature Tj falls, the circuit will be automatically reset.
Furthermore, since the temperature protection circuit is activated under the condition exceeding the absolute maximum ratings, NEVER attempt to use the temperature protection circuit for set design or else.

12) Input capacitor
In order to derate a peak noise, which occurs while in switching operation, be sure to insert a capacitor (ceramic capacitor) having a low ESR of 10 to 100 µF as close to the pin as possible between the VCC and Ground.

● Power dissipation

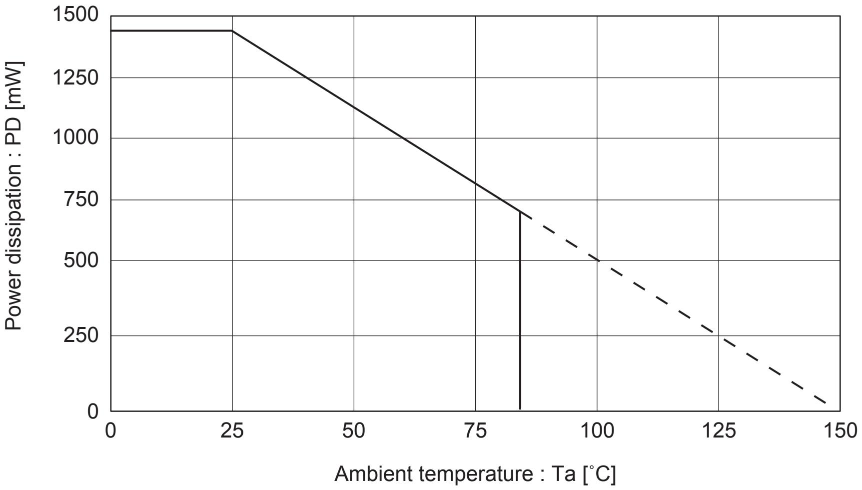
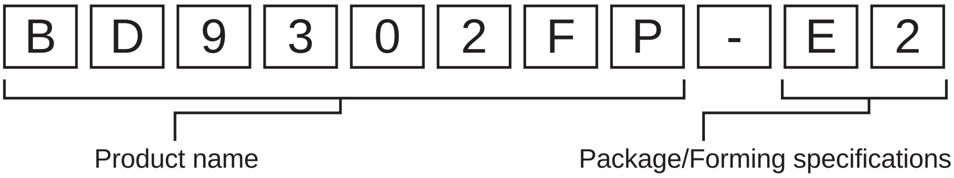


Fig.37 Thermal derating characteristics

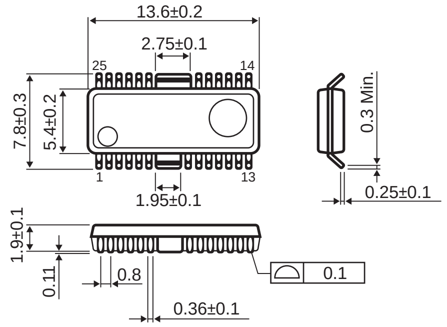
● Selection of order type



● Package specifications

HSOP25

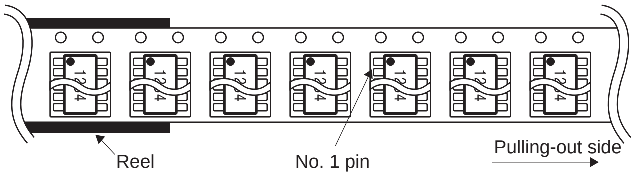
<Outline dimensions>



(Unit : mm)

<Package specifications>

Package style	Embossed carrier tape
Q'ty per package	2000 pcs
Packaging direction	E2 (When holding a reel by left hand and pulling out the tape by right hand, No. 1 pin appears in the upper left of the reel.)



* Please place an order for this IC in multiples of the quantity per package.

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