WINBOND LPC I/O

W83697UF

W83697UG

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1. GENERAL DESCRIPTION

The W83697UF is evolving product from Winbond's most popular I/O family. They feature a whole new interface, namely LPC (Low Pin Count) interface, which will be supported in the new generation chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. With this additional freedom, we can implement more devices on a single chip as demonstrated in W83697UF's integration of Game Port and MIDI Port. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

The disk drive adapter functions of W83697UF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83697UF greatly reduces the number of components required for interfacing with floppy disk drives. The W83697UF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data tranufer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83697UF provides four high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. All UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of **230k**, **460k**, or **921k bps** which support higher speed modems. In addition, the W83697UF provides IR functions: **IrDA 1.0** (**SIR** for 1.152K bps) and TV remote IR (**Consumer IR**, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

The W83697UF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

The W83697UF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function. General Purpose Port 1 is designed to be functional even in power down mode (VCC is off).

The W83697UF is made to fully comply with **Microsoft© PC98 and PC99 Hardware Design Guide, and meet the requirements of ACPI.**

The W83697UF contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices. They are very important for a entertainment or consumer computer.

The W83697UF provides Flash ROM interface. That can support up to 4M legacy flash ROM.

2. FEATURES

General

- Meet LPC Spec. 1.1
- Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)
- Include all the features of Winbond I/O W83877TF
- Integrate Smart Card functions
- Compliant with Microsoft PC98/PC99 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95/98 driver**

UART

- Four high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation

- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate up to **921k bps** for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR with Wake-Up function.

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Game Port

- Support two separate Joysticks
- Support every Joystick two axes (X,Y) and two buttons (S1,S2) controllers

MIDI Port

- The baud rate is 31.25 Kbaud
- 16-byte input FIFO
- 16-byte output FIFO

Flash ROM Interface

- Support up to 4M flash ROM

Fan Speed Control

- Support 3 sets of PWM Fan Speed Control

General Purpose I/O Ports

- 60 programmable general purpose I/O ports
- General purpose I/O ports can serve as simple I/O ports, watch dog timer output, power LED output, infrared I/O pins, suspend LED output, Beep output
- Functional in power down mode

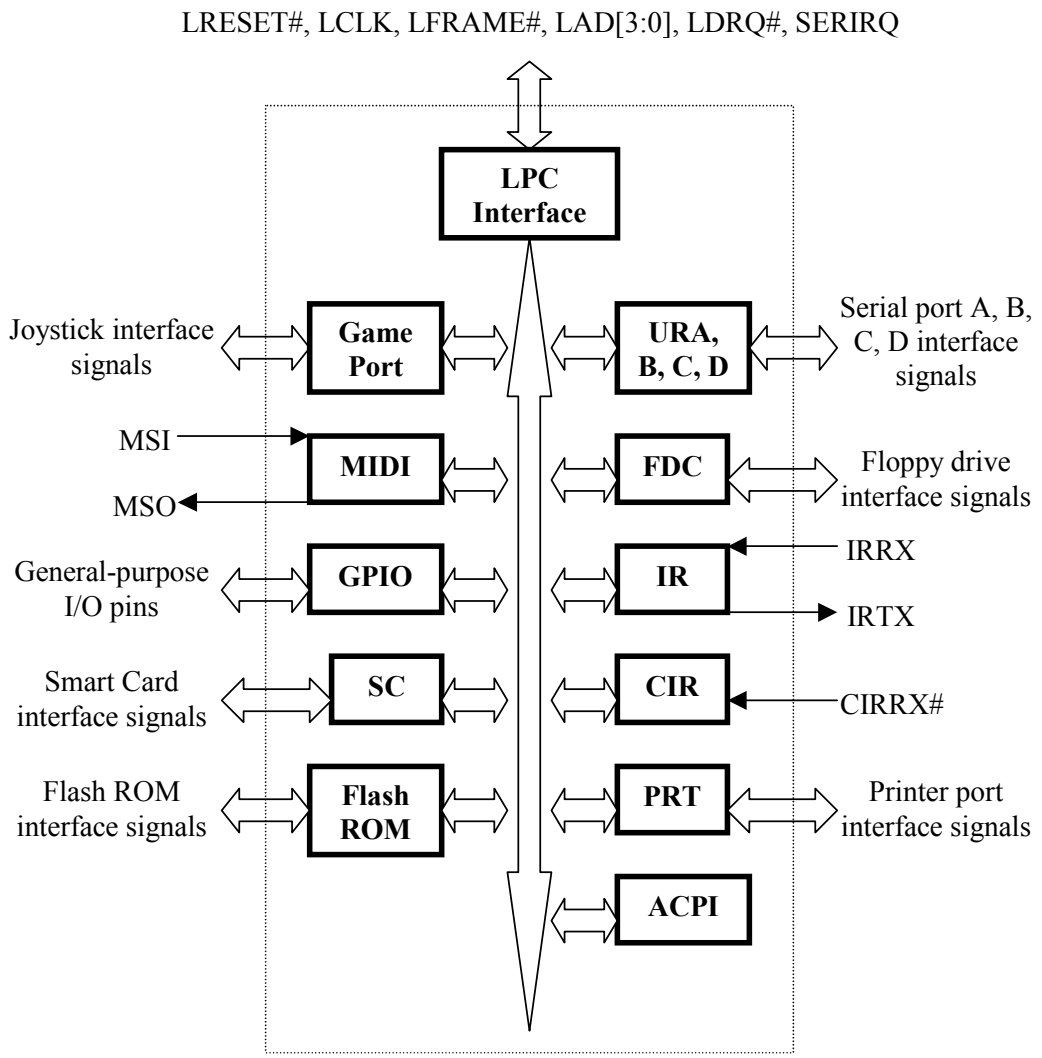
Smart Card Reader Interface

- ISO7816 protocol compliant
- PC/SC T=0 , T=1 compliant

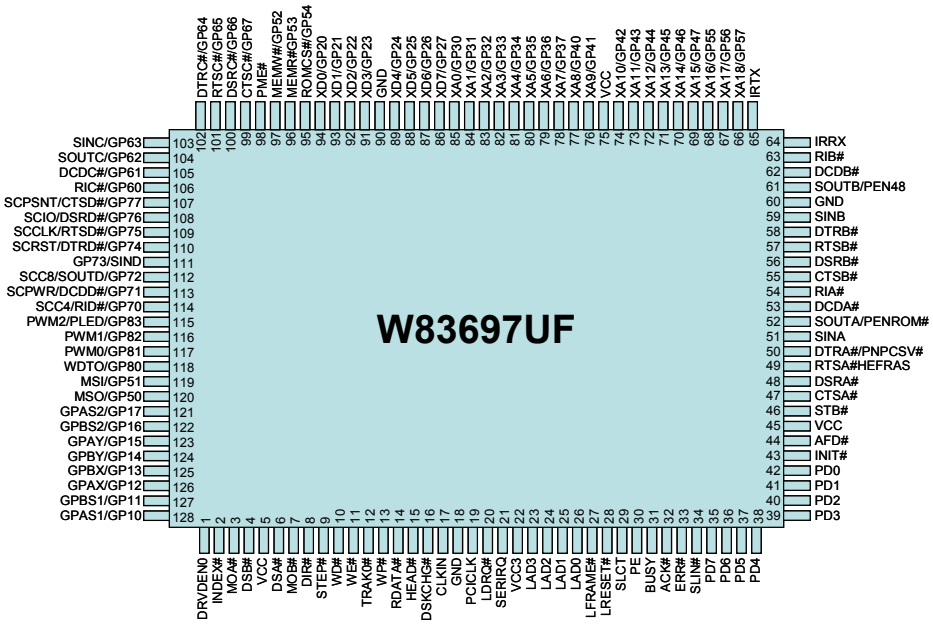
Package

- 128-pin PQFP

3. BLOCK DIAGRAM FOR W83697UF



4. PIN CONFIGURATION FOR W83697UF



5. PIN DESCRIPTION

Note: Please refer to Section DC CHARACTERISTICS for details

PIN DESCRIPTION	
I/O8t	TTL level bi-directional pin with 8mA source-sink capability
I/O12t	TTL level bi-directional pin with 12mA source-sink capability
I/O24t	TTL level bi-directional pin with 24 mA source-sink capability
I/O12tp3	3.3V TTL level bi-directional pin with 12mA source-sink capability
I/O12ts	TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability
I/O24ts	TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/O24tsp3	3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability
I/OD12t	TTL level bi-directional pin and open-drain output with 12mA sink capability
I/OD24t	TTL level bi-directional pin and open-drain output with 24mA sink capability
I/OD24c	CMOS level bi-directional pin and open-drain output with 24mA sink capability
I/OD24a	Bi-directional pin with analog input and open-drain output with 24mA sink capability
I/OD12ts	TTL level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD24ts	TTL level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability
I/OD12cs	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 12mA sink capability
I/OD16cs	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 16mA sink capability
I/OD24cs	CMOS level Schmitt-trigger bi-directional pin and open-drain output with 24mA sink capability
I/OD12csd	CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open-drain output with 12mA sink capability
I/OD12csu	CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open-drain output with 12mA sink capability
O4	Output pin with 4 mA source-sink capability
O8	Output pin with 8 mA source-sink capability
O12	Output pin with 12 mA source-sink capability
O16	Output pin with 16 mA source-sink capability
O24	Output pin with 24 mA source-sink capability
O12p3	3.3V output pin with 12 mA source-sink capability

Pin description, continued

PIN DESCRIPTION	
O_{24p3}	3.3V output pin with 24 mA source-sink capability
OD_{12}	Open-drain output pin with 12 mA sink capability
OD_{24}	Open-drain output pin with 24 mA sink capability
OD_{12p3}	3.3V open-drain output pin with 12 mA sink capability
IN_{t}	TTL level input pin
IN_{tp3}	3.3V TTL level input pin
IN_{td}	TTL level input pin with internal pull down resistor
IN_{tu}	TTL level input pin with internal pull up resistor
IN_{ts}	TTL level Schmitt-trigger input pin
IN_{tsp3}	3.3V TTL level Schmitt-trigger input pin
IN_{c}	CMOS level input pin
IN_{cu}	CMOS level input pin with internal pull up resistor
IN_{cd}	CMOS level input pin with internal pull down resistor
IN_{cs}	CMOS level Schmitt-trigger input pin
IN_{csu}	CMOS level Schmitt-trigger input pin with internal pull up resistor

5.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
CLKIN	17	IN_{tp3}	System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input.
PME#	98	OD_{12p3}	Generated PME event.
PCICLK	19	IN_{tsp3}	PCI clock input.
LDRQ#	20	O_{12p3}	Encoded DMA Request signal.
SERIRQ	21	I/O_{12tp3}	Serial IRQ input/Output.
LAD[3:0]	23-26	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	27	IN_{tsp3}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	28	IN_{tsp3}	Reset signal. It can connect to PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	2	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
MOA#	3	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSB#	4	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
MOB#	7	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24}	Write enable. An open drain output.
TRAK0#	12	INcsu	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
WP#	13	INcsu	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
RDATA#	14	INcsu	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
HEAD#	15	OD24	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	16	INcsu	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

5.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	29	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
WE2#		OD_{12}	EXTENSION FDD MODE: WE2# This pin is for Extension FDD B; its function is the same as the WE# pin of FDC. EXTENSION 2FDD MODE: WE2# This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE	30	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WD2#		OD_{12}	EXTENSION FDD MODE: WD2# This pin is for Extension FDD B; its function is the same as the WD# pin of FDC. EXTENSION 2FDD MODE: WD2# This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.
BUSY	31	IN_{ts}	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
MOB2#		OD_{12}	EXTENSION FDD MODE: MOB2# This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC. EXTENSION 2FDD MODE: MOB2# This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.

Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
ACK#	32	IN_{ts}	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSB2#		OD_{12}	EXTENSION FDD MODE: DSB2# This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC. EXTENSION 2FDD MODE: DSB2# This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
ERR#	33	IN_{ts}	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
HEAD2#		OD_{12}	EXTENSION FDD MODE: HEAD2# This pin is for Extension FDD B; its function is the same as the HEAD#pin of FDC. EXTENSION 2FDD MODE: HEAD2# This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.
SLIN#	34	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STEP2#		OD_{12}	EXTENSION FDD MODE: STEP2# This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC. EXTENSION 2FDD MODE: STEP2# This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.

Multi-mode parallel port, continued

SYMBOL	PIN	I/O	FUNCTION
INIT#	43	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DIR2#		OD_{12}	EXTENSION FDD MODE: DIR2# This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC. EXTENSION 2FDD MODE: DIR2# This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.
AFD#	44	OD_{12}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DRVDEN0		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC. EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
STB#	46	OD_{12}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
INDEX2#		IN_{ts}	EXTENSION FDD MODE: INDEX2# This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: INDEX2# This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.

Multi-mode parallel port, continued

SYMBOL	PIN	I/O	FUNCTION
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
TRAK02#		IN_{ts}	EXTENSION FDD MODE: TRAK02# This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: TRAK02# This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
WP2#		IN_{ts}	EXTENSION FDD MODE: WP2# This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. It is pulled high internally. EXTENSION. 2FDD MODE: WP2# This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC. It is pulled high internally.
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
RDATA2#		IN_{ts}	EXTENSION FDD MODE: RDATA2# This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: RDATA2# This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.

Multi-mode parallel port, continued

SYMBOL	PIN	I/O	FUNCTION
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
DSKCHG2#		IN_{ts}	EXTENSION FDD MODE: DSKCHG2# This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: DSKCHG2# This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	36	I/O_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
MOA2#		OD_{12}	EXTENSION. 2FDD MODE: MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.
PD7	35	I/O_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
DSA2#		OD_{12}	EXTENSION 2FDD MODE: DSA2# This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.

5.4 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA# CTSB#	47 55	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DSRA# DSRB#	48 56	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA# HEFRAS	49	O_8 INcd	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
RTSB#	57	O_8	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
DTRA# PNPCSV#	50	O8 INcd	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PNPCSV#, which provides the power-on value for CR24 bit 0 (PNPCSV#). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
DTRB#	58	O_8	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	51 59	INt	Serial Input. It is used to receive serial data through the communication link.
SOUTA PENROM#	52	O_8 INcd	UART A Serial Output. It is used to transmit serial data out to the communication link. During power on reset , this pin is pulled down internally and is defined as PENROM#, which provides the power on value for CR24 bit 1. A 4.7kΩ is recommended if intends to pull up .
SOUTB PEN48	61	O_8 INcd	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up.
DCDA# DCDB#	53 62	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA# RIB#	54 63	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

Serial Port Interface, continued

SYMBOL	PIN	I/O	FUNCTION
CTSC# GP67	99	IN_t I/OD_{12t}	Clear To Send. It is the modem control input. General purpose I/O port 6 bit7.
DSRC# GP66	100	IN_t I/OD_{12t}	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. General purpose I/O port 6 bit6.
RTSC# GP65	101	O_{12} I/OD_{12t}	UART C Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. General purpose I/O port 6 bit5.
DTRC# GP64	102	O_{12} I/OD_{12t}	UART C Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. General purpose I/O port 6 bit4.
SINC GP63	103	IN_t I/OD_{12t}	Serial Input. It is used to receive serial data through the communication link. General purpose I/O port 6 bit3.
SOUTC GP62	104	O_{12} I/OD_{12t}	UART B Serial Output. It is used to transmit serial data out to the communication link. General purpose I/O port 6 bit2.
DCDC# GP61	105	IN_t I/OD_{12t}	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier. General purpose I/O port 6 bit1.
RIC# GP60	106	IN_t I/OD_{12t}	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. General purpose I/O port 6 bit0.

5.5 Infrared Port

SYMBOL	PIN	I/O	FUNCTION
IRRX	64	IN_{ts}	Alternate Function Input: Infrared Receiver input. General purpose I/O port 3 bit 6.
IRTX	65	O_{12}	Alternate Function Output: Infrared Transmitter Output. General purpose I/O port 3 bit 7.

5.6 Flash ROM Interface

SYMBOL	PIN	I/O	FUNCTION
XA18-XA16 GP57-GP55	66-68	O_{12} I/OD_{12t}	Flash ROM interface Address[18:16] General purpose I/O port 5 bit7-5
XA15-XA10 GP47-GP42	69-74	O_{12} I/OD_{12t}	Flash ROM interface Address[15:10] General purpose I/O port 4 bit7-2
XA9-XA8 GP41-GP40	76-77	O_{12} I/OD_{12t}	Flash ROM interface Address[9:8] General purpose I/O port 4 bit1-0
XA7-XA0 GP37-GP30	78-85	O_{12} I/OD_{12t}	Flash ROM interface Address[7:0] General purpose I/O port 3 bit7-0
XD7-XD4 GP27-GP24	86-89	I/O_{12t} I/OD_{12t}	Flash ROM interface Data Bus[7:4] General purpose I/O port 2 bit7-4
XD3-XD0 GP23-GP20	91-94	I/O_{12t} I/OD_{12t}	Flash ROM interface Data Bus [3:0] General purpose I/O port 2 bit3-0
ROMCS# GP54	95	O_{12} I/OD_{12t}	Flash ROM interface Chip Select General purpose I/O port 5 bit4
MEMR# GP53	96	O_{12} I/OD_{12t}	Flash ROM interface Memory Read Enable General purpose I/O port 5 bit3
MEMW# GP52	97	O_{12} I/OD_{12t}	Flash ROM interface Memory Write Enable General purpose I/O port 5 bit2

5.7 General Purpose I/O Port

SYMBOL	PIN	I/O	FUNCTION
GP73 SIND	111	I/OD_{12t} IN_t	General purpose I/O port 7 bit3 Serial Input. It is used to receive serial data through the communication link.
GP80 WDTO	118	I/OD_{12t} OD_{12}	General purpose I/O port 8 bit0 Watch dog timer output.

5.8 Smart Card Interface

SYMBOL	PIN	I/O	FUNCTION
SCPSNT	107	IN_{ts}	Smart card present detection Schmitt-trigger input.
CTSD#		IN_t	Clear To Send. It is the modem control.
GP77		I/OD_{24t}	General purpose I/O port 7 bit7.
SCIO	108	I/O_{24t}	Smart card data I/O channel.
DSRD#		IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP76		I/OD_{24t}	General purpose I/O port 7 bit6.
SCCLK	109	O_4	Smart card clock output.
RTSD#		O_4	UART C Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
GP75		I/OD_{4t}	General purpose I/O port 7 bit5.
SCRST	110	O_{24}	Smart card reset output.
DTRD#		O_{24}	UART C Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate.
GP74		I/OD_{24t}	General purpose I/O port 7 bit4.
SCC8	112	I/O_{24t}	Smart card General Purpose I/O channel.
SOUTC		O_{24t}	UART B Serial Output. It is used to transmit serial data out to the communication link.
GP72		I/OD_{24t}	General purpose I/O port 7 bit2.
SCPWR	113	O_{12}	Smart card power control.
DCDD#		IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
GP71		I/OD_{12t}	General purpose I/O port 7 bit1.
SCC4	114	I/O_{24t}	Smart card General Purpose I/O channel.
RID#		IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
GP70		I/OD_{24t}	General purpose I/O port 7 bit0.

5.9 PWM & General Purpose I/O Port 8

SYMBOL	PIN	I/O	FUNCTION
PWM2 PLED GP83	115	O_{12} O_{12} I/OD_{12t}	Fan speed control . Use the Pulse Width Modulation (**PWM**) Power LED output, this signal is low after system reset. General purpose I/O port 8 bit2-1
PWM1-0 GP82-81	116-117	O_{12} I/OD_{12t}	Fan speed control . Use the Pulse Width Modulation (**PWM**) Technic knowledge to control the Fan's RPM. General purpose I/O port 8 bit2-1

5.10 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
MSI GP51	119	INcu I/OD_{24c}	MIDI serial data input . General purpose I/O port 5 bit 1.
MSO GP50	120	O_{12} I/OD_{12t}	MIDI serial data output. General purpose I/O port 5 bit 0.
GPAS2 GP17	121	INcs I/OD_{24cs}	Active-low, Joystick I switch input 2. This pin has an internal pull-up resistor. (Default) General purpose I/O port 1 bit 7.
GPBS2 GP16	122	INcs I/OD_{24cs}	Active-low, Joystick II switch input 2. This pin has an internal pull-up resistor. (Default) General purpose I/O port 1 bit 6.
GPAY GP15	123	I/OD_{24a} I/OD24cs	Joystick I timer pin. this pin connect to Y positioning variable resistors for the Josystick. (Default) General purpose I/O port 1 bit 5.
GPBY GP14	124	I/OD_{24a} I/OD_{24cs}	Joystick II timer pin. this pin connect to Y positioning variable resistors for the Josystick. (Default) General purpose I/O port 1 bit 4.
GPBX GP13	125	I/OD_{24a} I/OD_{24cs}	Joystick II timer pin. this pin connect to X positioning variable resistors for the Josystick. (Default) General purpose I/O port 1 bit 3.
GPAX GP12	126	I/OD24a I/OD_{24cs}	Joystick I timer pin. this pin connect to X positioning variable resistors for the Josystick. (Default) General purpose I/O port 1 bit 2.

Game Port & MIDI Port, continued

SYMBOL	PIN	I/O	FUNCTION
GPBS1	127	Incs	Active-low, Joystick II switch input 1. This pin has an internal pull-up resistor. (Default)
GP11		I/OD_{24csu}	General purpose I/O port 1 bit 1.
GPAS1	128	Incs	Active-low, Joystick I switch input 1. This pin has an internal pull-up resistor. (Default)
GP10		I/OD_{24cs}	General purpose I/O port 1 bit 0.

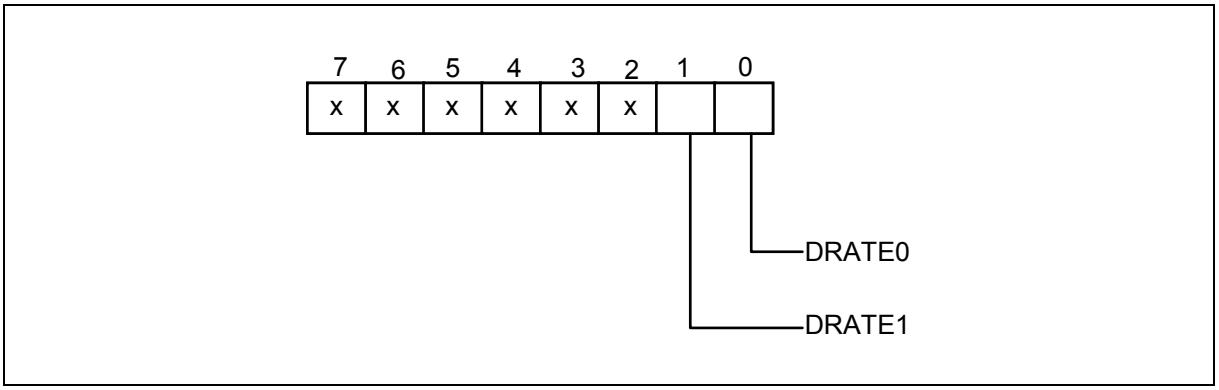
5.11 POWER PINS

SYMBOL	PIN	FUNCTION
VCC	5, 45, 75,	+5V power supply for the digital circuitry.
VCC3V	22	+3.3V power supply for driving 3V on host interface.
GND	18, 60, 90,	Ground.

6. CONFIGURATION REGISTER

6.1 Plug and Play Configuration

The W83697UF uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83697UF, there are eleven Logical Devices (from Logical Device 0 to Logical Device B with the exception of logical device 4 for backward compatibility) which correspond to eleven individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), UART2 (logical device 3), CIR (Consumer IR, logical device 6), GPIO1 (logical device 7), GPIO5(logical device 8),GPIO2 ~GPIO4(logical device 9), ACPI ((logical device A), and Hardware monitor (logical device B). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7.



6.2 Compatible PnP

6.2.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	ADDRESS AND VALUE
0	write 87h to the location 2Eh twice
1	write 87h to the location 4Eh twice

After Power-on reset, the value on RTSA# (pin 49) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 2Eh or 4Eh same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 2Fh or 4Fh).

After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

6.2.2 Extended Functions Enable Registers (EFERs)

After a power-on reset, the W83697UF enters the default operating mode. Before the W83697UF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 2Eh or 4Eh (as described in previous section).

6.2.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers (EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 2Eh or 4Eh on PC/AT systems; the EFDRs are read/write registers with port address 2Fh or 4Fh on PC/AT systems.

6.3 Configuration Sequence

To program W83697UF configuration registers, the following configuration sequence must be followed:

(1). Enter the extended function mode

(2). Configure the configuration registers

(3). Exit the extended function mode

6.3.1 Enter the extended function mode

To place the chip into the extended function mode, two successive wrtites of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

6.3.2 Configurate the configuration registers

The chip selects the logical device and activates the desired logical devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). EFIR is located at the same address as EFER, and EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e.,0x07) to the EFIR and then write the number of the desired logical device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required. Secondly, write the address of the desired configuration register within the logical device to the EFIR and then write (or read) the desired configuration register through EFDR.

6.3.3 Exit the extended function mode

To exit the extended function mode, one write of 0xAA to EFER is required. Once the chip exits the extended function mode, it is in the normal running mode and is ready to enter the configuration mode.

6.3.4 Software programming example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so EFIR is located at 2Eh and EFDR is located at 2Fh. If HEFRAS (CR26 bit 6) is set, 4Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;--------------------------------------------------------------------------------
; Enter the extended function mode, interruptible double-write    |
;--------------------------------------------------------------------------------
MOV     DX,2EH
MOV AL,87H
OUT     DX,AL
OUT     DX,AL
;--------------------------------------------------------------------------------
; Configurate logical device 1, configuration register CRF0   |
;--------------------------------------------------------------------------------
MOV     DX,2EH
MOV     AL,07H
OUT     DX,AL           ; point to Logical Device Number Reg.
MOV     DX,2FH
MOV     AL,01H
OUT     DX,AL           ; select logical device 1
;
MOV     DX,2EH
```

```
MOV     AL,F0H
OUT     DX,AL           ; select CRF0
MOV     DX,2FH
MOV AL,3CH
OUT     DX,AL           ; update CRF0 with value 3CH
;-----------------------------------------
; Exit extended function mode     |
;-----------------------------------------
MOV     DX,2EH
MOV AL,AAH
OUT     DX,AL
```

6.4 Chip (Global) Control Register

CR02 (Default 0x00) (Write only)

Bit [7:1]: Reserved.

Bit 0 = 1 SWRST --> Soft Reset.

CR07

Bit [7:0]: LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20 (read only)

Bit [7:0]: DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0
= 0x 68 (for W83697UF)

CR21 (read only)

DEVREVB7 - DEBREVB0 --> Device Rev
= 0x1X (for W83697UF)

Bit [7:0]:

X : Version change number. (Bit [3:0]) --> begin from 1

CR22 (Default 0xef)

Bit 7: SCPWD

0 Power down

1 No Power down

Bit 6: URDPWD

0 Power down

1 No Power down

Bit 5: URCPWD
- 0 Power down
- 1 No Power down

Bit 4: Reserved

Bit 3: URBPWD
- 0 Power down
- 1 No Power down

Bit 2: URAPWD
- 0 Power down
- 1 No Power down

Bit 1: PRTPWD
- 0 Power down
- 1 No Power down

Bit 0: FDCPWD
- 0 Power down
- 1 No Power down

CR23 (Default 0xfe)

Bit [7:1]: Reserved.

Bit 0: IPD (Immediate Power Down).
When set to 1, it will put the whole chip into power down mode immediately.

CR24 (Default 0s1000ss)

Bit 7: Flash ROM I/F Address Segment (000F0000h ~ 000FFFFFh) enable/disable
- 0 Enable
- 1 Disable

Bit 6: CLKSEL(Enable 48Mhz)
- 0 The clock input on Pin 1 should be 24 MHz.
- 1 The clock input on Pin 1 should be 48 MHz.
  The corresponding power-on setting pin is SOUTB (pin 61).

Bit [5:4]: ROM size select
- 00 1M
- 01 2M
- 10 4M
- 11 Reserved

Bit 3: MEMW# Select (PIN97)

0 MEMW# Disable

1 MEMW# Enable

Bit 2: Flash ROM I/F Address Segment (000E0000h ~ 000EFFFFh) enable/disable

0 Enable

1 Disable

Bit 1: Enable Flash ROM Interface

0 Flash ROM Interface is enabled after hardware reset

1 Flash ROM Interface is disabled after hardware reset
The corresponding power-on setting pin is PENROM#(pin 52)

Bit 0: PNPCSV

0 The Compatible PnP address select registers have default values.

1 The Compatible PnP address select registers have no default value.
The corresponding power-on setting pin is DTRA# (pin 50).

CR25 (Default 0x00)

Bit 7: SCTRI

Bit 6: URDTRI

Bit 5: URCTRI

Bit 4: Reserved

Bit 3: URBTRI

Bit 2: URATRI

Bit 1: PRTTRI

Bit 0: FDCTRI

CR26 (Default 0x00)

Bit 7: SEL4FDD

0 Select two FDD mode.

1 Select four FDD mode.

Bit 6: HEFRAS
These two bits define how to enable Configuration mode. The corresponding power-on setting pin is RTSA #(pin 49).
HEFRAS Address and Value

0 Write 87h to the location 2E twice.

1 Write 87h to the location 4E twice.

Bit 5: LOCKREG

0 Enable R/W Configuration Registers.

1 Disable R/W Configuration Registers.

Bit 4: Reserved

Bit 3: DSFDLGRQ

0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ

1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2: DSPRLGRQ

0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ

1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ

Bit 1: DSUALGRQ

0 Enable UART A/C legacy mode IRQ selecting, then HCR bit 3 is effective on selecting IRQ

1 Disable UART A/C legacy mode IRQ selecting, then HCR bit 3 is not effective on selecting IRQ

Bit 0: DSUBLGRQ

0 Enable UART B/D legacy mode IRQ selecting, then HCR bit 3 is effective on selecting IRQ

1 Disable UART B/D legacy mode IRQ selecting, then HCR bit 3 is not effective on selecting IRQ

CR28 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3]: Flash ROM I/F Address Segment (FFE80000h ~ FFEFFFFFh) enable/disable

0 Disable

1 Enable

Bit [2:0]: PRTMODS2 - PRTMODS0

0xx Parallel Port Mode

100 Reserved

101 External FDC Mode

110 Reserved

111 External two FDC Mode

CR29 (GPIO1,5(50~51) & Game port & MIDI port Select. Default 0x00)

Bit 7: Port Select (select Game Port or General Purpose I/O Port 1)
- 0 Game Port
- 1 General Purpose I/O Port 1 (pin121~128 select function GP10~GP17)

Bit [6:5]: (Pin119)
- 00 MSI
- 01 Reserved
- 10 Reserved
- 11 GP51

Bit [4:3]: (Pin 120)
- 00 MSO
- 01 Reserved
- 10 Reserved
- 11 GP50

Bit 2: Reserved

Bit [1:0]: Reserved

CR2A(GPIO2 ~ 5& Flash ROM Interface Select,
default 0xFF if PENROM# = 0 during POR,
default 0x00 otherwise)

Bit 7: (PIN 86 ~89 & 91 ~94)
- 0 GPIO 2
- 1 Flash IF (xD7 ~ XD0)

Bit 6: (PIN 78 ~ 85)
- 0 GPIO 3
- 1 Flash IF (XA7 ~ XA0)

Bit 5: (PIN 69 ~ 74 & 76 ~77)
- 0 GPIO 4
- 1 Flash IF (XA15 ~ XA10 & XA9 ~ A8)

Bit 4: (PIN 66 ~ 68 & 95 ~ 97)
- 0 GPIO 5(GP52 ~ 57)
- 1 Flash IF(XA18 ~ XA16 , ROMCS#, MEMR #, MEMW#)

Bit [3:0]: Reserved

CR2B(PWM & GPIO8, URC & GPIO6 Select. Default 0x00)

Bit [7]: Reserved.

Bit [6:5]: (Pin115)

00 PWM2

01 PLED

10 Reserved

11 GP83

Bit [4]: (Pin116)

0 PWM1

1 GP82

Bit [3]: (Pin117)

0 PWM0

1 GP81

Bit [2]: (Pin118)

0 WDTO

1 GP80

Bit [1]: (Pin99, Pin100, Pin101, Pin102, Pin105, Pin106)

0 URC(NCTSC, NDSRC, NRTSC, NDTRC, NDCDC, NRIC)

0 GPIO6(GP67, GP66, GP65, GP64, GP61, GP60)

Bit [0]: (Pin103, Pin104)

0 URC(SINC, SOUTC)

1 GPIO6(GP63, GP62)

CR2C(SC & URD & GPIO7 Select. Default 0x30)

Bit [7:6]: (Pin107, Pin108, Pin109, Pin110, Pin113)

00 SC(SCPSNT, SCIO,SCCLK, SCRST, SCPWR)

01 URD(NCTSD,NDSRD, NRTSD, NDTRD, NDCDD)

10 Reserved

11 GPIO7(GP77, GP76, GP75, GP74, GP71)

Bit [5:4]: (Pin111)

00 Reserved

01 SIND

10 Reserved

11 GP73

Bit [3:2]: (Pin112)

00 SCC8

01 SOUTD

10 Reserved

11 GP72

Bit [1:0]: (Pin114)

00 SCC4

01 NRID

10 Reserved

11 GP70

6.5 Logical Device 0 (FDC)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x03, 0xf0 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x06 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for FDC.

CR74 (Default 0x02 if PNPCSV = 0 during POR, default 0x04 otherwise)

Bit [7:3]: Reserved.

Bit [2:0]: These bits select DRQ resource for FDC.

= 0x00 DMA0

= 0x01 DMA1

= 0x02 DMA2

= 0x03 DMA3

= 0x04 - 0x07 No DMA active

CRF0 (Default 0x0E)

FDD Mode Register

FIPURDWN

Bit 7: This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.

0 The internal pull-up resistors of FDC are turned on.(Default)

1 The internal pull-up resistors of FDC are turned off.

Bit 6: INTVERTZ

This bit determines the polarity of all FDD interface signals.

0 FDD interface signals are active low.

1 FDD interface signals are active high.

DRV2EN (PS2 mode only)

Bit 5: When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

Bit 4: Swap Drive 0, 1 Mode

0 No Swap (Default)

1 Drive and Motor select 0 and 1 are swapped.

Bit 3 - 2 Interface Mode

11 AT Mode (Default)

10 (Reserved)

01 PS/2

00 Model 30

Bit 1: FDC DMA Mode

0 Burst Mode is enabled

1 Non-Burst Mode (Default)

Bit 0: Floppy Mode

0 Normal Floppy Mode (Default)

1 Enhanced 3-mode FDD

CRF1 (Default 0x00)

Bit 7 - 6: Boot Floppy

00 FDD A

01 FDD B

10 FDD C

11 FDD D

Bit [5:4]: Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.

Bit [3:2]: Density Select

- 00 Normal (Default)
- 01 Normal
- 10 1 (Forced to logic 1)
- 11 0 (Forced to logic 0)

Bit 1: DISFDDWR

- 0 Enable FDD write.
- 1 Disable FDD write(forces pins WE, WD stay high).

Bit 0: SWWP

- 0 Normal, use WP to determine whether the FDD is write protected or not.
- 1 FDD is always write-protected.

CRF2 (Default 0xFF)

Bit [7:6]: FDD D Drive Type

Bit [5:4]: FDD C Drive Type

Bit [3:2]: FDD B Drive Type

Bit [1:0]: FDD A Drive Type

CRF4 (Default 0x00)

FDD0 Selection:

Bit 7: Reserved.

Bit 6: Precomp. Disable.

- 1 Disable FDC Precompensation.
- 0 Enable FDC Precompensation.

Bit 5: Reserved.

Bit 4 - 3: DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).

- 00 Select Regular drives and 2.88 format
- 01 3-mode drive
- 10 2 Meg Tape
- 11 Reserved

Bit 2: Reserved.

Bit [1:0]: DTYPE0, DTYPE1: Drive Type select (Refer to TABLE B).

CRF5 (Default 0x00)

FDD1 Selection: Same as FDD0 of CRF4.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0(PIN 2)	DRVDEN1(PIN 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

6.6 Logical Device 1 (Parallel Port)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x03, 0x78 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Parallel Port I/O base address.

[0x100:0xFFC] on 4 byte boundary (EPP not supported) or

[0x100:0xFF8] on 8 byte boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR70 (Default 0x07 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Parallel Port.

CR74 (Default 0x03)

Bit [7:3]: Reserved.

Bit [2:0]: These bits select DRQ resource for Parallel Port.

0x00=DMA0
0x01=DMA1
0x02=DMA2
0x03=DMA3
0x04 - 0x07= No DMA active

CRF0 (Default 0x3F)

Bit 7: Reserved.

Bit [6:3]: ECP FIFO Threshold.

Bit [2:0]: Parallel Port Mode (CR28 PRTMODS2 = 0)

100 Printer Mode
000 Standard and Bi-direction (SPP) mode
001 EPP - 1.9 and SPP mode
101 EPP - 1.7 and SPP mode
010 ECP mode
011 ECP and EPP - 1.9 mode
111 ECP and EPP - 1.7 mode (Default)

6.7 Logical Device 2 (UART A)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x03, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x04 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 1.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:2]: Reserved.

Bit [1:0]: SUACLKB1, SUACLKB0

00 UART A clock source is 1.8462 Mhz (24MHz/13)

01 UART A clock source is 2 Mhz (24MHz/12)

10 UART A clock source is 24 Mhz (24MHz/1)

11 UART A clock source is 14.769 Mhz (24mhz/1.625)

6.8 Logical Device 3 (UART B)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x02, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x03 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 2.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:4]: Reserved.

Bit 3: RXW4C

0 No reception delay when SIR is changed from TX mode to RX mode.

1 Reception delays 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2: TXW4C

0 No transmission delay when SIR is changed from RX mode to TX mode.

1 Transmission delays 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit [1:0]: SUBCLKB1, SUBCLKB0

00 UART B clock source is 1.8462 Mhz (24MHz/13)

01 UART B clock source is 2 Mhz (24MHz/12)

10 UART B clock source is 24 Mhz (24MHz/1)

11 UART B clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (Default 0x00)

Bit 7: Reserved.

Bit 6: IRLOCSEL. IR I/O pins' location select.

0 Through SINB/SOUTB.

1 Through IRRX/IRTX.

Bit 5: IRMODE2. IR function mode selection bit 2.

Bit 4: IRMODE1. IR function mode selection bit 1.

Bit 3: IRMODE0. IR function mode selection bit 0.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	tri-state	high
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

Bit 2: HDUPLX. IR half/full duplex function select.

0 The IR function is Full Duplex.

1 The IR function is Half Duplex.

Bit 1: TX2INV.

0 the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.

1 inverse the SOUTB pin of UART B function or IRTX pin of IR function.

Bit 0: RX2INV.

0 the SINB pin of UART B function or IRRX pin of IR function in normal condition.

1 inverse the SINB pin of UART B function or IRRX pin of IR function

6.9 Logical Device 7 (Game Port and GPIO Port 1)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Game/GP1 Port is active.

0 Game/GP1 Port is inactive.

CR60, CR61 (Default 0x02, 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the Game Port base address [0x100:0xFFF] on 8 byte boundary.

CR62, CR63 (Default 0x00, 0x00)

These two registers select the GPIO1 base address [0x100:0xFFF] on 1 byte boundary

O address : CRF1 base address

CRF0 (GP10-GP17 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP10-GP17 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP10-GP17 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

6.10 Logical Device 8 (MIDI Port and GPIO Port 5)

CR30 (MIDI Port Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 MIDI/GP5 port is activate

0 MIDI/GP5 port is inactive.

CR60, CR61 (Default 0x03, 0x30 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the MIDI Port base address [0x100:0xFFF] on 2byte boundary.

CR62, CR63 (Default 0x00, 0x00)

These two registers select the GPIO5 base address [0x100:0xFFF] on 4byte boundary.

IO address : CRF1 base address

IO address + 1 : CRF3 base address

IO address + 2 : CRF4 base address

IO address + 3 : CRF5 base address

CR70 (Default 0x09 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for MIDI Port .

CRF0 (GP5 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP5 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP5 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (PLED mode register. Default 0x00)

Bit [7:3] : Reserved .

Bit 2: select WDTO count mode.

- 0 second
- 1 minute

Bit [1:0]: select PLED mode

- 00 Power LED pin is tri-stated.
- 01 Power LED pin is droved low.
- 10 Power LED pin is a 1Hz toggle pulse with 50 duty cycle.
- 11 Power LED pin is a 1/4Hz toggle pulse with 50 duty cycle.

CRF4 (Default 0x00)

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value.

Bit [7:0]: = 0x00 Time-out Disable
= 0x01 Time-out occurs after 1 second/minute
= 0x02 Time-out occurs after 2 second/minutes
= 0x03 Time-out occurs after 3 second/minutes
.....
= 0xFF Time-out occurs after 255 second/minutes

CRF5 (Default 0x00)

Bit [7] : Reserved .

Bit [6] : invert Watch Dog Timer Status

Bit 5: Force Watch Dog Timer Time-out, Write only*

1 Force Watch Dog Timer time-out event; this bit is self-clearing.

Bit 4: Watch Dog Timer Status, R/W

1 Watch Dog Timer time-out occurred.

0 Watch Dog Timer counting

Bit [3:0]: These bits select IRQ resource for Watch Dog. Setting of 2 selects SMI.

6.11 Logical Device 9 (GPIO Port 2 ~ GPIO Port 4)

CR30 (Default 0x00)

Bit [7:3] Reserved.

Bit 2: 1 GP4 port is active.

0 GP4 port is inactive

Bit 1: 1 GP3 port is active.

0 GP3 port is inactive

Bit 0: 1 GP2 port is active.

0 GP2 port is inactive.

CR60,CR61(Default 0x00,0x00).

These two registers select the GP2,3,4 base address(0x100:FFF) ON 3 bytes boundary.

IO address: CRF1 base address

IO address + 1 : CRF4 base address

IO address + 2 : CRF7 base address

CRF0 (GP2 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP2 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP2 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (GP3 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

CRF4 (GP3 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

CRF5 (GP3 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF6 (GP4 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

CRF7 (GP4 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

CRF8 (GP4 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

6.12 Logical Device A (ACPI)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.
0 Logical device is inactive.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resources for $\overline{SMI}$ / $\overline{PME}$

CRF0 (Default 0x00)

Bit 7: CHIPPME. Chip level auto power management enable.

0 disable the auto power management functions

1 enable the auto power management functions.

Bit 6: Reserved. (Return zero when read)

Bit 5: MIDIPME. MIDI port auto power management enable.

0 disable the auto power management functions

1 enable the auto power management functions.

Bit 4: Reserved. (Return zero when read)

Bit 3: PRTPME. PRT auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 2: FDCPME. FDC auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 1: URAPME. UART A auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 0: URBPME. UART B auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

CRF1 (Default 0x00)

Bit 7: WAK_STS. This bit is set when the chip is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1 to this bit position or by the sleeping/working state machine automatically when the global standby timer expires.

0 the chip is in the sleeping state.

1 the chip is in the working state.

Bit 6: Reserved. (Return zero when read)

Bit 5: MIDI's trap status.

Bit 4: Reserved. (Return zero when read)

Bit 3: PRT's trap status.

Bit 2: FDC's trap status.

Bit 1: URA's trap status.

Bit 0:. URB's trap status

CRF2 (Default 0x00)

Bit [7:3]: Reserved. (Return zero when read)

Bit 2: SC's trap status.

Bit 1: URD's trap status.

Bit 0: URC's trap status.

CRF3 (Default 0x00)

These bits indicate the IRQ status of the individual device respectively. The device's IRQ status bit is set by their source device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 7: URDIRQSTS. URD IRQ status.

Bit 6: URCIRQSTS. URC IRQ status.

Bit [5:4]: Reserved. (Return zero when read)

Bit 3: PRTIRQSTS. PRT IRQ status.

Bit 2: FDCIRQSTS. FDC IRQ status.

Bit 1: URAIRQSTS. UART A IRQ status.

Bit 0: URBIRQSTS. UART B IRQ status.

CRF4 (Default 0x00)

These bits indicate the IRQ status of the individual GPIO function or logical device respectively. The status bit is set by their source function or device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 7: Reserved. (Return zero when read)

Bit 6: SCIRQSTS. SC IRQ status.

Bit [5:3]: Reserved. (Return zero when read)

Bit 2: WDTIRQSTS. Watch dog timer IRQ status.

Bit 1: Reserved. (Return zero when read).

Bit 0: MIDIIRQSTS. MIDI IRQ status.

CRF6 (Default 0x00)

These bits enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to any IRQ of the devices.

$\overline{SMI}/\overline{PME}$ logic output = (PRTIRQEN and PRTIRQSTS) or (FDCIRQEN and FDCIRQSTS)
or (URAIRQEN and URAIRQSTS) or (URBIRQEN and URBIRQSTS)
or (URCIRQEN and URCIRQSTS) or (WDTIRQEN and WDTIRQSTS)
or (URDIRQEN and URDIRQEN) or (MIDIIRQEN and MIDIIRQEN)
or (SCIRQEN and SCIRQEN)

Bit 7: URDIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to URD's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to URD's IRQ.

Bit 6: URCIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to URC's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to URC's IRQ.

Bit [5:4]: Reserved (Return zero when read)

Bit 3: PRTIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to PRT's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to PRT's IRQ.

Bit 2: FDCIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to FDC's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to FDC's IRQ.

Bit 1: URAIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART A's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART A's IRQ.

Bit 0: URBIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART B's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to UART B's IRQ.

CRF7 (Default 0x00)

These bits enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to any IRQ of the devices.

Bit 7: Reserved. (Return zero when read)

Bit 6: SCIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to SC timer's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to SC timer's IRQ.

Bit [5:3]: Reserved. (Return zero when read)

Bit 2: WDTIRQEN.

0 disable the generation of an $\overline{SMI}/\overline{PME}$ interrupt due to watch dog timer's IRQ.

1 enable the generation of an $\overline{SMI}/\overline{SMI}$ interrupt due to watch dog timer's IRQ.

Bit 1: Reserved. (Return zero when read)

Bit 0: MIDIIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

CRF9 (Default 0x00)

Bit [7:3]: Reserved. Return zero when read.

Bit 2: PME_EN: Select the power management events to be either an $\overline{PME}$ or $\overline{SMI}$ interrupt for the IRQ events. Note that: this bit is valid only when SMIPME_OE = 1.

0 the power management events will generate an $\overline{SMI}$ event.

1 the power management events will generate an $\overline{PME}$ event.

Bit 1: FSLEEP: This bit selects the fast expiry time of individual devices.

0 1 S

1 8 mS

Bit 0: SMIPME_OE: This is the $\overline{SMI}$ and $\overline{PME}$ output enable bit.

0 neither $\overline{SMI}$ nor $\overline{PME}$ will be generated. Only the IRQ status bit is set.

1 an $\overline{SMI}$ or $\overline{PME}$ event will be generated.

CRFA (Default 0x00)

Bit [7:3]: Reserved. (Return zero when read)

Bit 2: SCPME. SC auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 1: URDPME. UART D auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 0: URCPME. UART C auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

6.13 Logical Device B (PWM)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x00, 0x00)

These two registers select Pulse Width Modulation base address [0x100:0xFFF] on 8-byte boundary.

6.14 Logical Device C (SMART CARD)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x00, 0x00)

These two registers select Smart Card base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bit select IRQ resource for Smart Card interface.

CRF0 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Smart Card present signal (SCPSNT) is LOW active.

0 SCPSNT is HIGH active.

6.15 Logical Device D (URC & GPIO Port 6)

CR30 (Default 0x00)

Bit [7:2]: Reserved.

Bit 1: 1 Activate GPIO6.

0 GPIO6 is inactive

Bit 0: 1 Activate URC.

0 URC is inactive.

CR60, CR61 (Default 0x03, 0xE8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select the Serial Port 3 I/O base address [0x100:0xFF8] on 8byte boundary.

CR62, CR63 (Default 0x00)

These two registers select the GPIO6 base address [0x100:0xFFF] on 4byte boundary.

IO address: CRF2 base address

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 3.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:2]: Reserved.

Bit [1:0]: SUCCLKB1, SUCCLKB0

00 UART C clock source is 1.8462 Mhz (24MHz/13)

01 UART C clock source is 2 Mhz (24MHz/12)

10 UART C clock source is 24 Mhz (24MHz/1)

11 UART C clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (GP6 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF2 (GP6 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF3 (GP6 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF4 (GP6 output style register. Default 0x00)

When set to a '1', the outgoing port is pulse mode.

When set to a '0', the outgoing port is level mode.

6.16 Logical Device E (URD & GPIO Port 7)

CR30 (Default 0x00)

Bit [7:2]: Reserved.

Bit 1: 1 Activate GPIO7.

0 GPIO7 is inactive

Bit 0: 1 Activate URD.

0 URD is inactive

CR60, CR61 (Default 0x02, 0xE8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select the Serial Port 4 I/O base address [0x100:0xFF8] on 8yte boundary.

CR62, CR63 (Default 0x00)

These two registers select the GPIO7 base address [0x100:0xFFF] on 4byte boundary.

IO address : CRF2 base address

CR70(Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 4.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:2]: Reserved.

Bit [1:0]: SUDCLKB1, SUDCLKB0

00 UART D clock source is 1.8462 Mhz (24MHz/13)

01 UART D clock source is 2 Mhz (24MHz/12)

10 UART D clock source is 24 Mhz (24MHz/1)

11 UART D clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (GP7 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF2 (GP7 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF3 (GP7 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

6.17 Logical Device F (GPIO Port 8)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activate GPIO8.

0 GPIO8 is inactive.

CR60, CR61 (Default 0x00)

These two registers select the GPIO8 base address [0x100:0xFFF] on 2byte boundary.

IO address : CRF1 base address

CRF0 (GP8 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP8 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP8 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

7. SPECIFICATIONS

7.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage (5V)	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
RTC Battery Voltage V_{BAT}	2.2 to 4.0	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 DC CHARACTERISTICS

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	I_{BAT}			2.4	uA	V_{BAT} = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	I_{BAT}			2.0	mA	V_{SB} = 5.0 V, All ACPI pins are not connected.
I/O_{8t} - TTL level bi-directional pin with 8mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 8 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12t} - TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24t} - TTL level bi-directional pin with 24mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12tp3} – 3.3V TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA

DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12tp3} – 3.3V TTL level bi-directional pin with 12mA source-sink capability						
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12ts} - TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24ts} - TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 Ma
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{24tsp3} – 3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{12t} - TTL level bi-directional pin and open-drain output with 12mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24t} - TTL level bi-directional pin and open-drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{24c} - CMOS level bi-directional pin and open drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD_{24a} - Bi-directional pin with analog input and open-drain output with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/OD_{12ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=5V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD$_{24ts}$ - TTL level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						
Input Low Threshold Voltage	Vt-	0.5	0.8	1.1	V	
Input High Threshold Voltage	Vt+	1.6	2.0	2.4	V	
Hystersis	VTH	0.5	1.2		V	VDD=5V
Output Low Voltage	VOL			0.4	V	IOL = 24 mA
Input High Leakage	ILIH			+10	µA	VIN = 5V
Input Low Leakage	ILIL			-10	µA	VIN = 0V
I/OD12cs - CMOS level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	VDD = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	VDD = 5 V
Hystersis	VTH	1.5	2		V	VDD = 5 V
Output Low Voltage	VOL			0.4	V	IOL = 12 mA
Input High Leakage	ILIH			+10	µA	VIN = 5V
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
I/OD16cs - CMOS level Schmitt-trigger bi-directional pin and open drain output with 16mA sink capability						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	VDD = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	VDD = 5 V
Hystersis	VTH	1.5	2		V	VDD = 5 V
Output Low Voltage	VOL			0.4	V	IOL = 16 mA
Input High Leakage	ILIH			+10	µA	VIN = 5V
Input Low Leakage	ILIL			-10	µA	VIN = 0 V
I/OD24cs - CMOS level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	VDD = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	VDD = 5 V

DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD24cs - CMOS level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						
Hysteresis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD12csd - CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	V_{DD} = 5 V
Hysteresis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
I/OD12csu - CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	V_{DD} = 5 V
Hysteresis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
O4 - Output pin with 4mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -4 mA
O8 - Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
O12 - Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA

DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
O_{16} - Output pin with 16mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -16 mA
O_{24} - Output pin with 24mA source-sink capability						
Output Low Voltage	VOL			0.4	V	I_{OL} = 24 mA
Output High Voltage	VOH	2.4			V	I_{OH} = -24 mA
O_{12p3} - 3.3V output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O_{24p3} - 3.3V output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12} - Open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} - Open drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12p3} - 3.3V open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{tp3} - 3.3V TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{td} - TTL level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V

DC CHARACTERISTICS, continued

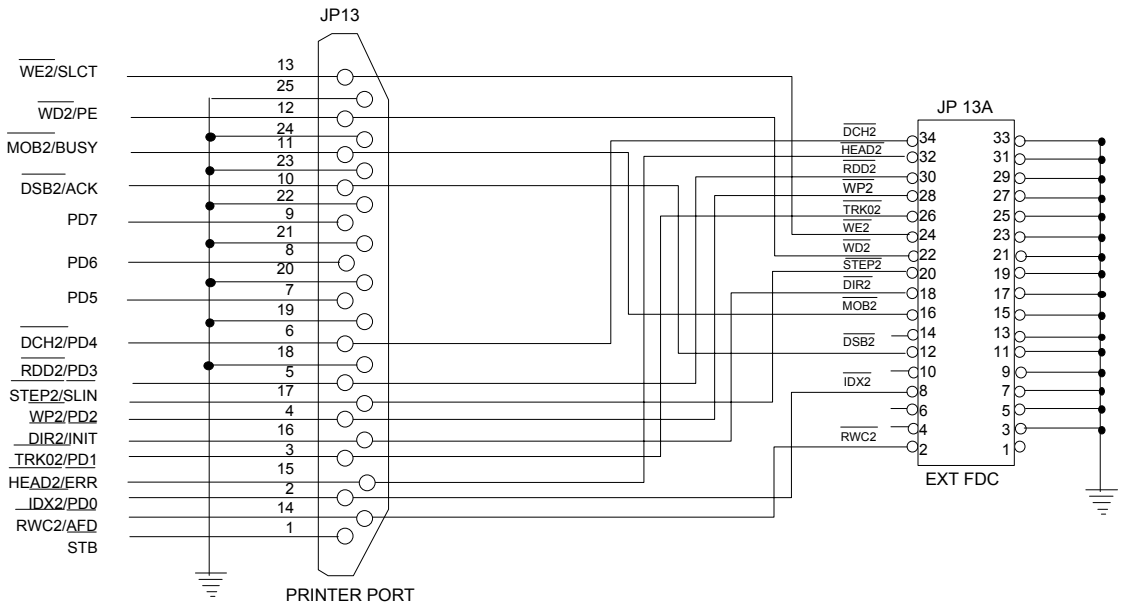
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_{td} - TTL level input pin with internal pull down resistor						
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
INtu - TTL level input pin with internal pull up resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
INts - TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.0	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.8	1.9	2.0	V	V_{DD} = 5 V
Hystersis	V_{TH}	0.8	1.0		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
INtsp3 - 3.3 V TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.0	V	V_{DD} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.8	1.9	2.0	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.8	1.0		V	V_{DD} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
INc - CMOS level input pin						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
INcu - CMOS level input pin with internal pull up resistor						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

DC CHARACTERISTICS, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
IN_{cd} - CMOS level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{cs} - CMOS level Schmitt-trigger input pin						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{csu} - CMOS level Schmitt-trigger input pin with internal pull up resistor						
Input Low Threshold Voltage	Vt-	1.3	1.5	1.7	V	V_{DD} = 5 V
Input High Threshold Voltage	Vt+	3.2	3.5	3.8	V	V_{DD} = 5 V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 5V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

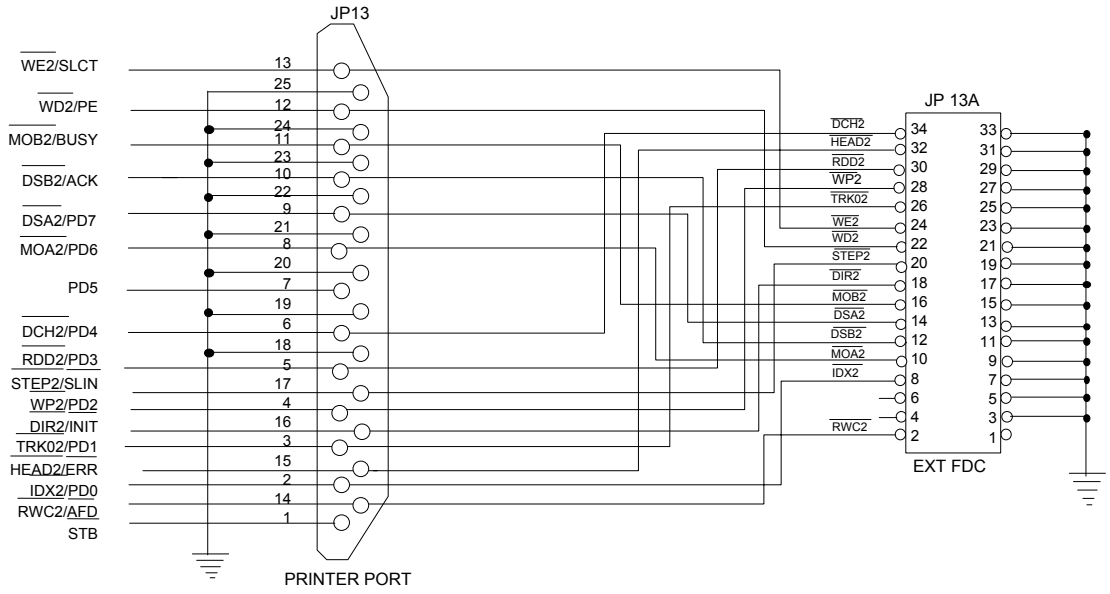
8. APPLICATION CIRCUITS

8.1 Parallel Port Extension FDD



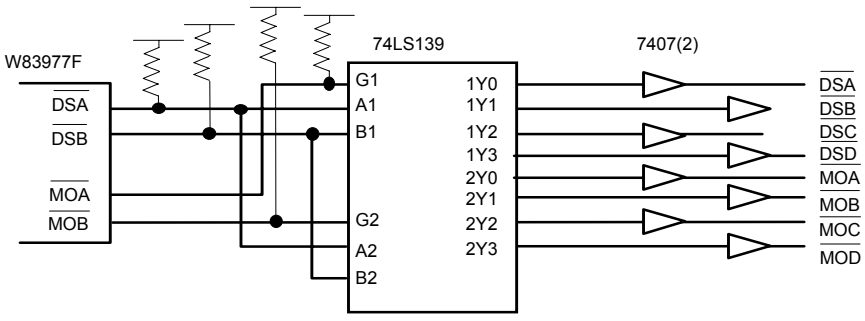
Parallel Port Extension FDD Mode Connection Diagram

8.2 Parallel Port Extension 2FDD



Parallel Port Extension 2FDD Connection Diagram

8.3 Four FDD Mode

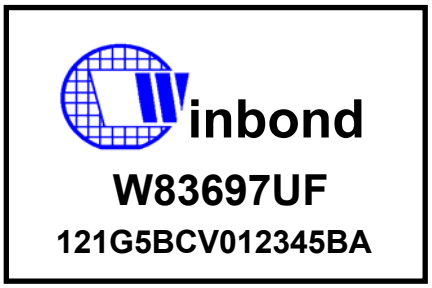


9. ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83697UF,W83697UG	128-pin QFP	W83697UG is with pb-free package

10. HOW TO READ THE TOP MARKING

Example: The top marking of W83697UF/W83697UG

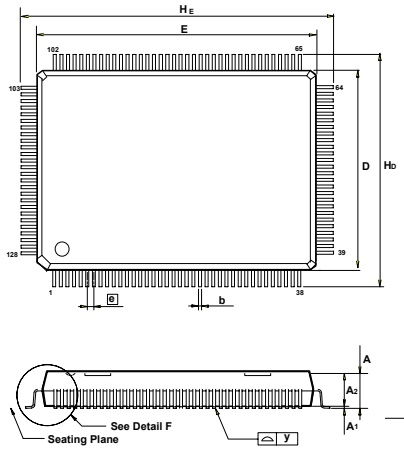


1st line: Winbond logo
2nd line: the type number: W83697UF, W83697UG
3th line: the tracking code 121 G 5 B CV012345BA

121: packages made in 2001, week 21
G: assembly house ID; A means ASE, S means SPIL, G means GR, ... etc.
5: Winbond internal use.
B: IC revision; A means version A, B means version B
CV012345BA: wafer production series lot number

11. PACKAGE DIMENSIONS

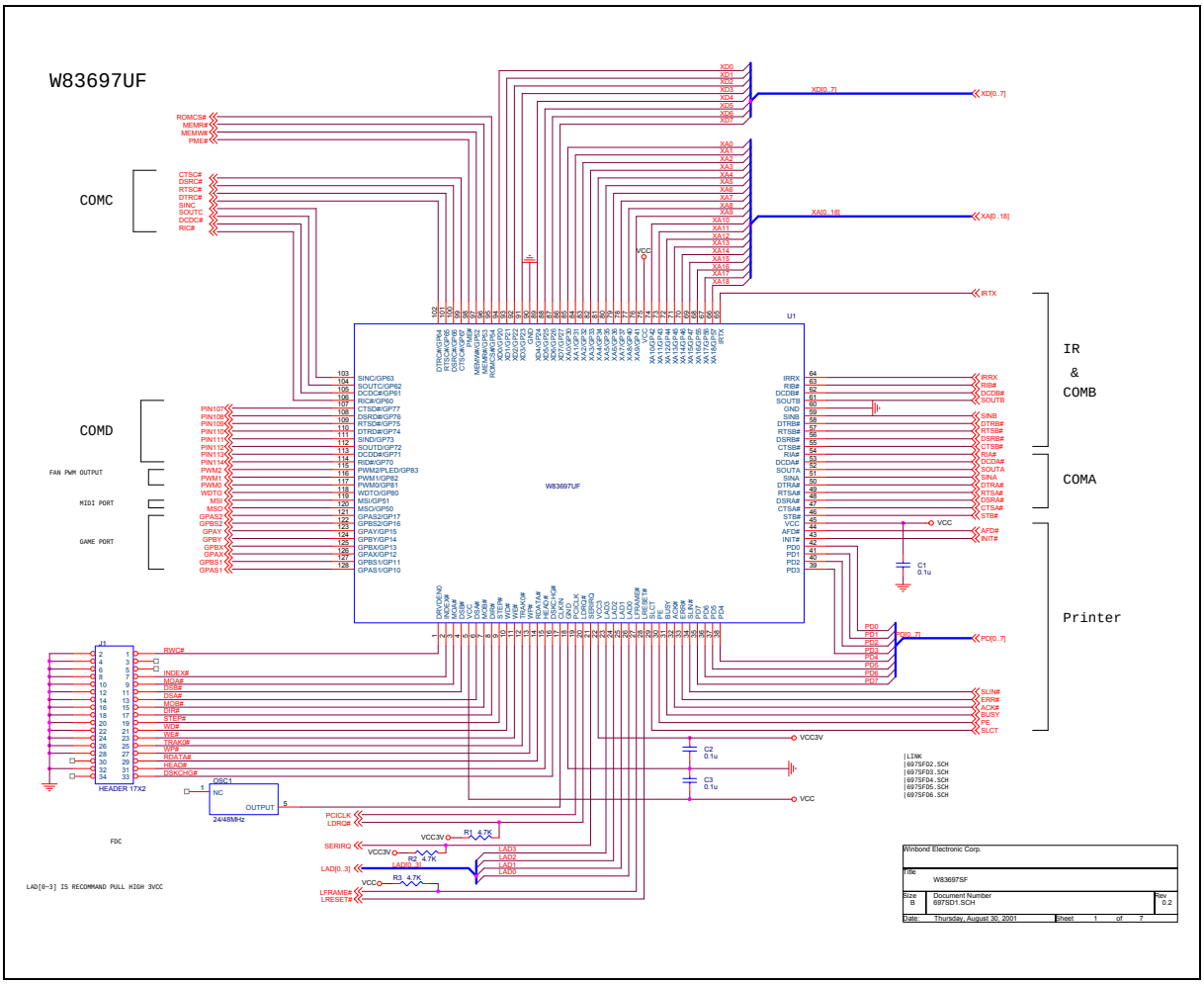
(128-pin PQFP)

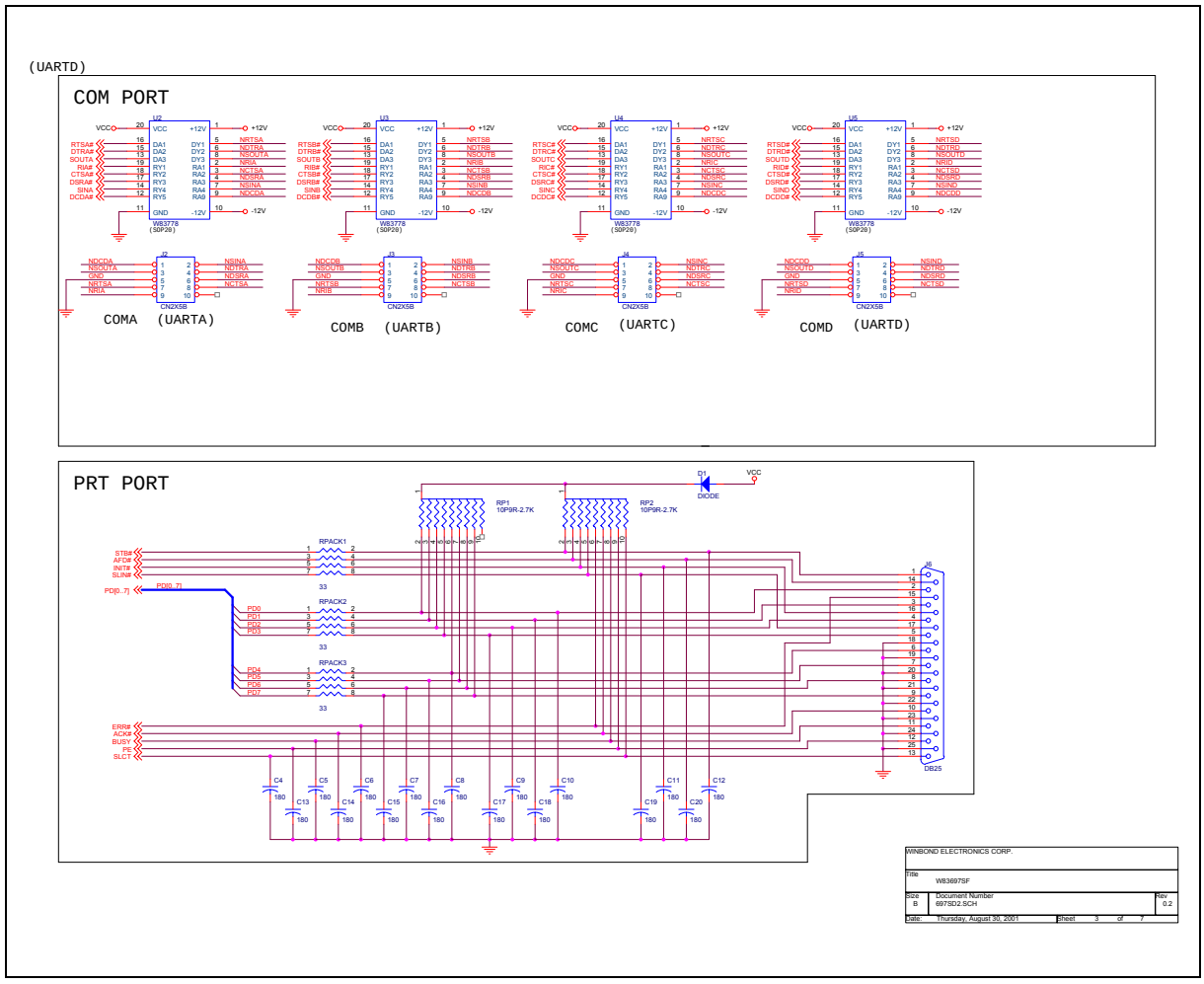


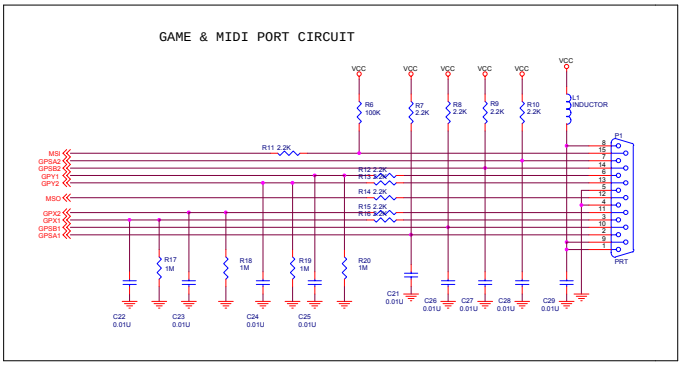
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	——	0.50	——	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	——	1.60	——	—	0.063	—
y	——	——	0.08	—	—	0.003
θ	0	——	7	0	—	7

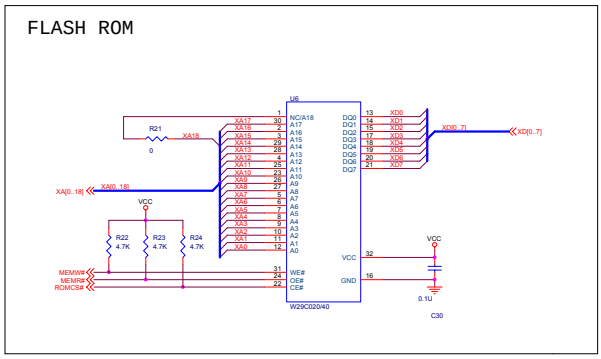
Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

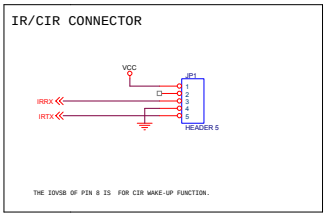
12. APPENDIX A: DEMO CIRCUIT



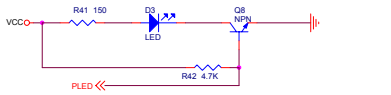

(UARTD)
COM PORT
COMA (UARTA)
COMB (UARTB)
COMC (UARTC)
COMD (UARTD)
PRT PORT
DIODE
RP1 10P9R-2.7K
RP2 10P9R-2.7K
RPACK1
RPACK2
RPACK3
DB25
MINBOND ELECTRONICS CORP.
W83697SF
Thursday, August 30, 2001

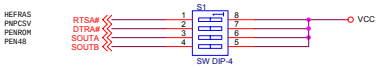






WINBOND ELECTRONICS CORP.			
Title: W83697SF			
Size: B	Document Number: 697SD3.SCH		Rev: 0.2
Date: Thursday, August 30, 2001	Sheet 4 of 7		





	S1 (HEFRAS)	S2 (PNPCSV)	S3 (PENROM)	S4 (PEN48)
ON	4E	Clear all default value	Disable ISA ROM Interface	Using 48M be IO clk
OFF	2E	Using default value	Enable ISA ROM Interface	Using 24M be IO clk

Winbond Electronic Corp.			
Title: W83697SF			
Size: B	Document Number: 697SD4.SCH		Rev: 0.2
Date: Thursday, August 30, 2001	Sheet 5 of 7		

697UF DEMO CIRCUIT VERSION CHANG NOTICE

2/26/2001 FIRST RELEASED

WINBOND ELECTRONICS CORP.			
Title: W83697SF			
Size: B	Document Number: 697SDS.SCH		Rev: 0.2
Date: Thursday, August 30, 2001	Sheet 7 of 7		

13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.50	04/27/01	n.a.	First Published
1.0	12/17/02		New update
1.1	02/18/03	7	Add Block Diagram
1.2	12/01/04		Add Pb-free part no"W83697UG"
A1	May 26, 2005	67	ADD Important Notice

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