The RF MOSFET Line

RF Power Field Effect Transistor

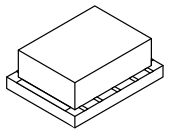
N–Channel Enhancement–Mode

MRF5007
MRF5007R1

7.0 W, 7.5 Vdc
512 MHz
N–CHANNEL
BROADBAND
RF POWER FET

The MRF5007 is designed for broadband commercial and industrial applications at frequencies to 520 MHz. The high gain and broadband performance of this device makes it ideal for large–signal, common source amplifier applications in 7.5 Volt portable FM equipment.

- Guaranteed Performance at 512 MHz, 7.5 Volts
  Output Power = 7.0 Watts
  Power Gain = 10 dB Min
  Efficiency = 50% Min
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- S–Parameter Characterization at High Bias Levels
- Excellent Thermal Stability
- All Gold Metal for Ultra Reliability
- Capable of Handling 20:1 VSWR, @ 10 Vdc, 512 MHz, 2.0 dB Overdrive
- True Surface Mount Package
- Available in Tape and Reel by Adding R1 Suffix to Part Number.
  R1 Suffix = 500 Units per 16 mm, 7 inch Reel.



CASE 430B–02, Style 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	25	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 Meg Ohm)	V_{DGR}	25	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous	I_D	4.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.14	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

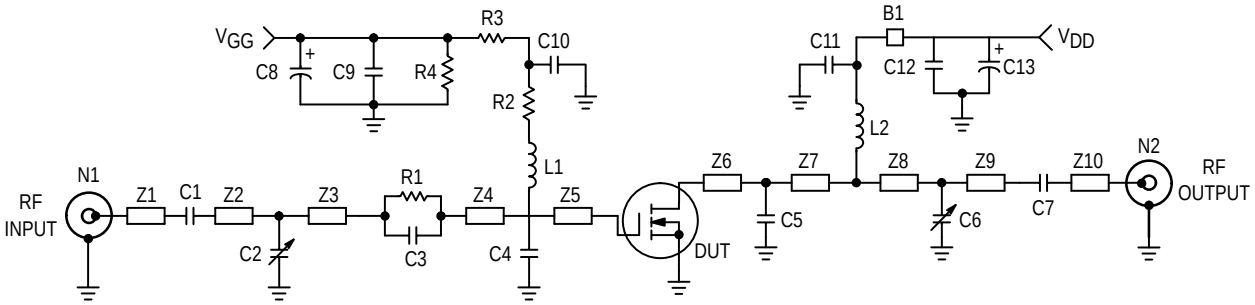
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.8	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 2.5 mAdc)	$V_{(BR)DSS}$	25	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1.0	mAdc
Gate–Source Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 10 mAdc)	$V_{GS(th)}$	1.25	2.2	3.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	—	—	0.3	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1.0 Adc)	g_{fs}	0.9	—	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	32	—	pF
Output Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	63	—	pF
Reverse Transfer Capacitance (V_{DS} = 7.5 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	10	13	16	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain f = 512 MHz (V_{DD} = 7.5 Vdc, P_{out} = 7.0 W, I_{DQ} = 75 mA)	G_{ps}	10	11.5	—	dB
Drain Efficiency f = 512 MHz (V_{DD} = 7.5 Vdc, P_{out} = 7.0 W, I_{DQ} = 75 mA)	η	50	55	—	%



B1	Fair Rite Products Short Ferrite Bead (2743021446)	R3	1.0 kΩ, 0.1 W Chip
C1, C7	100 pF, 100 mil Chip	R4	1.1 MΩ, 1/4 W Carbon
C2, C6	0–20 pF, Johanson	Z1, Z10	0.594″ x 0.08″ Microstrip
C3	47 pF, Miniature Clamped Mica Capacitor	Z2	0.811″ x 0.08″ Microstrip
C4	16 pF, Miniature Clamped Mica Capacitor	Z3	0.270″ x 0.08″ Microstrip
C5	21 pF, Miniature Clamped Mica Capacitor	Z4	0.122″ x 0.08″ Microstrip
C8, C13	10 μF, 50 V, Electrolytic	Z5	0.303″ x 0.08″ Microstrip
C9, C12	0.1 μF, Chip Capacitor	Z6	0.211″ x 0.08″ Microstrip
C10	1000 pF, 100 mil Chip	Z7	0.084″ x 0.08″ Microstrip
C11	140 pF, 100 mil Chip	Z8	0.060″ x 0.08″ Microstrip
L1	7 Turns, 0.076″ ID, #24 AWG Enamel	Z9	1.343″ x 0.08″ Microstrip
L2	5 Turns, 0.126″ ID, #20 AWG Enamel	Board — Glass Teflon®, 31 mils	
N1, N2	Type N Flange Mount	Note: BeCu part locators (0.147″ x 0.093″) soldered onto Z5 and Z6	
R1	39 Ω, 1/4 W Carbon		
R2	30 Ω, 0.1 W Chip		

Figure 1. 512 MHz Narrowband Test Circuit

TYPICAL CHARACTERISTICS

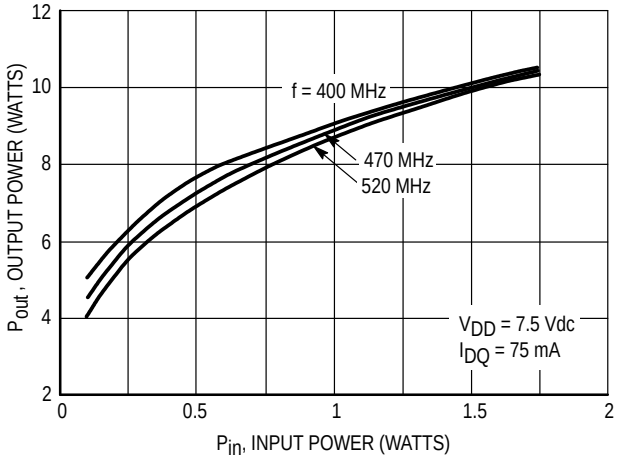


Figure 2. Output Power versus Input Power

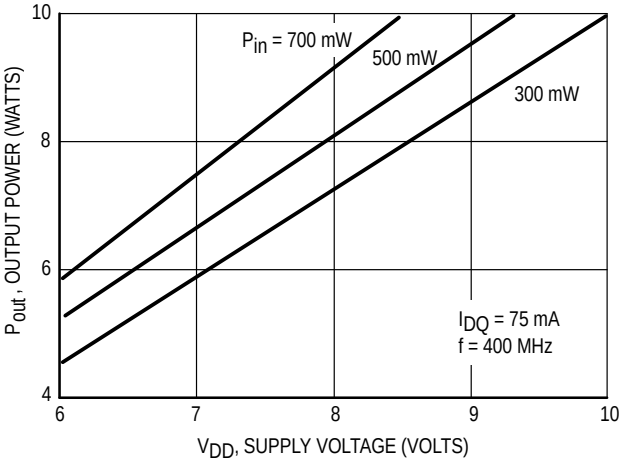


Figure 3. Output Power versus Supply Voltage

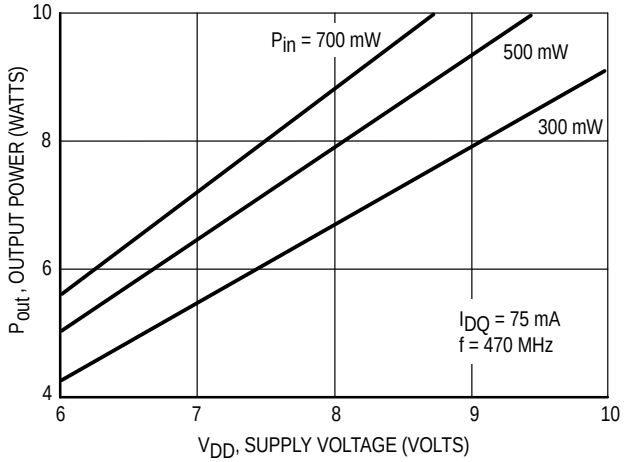


Figure 4. Output Power versus Supply Voltage

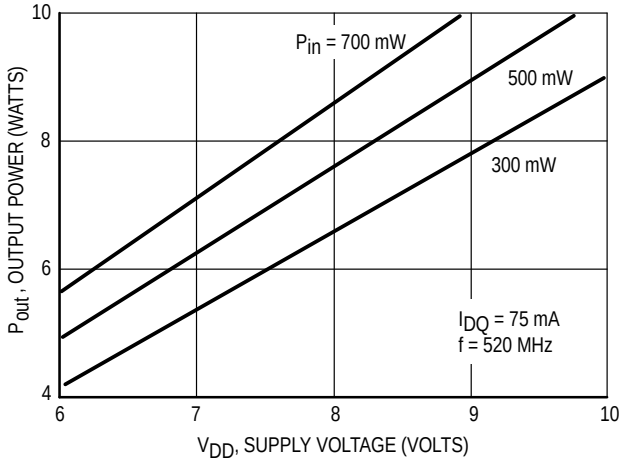


Figure 5. Output Power versus Supply Voltage

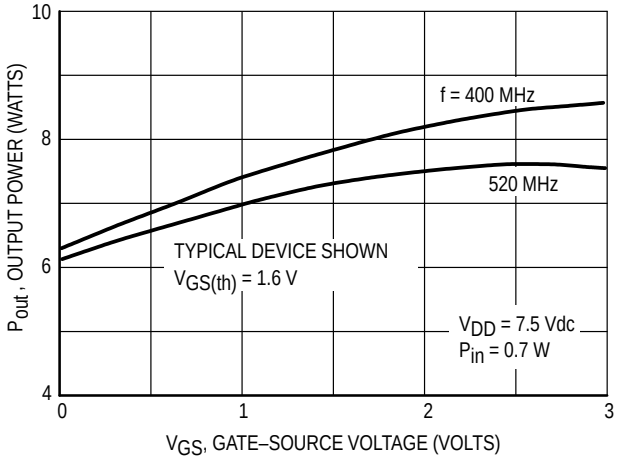


Figure 6. Output Power versus Gate Voltage

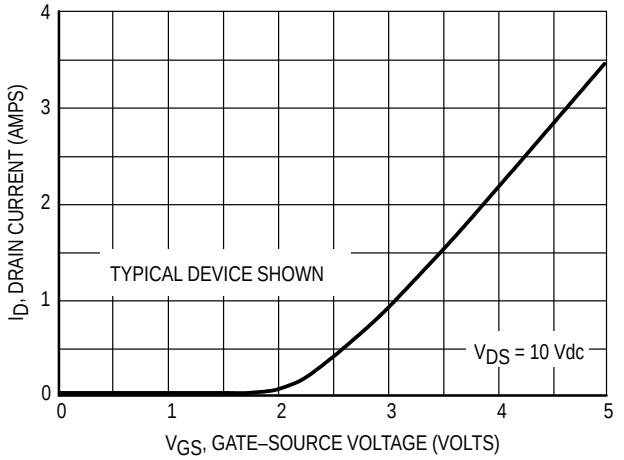


Figure 7. Drain Current versus Gate Voltage

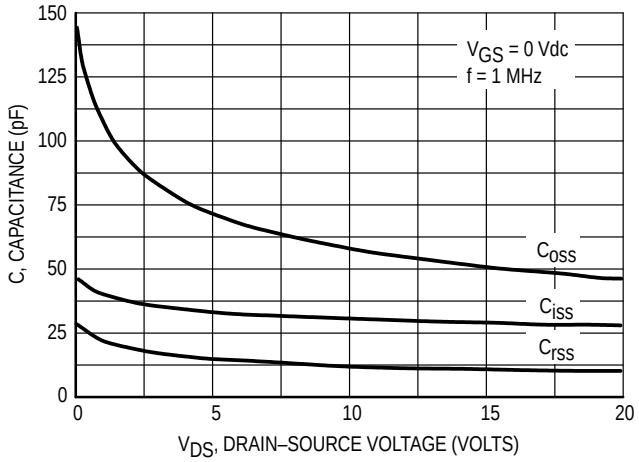


Figure 8. Capacitance versus Voltage

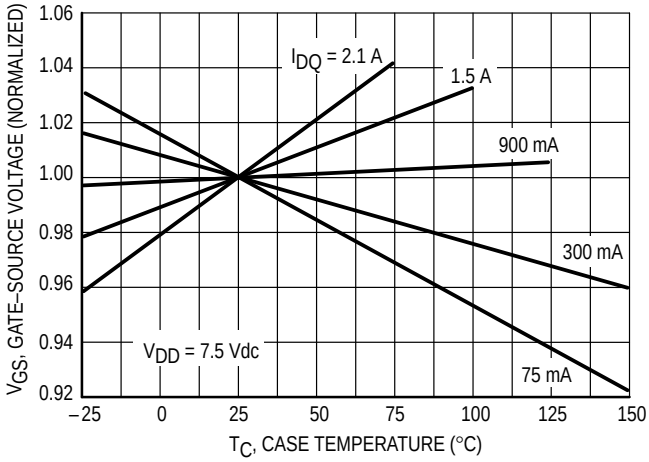


Figure 9. Gate–Source Voltage versus Case Temperature

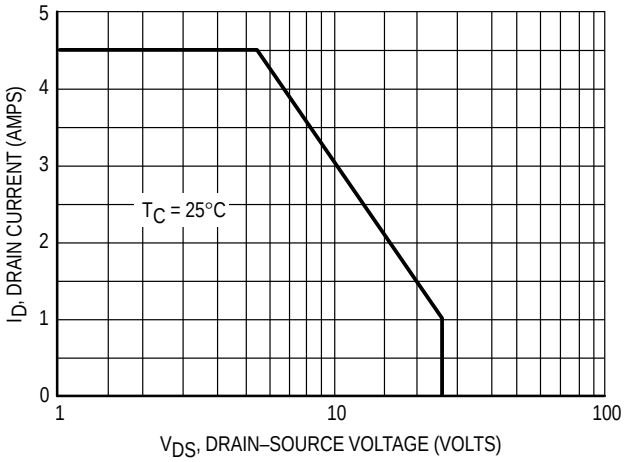
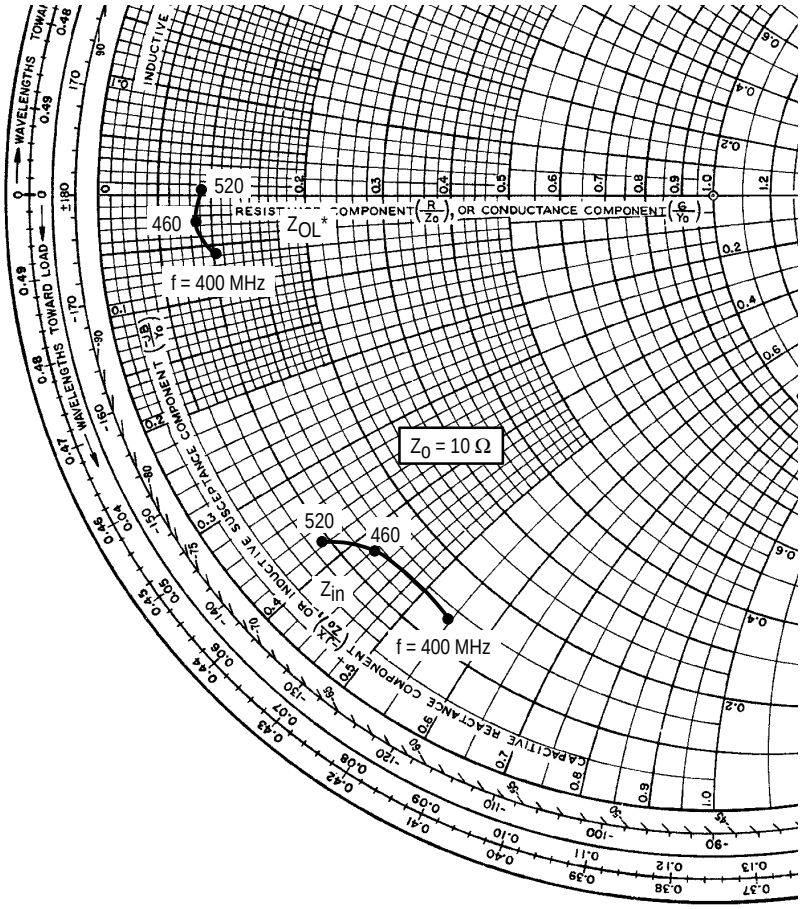


Figure 10. Maximum Rated Forward Biased Safe Operating Area



V_{DD} = 7.5 Vdc, I_{DQ} = 75 mA, P_{out} = 7.0 W

f MHz	Z_{in} Ohms	Z_{OL}* Ohms
400	1.4 – j5.4	1.0 – j0.6
430	1.4 – j4.5	0.9 – j0.5
460	1.3 – j4.2	0.9 – j0.3
490	1.2 – j4.0	0.9 – j0.1
520	1.0 – j3.7	0.9 + j0.1

Z_{in} = Conjugate of source impedance with parallel 39 Ω resistor and 47 pF capacitor in series with gate.

Z_{OL}* = Conjugate of the load impedance at given output power, voltage, frequency, and η_D > 50%.

Note: Z_{OL}* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

Figure 11. Series Equivalent Input and Output Impedance

Table 1. Common Source Scattering Parameters (V_{DS} = 7.5 Vdc)

I_D = 75 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
50	0.75	−132	6.05	103	0.08	15	0.76	−156
100	0.73	−152	3.13	88	0.08	1	0.80	−166
200	0.75	−162	1.52	71	0.08	−13	0.83	−171
300	0.78	−164	0.95	59	0.07	−22	0.85	−172
400	0.81	−166	0.66	49	0.06	−29	0.88	−173
500	0.83	−167	0.49	40	0.06	−35	0.90	−174
700	0.87	−170	0.30	27	0.05	−43	0.93	−175
850	0.89	−171	0.22	19	0.04	−46	0.94	−177
1000	0.91	−173	0.17	13	0.03	−48	0.96	−178
1200	0.92	−174	0.13	7	0.03	−48	0.97	−180

I_D = 500 mA

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
50	0.88	−152	6.89	100	0.03	12	0.87	−172
100	0.87	−166	3.50	91	0.03	4	0.88	−176
200	0.87	−172	1.74	81	0.03	−2	0.89	−178
300	0.87	−175	1.15	74	0.03	−6	0.89	−178
400	0.88	−176	0.84	68	0.03	−8	0.90	−179
500	0.88	−176	0.66	63	0.03	−11	0.90	−179
700	0.89	−177	0.45	53	0.03	−14	0.92	−179
850	0.90	−178	0.35	46	0.03	−15	0.92	−180
1000	0.90	−178	0.28	40	0.02	−15	0.93	179
1200	0.91	−179	0.22	34	0.02	−14	0.94	179

I_D = 1.5 A

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	$\angle\phi$	$\|S_{21}\|$	$\angle\phi$	$\|S_{12}\|$	$\angle\phi$	$\|S_{22}\|$	$\angle\phi$
50	0.91	−155	6.67	99	0.03	11	0.91	−174
100	0.91	−167	3.38	91	0.03	5	0.92	−177
200	0.91	−174	1.69	83	0.03	1	0.92	−179
300	0.91	−176	1.12	77	0.03	−1	0.92	−179
400	0.91	−177	0.83	72	0.02	−2	0.93	−180
500	0.91	−177	0.65	67	0.02	−3	0.93	180
700	0.92	−178	0.45	57	0.02	−4	0.93	179
850	0.92	−178	0.36	51	0.02	−4	0.94	179
1000	0.93	−179	0.29	46	0.02	−3	0.94	178
1200	0.93	−179	0.23	39	0.02	0	0.95	177

DESIGN CONSIDERATIONS

The MRF5007 is a common–source, RF power, N–Channel enhancement mode, Metal–Oxide Semiconductor Field–Effect Transistor (MOSFET). Motorola RF MOSFETs feature a vertical structure with a planar design. Motorola Application Note AN211A, "FETs in Theory and Practice," is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF portable power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

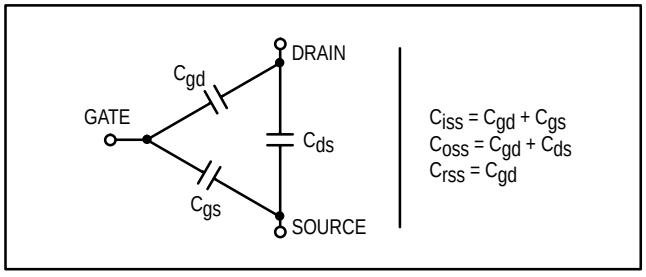
The major advantages of RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain–to–source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate–source voltage and drain current. The drain–source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high — on the order of $10^9\ \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended with appropriate RF decoupling.

Using a resistor to keep the gate–to–source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate–threshold voltage and turn the device on.

DC BIAS

Since the MRF5007 is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. See Figure 7 for a typical plot of drain current versus gate voltage. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. The MRF5007 was characterized at I_{DQ} = 75 mA, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF5007 may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. Figure 6 is an example of output power variation with gate–source bias voltage. This characteristic is very dependent on frequency and load line.

MOUNTING

The specified maximum thermal resistance of 7.0°C/W assumes a majority of the 0.137″ x 0.185″ source contact on the back side of the package is in good contact with an appropriate heat sink. In the test fixture shown in Figure 1, the device is clamped directly to a copper pedestal. As with all RF power devices, the goal of the thermal design should be to minimize the temperature at the back side of the package. It is recomended that this temperature not exceed 100°C for any operating condition. Contact customer service for additional information on thermal considerations for mounting.

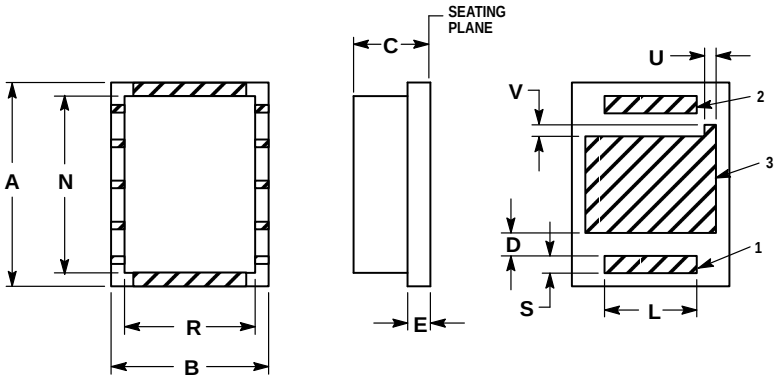
AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar transistors are suitable for the MRF5007. For examples see Motorola Application Note AN721, “Impedance Matching Networks Applied to RF Power Transistors.” Both small–signal S–parameters and large–signal impedances are provided. While the S–parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF power MOSFETs.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of the MRF5007 yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two port stability analysis with the MRF5007 S–parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Motorola Application Note AN215A, “RF Small–Signal Design Using Two–Port Parameters,” for a discussion of two port network theory and stability.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.260	0.270	6.60	6.86
B	0.200	0.210	5.08	5.33
C	0.090	0.104	2.29	2.64
D	0.020	0.040	0.51	1.02
E	0.022	0.028	0.56	0.71
L	0.115	0.125	2.92	3.18
N	0.226	0.236	5.74	5.99
R	0.166	0.176	4.22	4.47
S	0.019	0.029	0.48	0.74
U	0.010	0.020	0.25	0.51
V	0.010	0.020	0.25	0.51

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

CASE 430B–02
ISSUE A

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