DESCRIPTION

PT6306 is a 64-Bit High-Voltage Display Driver utilizing CMOS Technology specially designed for VFD display panels. It provides 64-bit bidirectional shift register, 64-bit latch and high-voltage CMOS Driver. The logic circuit operates on 5V power supply (CMOS Level Input) making it possible for PT6306 to be used in conjunction with a microcomputer. The driver block consists of 80V, 50mA (max.) high voltage output buffer. Pin assignments and application circuits are optimized for easy PCB Layout and cost saving benefits.

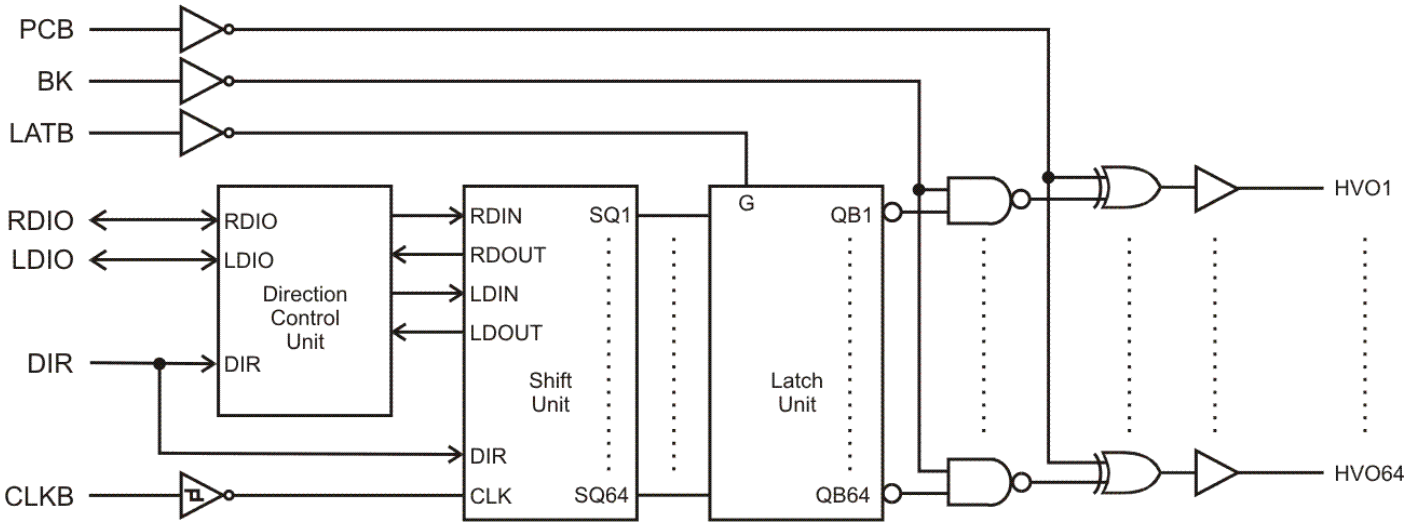
FEATURES

- CMOS Technology
- Low Power Consumption
- 64-Bit Bidirectional shift registers
- Data Controlled via External Transfer Clock and Latch
- High Speed Data Transfer (fmax=25MHz, Min.: 16MHz in cascade connection)
- Wide Operating temperature Range: -40 to +85℃
- High Voltage Output (80V, 50mA max.)
- Polarities of all Drivers may be inverted by using PCB Pin
- Available in COB and 100-pin, QFP

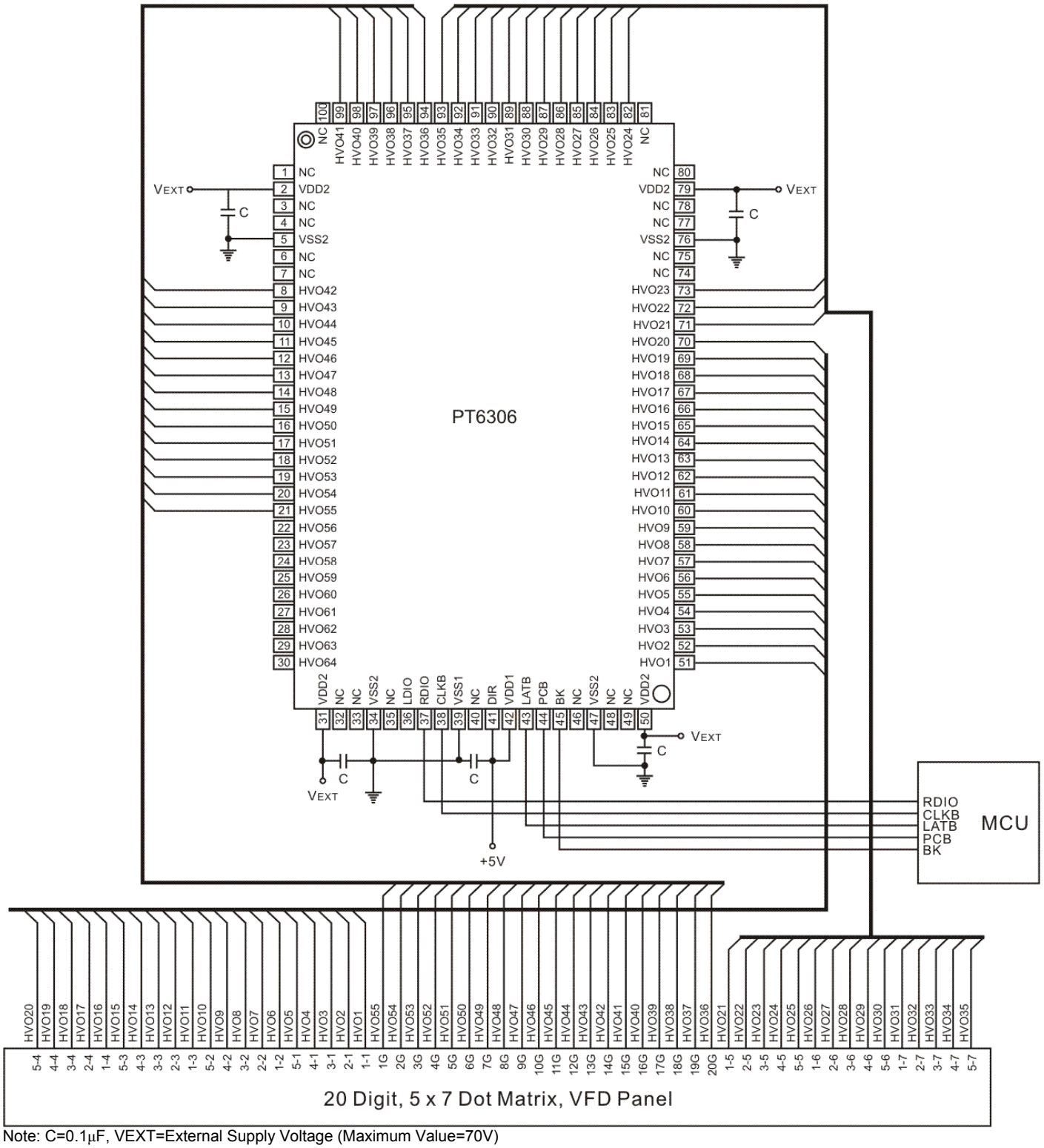
APPLICATION

- Micro Computer Peripheral

BLOCK DIAGRAM



APPLICATION CIRCUIT



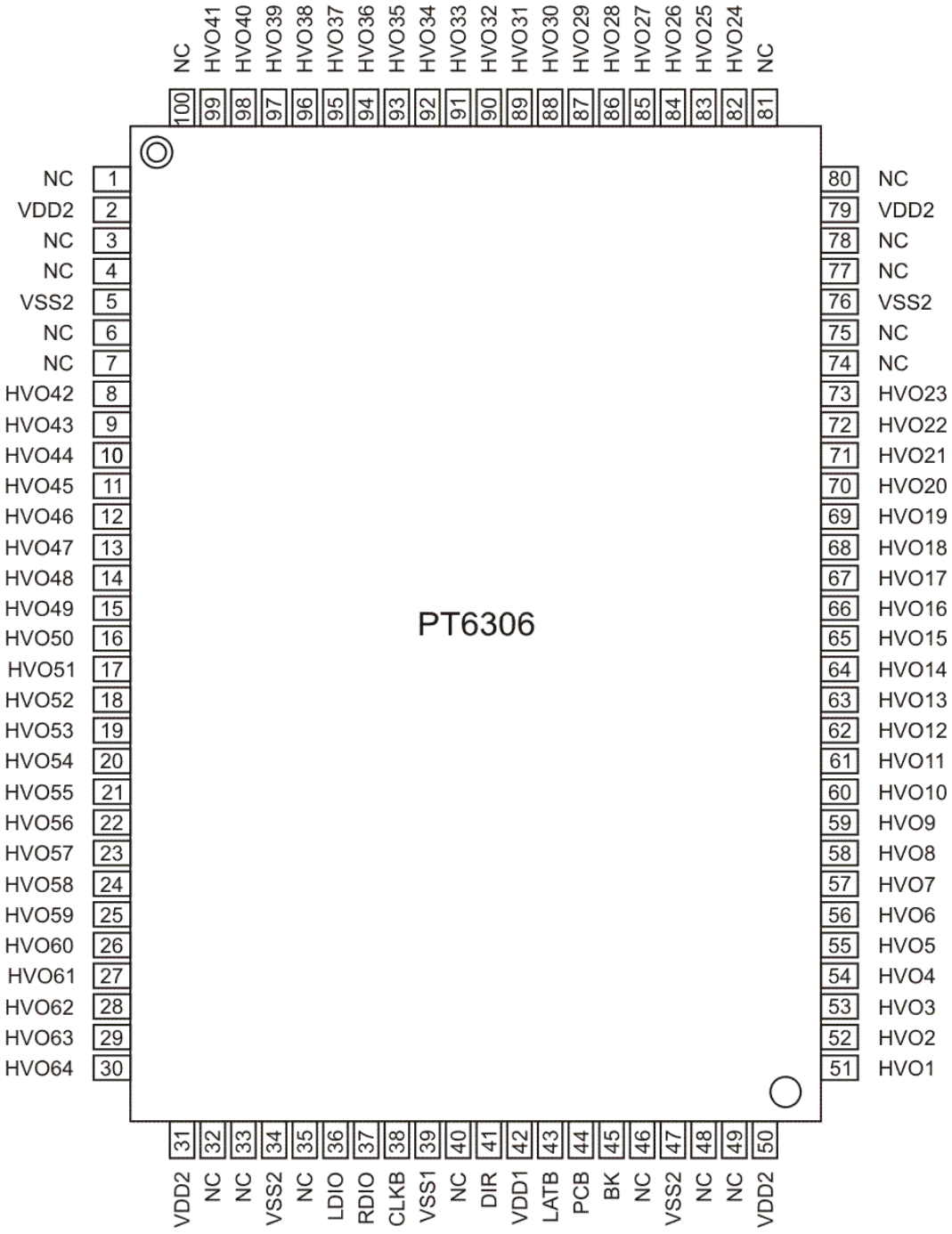
Note: C=0.1μF, VEXT=External Supply Voltage (Maximum Value=70V)

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6306	100 Pins, QFP	PT6306/PT6306-Q
PT6306-H	COB	-

PIN CONFIGURATION

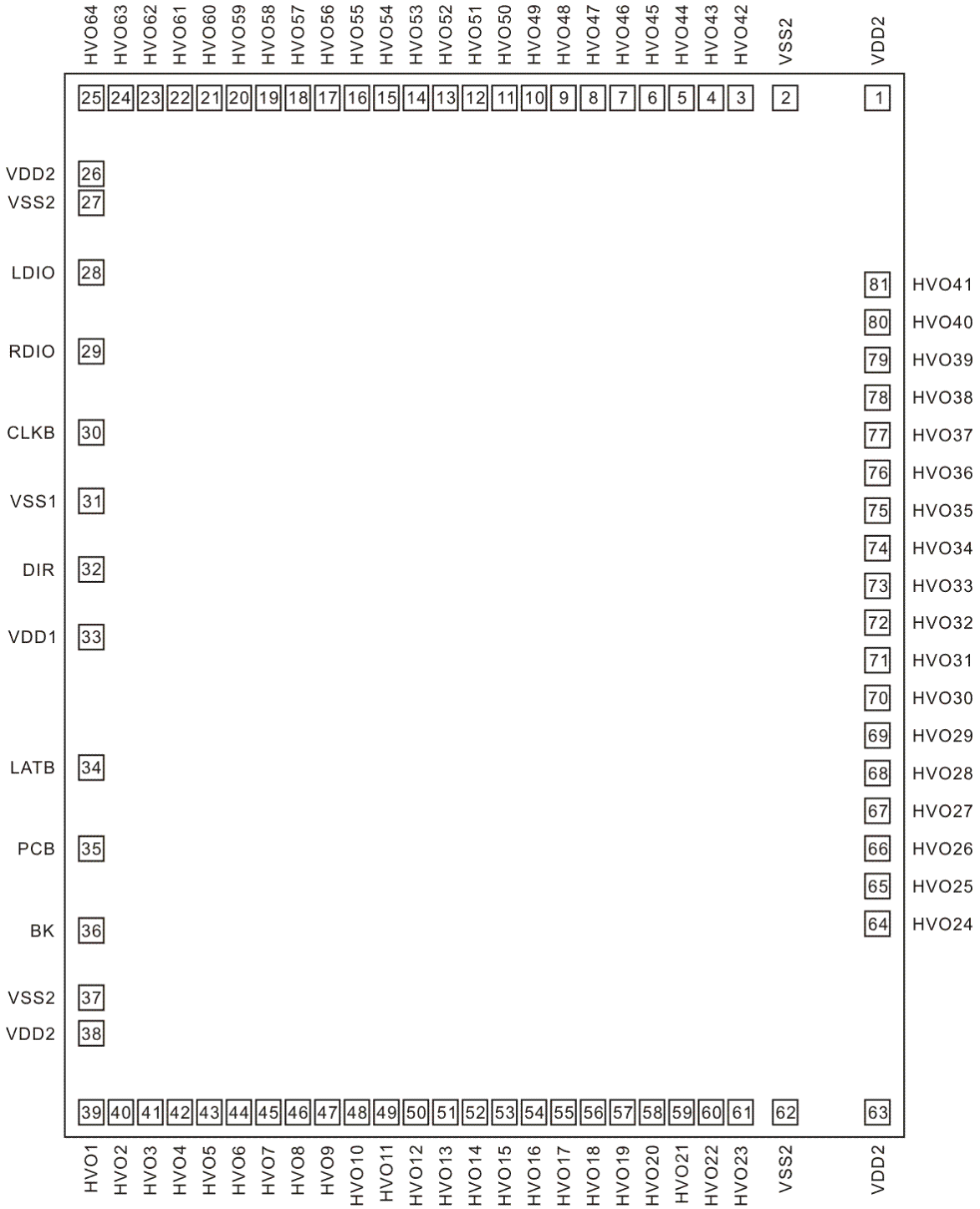
100-PIN, QFP



Pin Name	I/O	Description	Pin No.
VDD2	-	Power Supply: 10 to 70V	2, 31, 50, 79
VSS2	-	Ground	5, 34, 47, 76
HVO1 to HVO23	O	High Voltage Output Pins	51 to 73
HVO24 to HVO41			82 to 99,
HVO42 to HVO64			8 to 30
LDIO	I/O	Left Data I/O Pin	36
RDIO	I/O	Right Data I/O Pin	37
CLKB	I	Clock Input Pin	38
VSS1	-	Ground	39
DIR		Shift Directional Control Input Pin When this pin is set to “H” the Right Shift Mode is active: RDIO→HVO1…..HVO64→LDIO When this pin is set to “L” the Left Shift Mode is active: LDIO→HVO64…..HVO1→RDIO	41
VDD1	-	Power Supply: 5V +10%	42
LATB	I	Latch Strobe Input Pin	43
PCB	I	Reversed Polarity Pin	44
BK	I	Blank Input Pin	45
NC	-	Not Connected	1, 3, 4, 6, 7, 32, 33, 35, 40, 46, 48, 49, 74, 75, 77, 78, 80, 81, 100

Notes:
1. Use all the Power Supply Pins: VDD1, VDD2, VSS1, VSS2 (Make sure that VSS1 and VSS2 Pins have the same voltage level.)
2. Power must be supplied to VDD1, Logic Input and VDD2 so that the device may be protected from any harm caused by latch up. Power must be turned off in a reversed manner. Power ON. OFF sequences must be observed at all times, even during the transition period.

COB


1 VDD2
2 VSS2
3 HVO42
4 HVO43
5 HVO44
6 HVO45
7 HVO46
8 HVO47
9 HVO48
10 HVO49
11 HVO50
12 HVO51
13 HVO52
14 HVO53
15 HVO54
16 HVO55
17 HVO56
18 HVO57
19 HVO58
20 HVO59
21 HVO60
22 HVO61
23 HVO62
24 HVO63
25 HVO64
26 VDD2
27 VSS2
28 LDIO
29 RDIO
30 CLKB
31 VSS1
32 DIR
33 VDD1
34 LATB
35 PCB
36 BK
37 VSS2
38 VDD2
39 HVO1
40 HVO2
41 HVO3
42 HVO4
43 HVO5
44 HVO6
45 HVO7
46 HVO8
47 HVO9
48 HVO10
49 HVO11
50 HVO12
51 HVO13
52 HVO14
53 HVO15
54 HVO16
55 HVO17
56 HVO18
57 HVO19
58 HVO20
59 HVO21
60 HVO22
61 HVO23
62 VSS2
63 VDD2
64 HVO24
65 HVO25
66 HVO26
67 HVO27
68 HVO28
69 HVO29
70 HVO30
71 HVO31
72 HVO32
73 HVO33
74 HVO34
75 HVO35
76 HVO36
77 HVO37
78 HVO38
79 HVO39
80 HVO40
81 HVO41

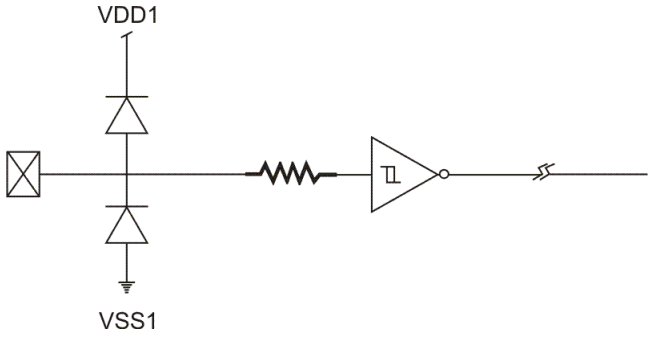
Pin Name	I/O	Description	Pin No.
VDD2	-	Power Supply: 10 to 70V	1, 26, 38, 63
VSS2	-	Ground	2, 27, 37, 62
HVO1 to HVO23	O	High Voltage Output Pins	39 to 61
HVO24 to HVO41			64 to 81
HVO42 to HVO64			3 to 25
LDIO	I/O	Left Data I/O Pin	28
RDIO	I/O	Right Data I/O Pin	29
CLKB	I	Clock Input Pin	30
VSS1	-	Ground	31
DIR		Shift Directional Control Input Pin When this pin is set to “H” the Right Shift Mode is active: RDIO→HVO1…..HVO64→LDIO When this pin is set to “L” the Left Shift Mode is active: LDIO→HVO64…..HVO1→RDIO	32
VDD1	-	Power Supply: 5V +10%	33
LATB	I	Latch Strobe Input Pin	34
PCB	I	Reversed Polarity Pin	35
BK	I	Blank Input Pin	36

Notes:
1. Use all the Power Supply Pins: VDD1, VDD2, VSS1, VSS2 (Make sure that VSS1 and VSS2 Pins have the same voltage level.)
2. Power must be supplied to VDD1, Logic Input and VDD2 so that the device may be protected from any harm caused by latch up. Power must be turned off in a reversed manner. Power ON. OFF sequences must be observed at all times, even during the transition period.

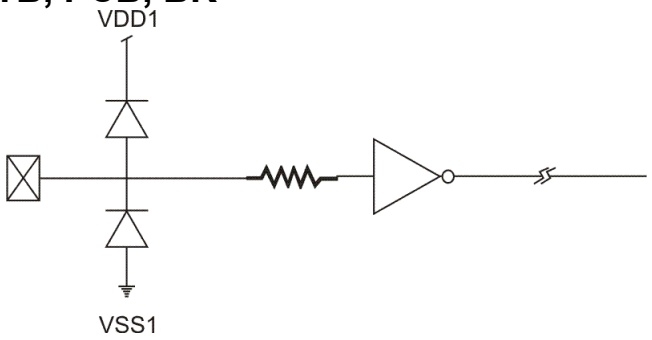
INPUT/OUTPUT PORT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

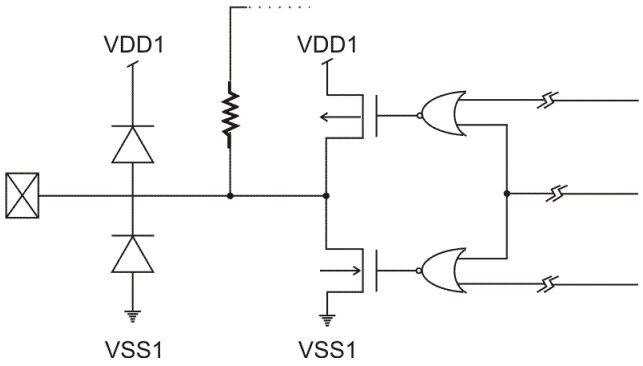
INPUT PIN: CLKB



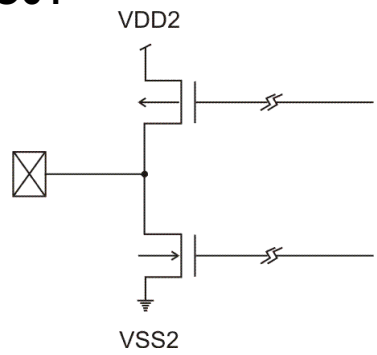
INPUT PINS: DIR, LATB, PCB, BK



INPUT/OUTPUT PINS: RDIO/LDIO



OUTPUT PINS: HVO1 TO HVO64



FUNCTION DESCRIPTION

SHIFT REGISTER TRUTH TABLE

Input		I/O		Shift Register
DIR	CLKB	RDIO	LDIO	
H	↓	Input	Output (see Note1)	Right Shift
H	H or L		Output	Hold
L	↓	Output (see Note2)	Input	Left Shift
L	H or L	Output		Hold

Notes:
1. SQ63 is shifted to the SQ64 position and the output from LDIO at the falling edge of the clock.
2. SQ2 is shifted to the SQ1 position and the output from RDIO at the falling edge of the clock.

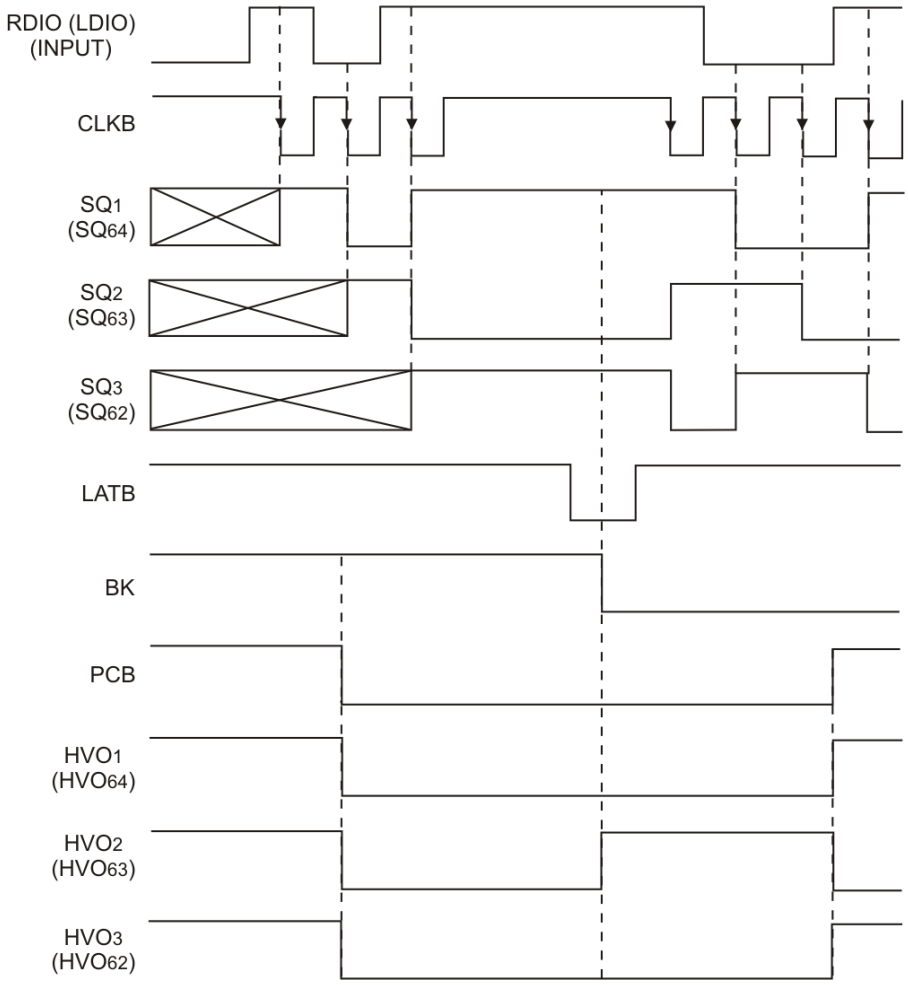
SHIFT REGISTER TRUTH TABLE

Input				Driver Output Stage
RDIO (LDIO)	LATB	BK	PCB	
x	x	H	H	H (All Driver Output are “High”)
x	x	H	L	L (All Driver Output are “Low”)
H	L	L	H	H
H	L	L	L	L
L	L	L	H	L
L	L	L	L	H
x	H	L	H	Output Data immediately before LATB goes to “High”
x	H	L	L	Reverses & Outputs Data immediately before LATB goes to “High”

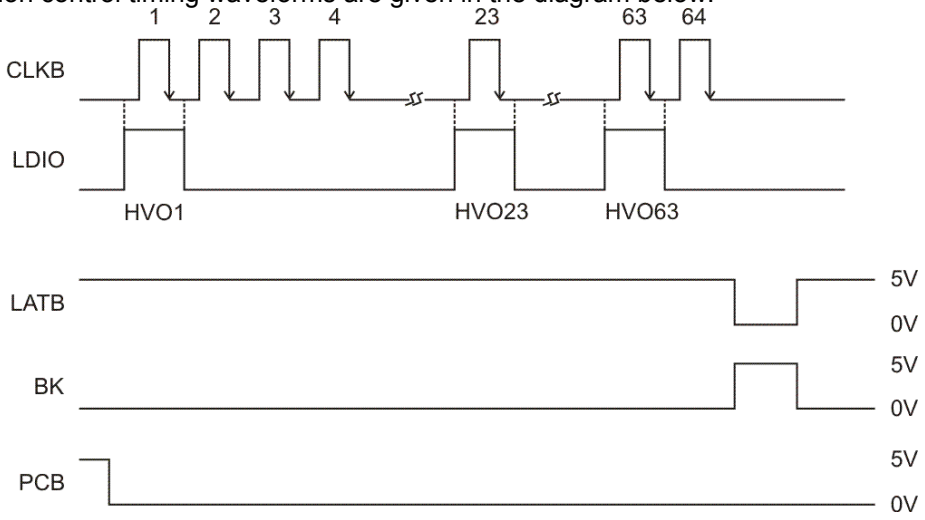
Note: x=“High” or “Low” State, H=“High” State, L=“Low” State.

TIMING CHARACTERISTIC WAVEFORMS

( ): FORDIR = Left



An example of function control timing waveforms are given in the diagram below.



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, Ta=25℃, VSS1=VSS2=0V)

Parameter	Symbol	Rating	Unit
Logic Power Supply Voltage	VDD1	-0.3 ~ +7	V
Logic Input Voltage	V1	-0.3 ~ VDD1+0.3	V
Logic Output Voltage	VO1	-0.3 ~ VDD1+0.3	V
Driver Power Supply Voltage	VDD2	0.3 ~ +80	V
Driver Output Voltage	VO2	-0.3 ~ VDD2+0.3	V
Driver Output Current	IO2	+50	mA
Power Dissipation	PD	1000	mW
Operating Temperature	Topr	-40 ~ +85	℃
Storage Temperature	Tstg	-65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, Topr=-40 to +85℃, VSS1=VSS2=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Power Supply Voltage	VDD1	3.0	5.0	5.5	V
High Level Input Voltage	VIH	0.8VDD1	-	VDD1	V
Low Level Input Voltage	VIL	0	-	0.2VDD1	V
Driver Power Supply Voltage	VDD2	10	-	70	V
Driver Output Current	IOL2	-	-	+40	mA
	IOH2	-	-	-40	mA

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, VDD1=3.3V/5.0V, VDD2=70V, VSS1=VSS2=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Level Output Voltage	VOH1	Logic IOH1=-1.0mA	0.9VDD1	-	-	V
Low Level Output Voltage	VOL1	Logic IOL1=1.0mA	-	-	0.1VDD1	V
High Level Output Voltage	VOH21	HVO1 to HVO64, IOH2=-1.0mA	69	-	-	V
	VOH22	HVO1 to HVO64, IOH2=-10.0mA	65	-	-	V
Low Level Output Voltage	VOL21	HVO1 to HVO64, IOL2=5.0mA	-	-	1.0	V
	VOL22	HVO1 to HVO64, IOL2=40.0mA	-	-	10	V
High Level Input Current	IIH	VI=VDD1	-	-	1.0	μA
Low Level Input Current	IIL	VI=0V	-	-	-1.0	μA
High Level Input Voltage	VIH	Logic	0.8VDD1	-	-	V
Low Level Input Voltage	VIL	Logic	-	-	0.2VDD1	V
State Current Dissipation	IDD11	Logic, Ta=25℃	-	-	10	μA
	IDD12	Logic, Topr=-40 to +85℃	-	-	100	μA
	IDD21	Driver, Ta=25℃	-	-	100	μA
	IDD22	Driver, Topr=-40 to +85℃	-	-	1000	μA

SWITCHING CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, VDD1=3.3V/5.0V, VDD2=70V, VSS1=VSS2=0V, Logic C_L=15pF, Driver C_L=50pF)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation Delay Time	tPHL1	CLKB→RDIO/LDIO	-	-	50	ns
	tPLH1		-	-	50	ns
	tPHL2	VDD1=3.3V CLKB→HVO1 to HVO64	-	-	1000	ns
		VDD1=5.0V CLKB→HVO1 to HVO64			160	
	tPLH2	VDD1=3.3V CLKB→HVO1 to HVO64	-	-	700	ns
		VDD1=5.0V CLKB→HVO1 to HVO64			160	
	tPHL3	VDD1=3.3V LATB→HVO1 to HVO64	-	-	1000	ns
		VDD1=5.0V LATB→HVO1 to HVO64			150	
	tPLH3	VDD1=3.3V LATB→HVO1 to HVO64	-	-	700	ns
		VDD1=5.0V LATB→HVO1 to HVO64			150	
	tPHL4	VDD1=3.3V BK→HVO1 to HVO64	-	-	1000	ns
		VDD1=5.0V BK→HVO1 to HVO64			145	
	tPLH4	VDD1=3.3V BK→HVO1 to HVO64	-	-	700	ns
		VDD1=5.0V BK→HVO1 to HVO64			145	
	tPHL5	VDD1=3.3V PCB→HVO1 to HVO64	-	-	1000	ns
		VDD1=5.0V PCB→HVO1 to HVO64			140	
	tPLH5	VDD1=3.3V PCB→HVO1 to HVO64	-	-	700	ns
		VDD1=5.0V PCB→HVO1 to HVO64			140	
Rise Time	tTLH	VDD=5V HVO1 to HVO64	-	-	100	ns
		VDD=3.3V HVO1 to HVO64	-	-	200	
Fall Time	tTHL	VDD=5V HVO1 to HVO64	-	-	100	ns
		VDD=3.3V HVO1 to HVO64	-	-	300	
Clock Frequency	f	Duty=50%, data loading	-	-	25	MHz
		In Cascade Connection	-	-	16	MHz
Input Capacitance	CI	-	-	-	20	pF

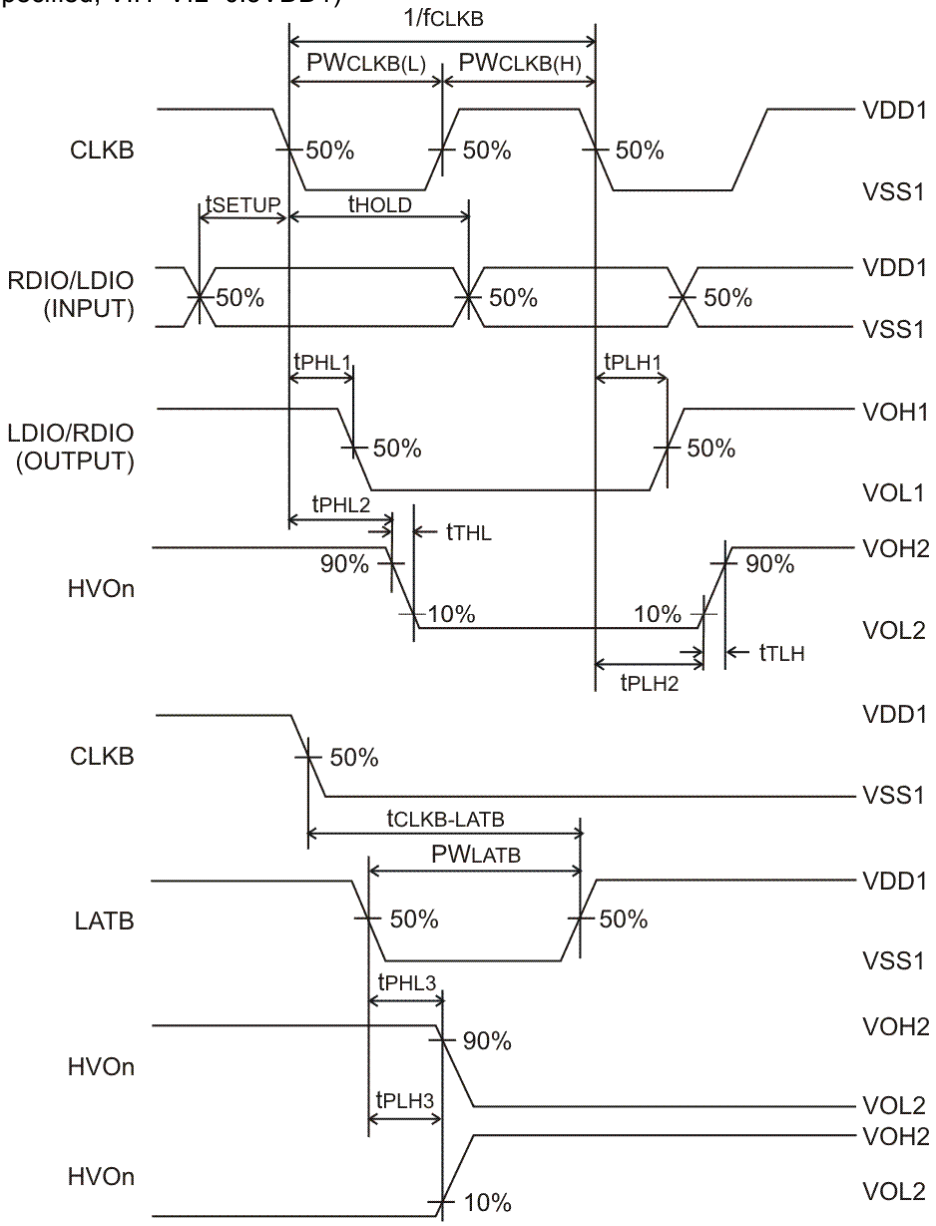
TIMING CHARACTERISTICS

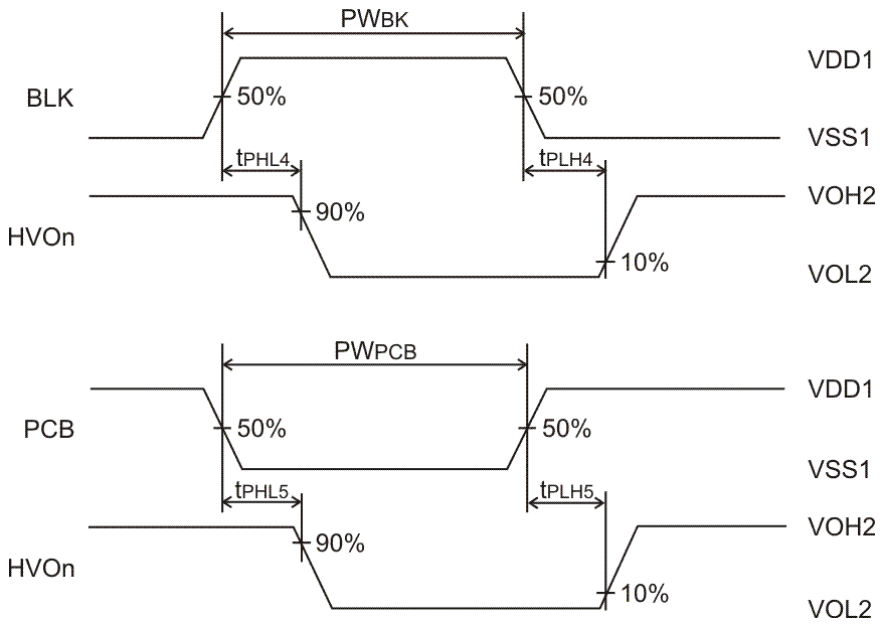
(Unless otherwise specified, Topr=-40 to +80℃, VDD1=3.3 to 5.0 V, VSS1=VSS2=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Pulse Width	PWCLKB (L), (H)	-	20	-	-	ns
Strobe Pulse Width	PWLATB	-	20	-	-	ns
Blank Pulse Width	PWBK	-	200	-	-	ns
PCB Pulse Width	PWPCB	-	200	-	-	ns
Data Setup Time	tSETUP	-	10	-	-	ns
Data Hold Time	tHOLD	-	10	-	-	ns
Clock-Strobe Time	tCLKB-LATB	CLKB↓ → LATB↑	50	-	-	ns

SWITCHING CHARACTERISTICS WAVEFORMS

(Unless otherwise specified, VIH=VIL=0.5VDD1)

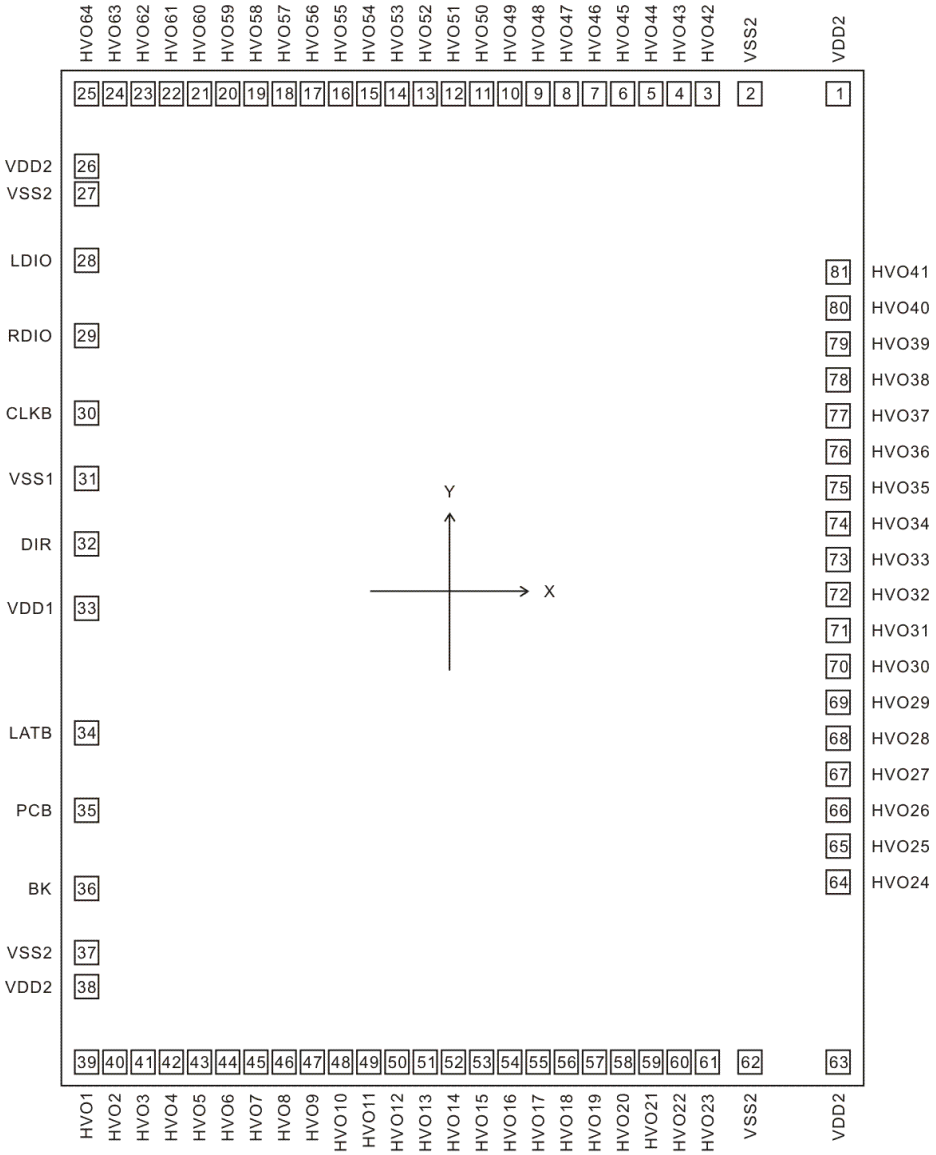



PWBK
BLK
50%
50%
VDD1
VSS1
tPHL4
tPLH4
VOH2
90%
HVOn
10%
VOL2
PWPCB
PCB
50%
50%
VDD1
VSS1
tPHL5
tPLH5
VOH2
90%
HVOn
10%
VOL2

PAD CONFIGURATION

(unit: μm)

. Die Size: X=2654±5
Y=3240±5
(Extended Buffer)
. Driver Pad Size: X=70
Y=70
. Driver Pad Pitch: 90
. Logic Pad Size: 70 x 70



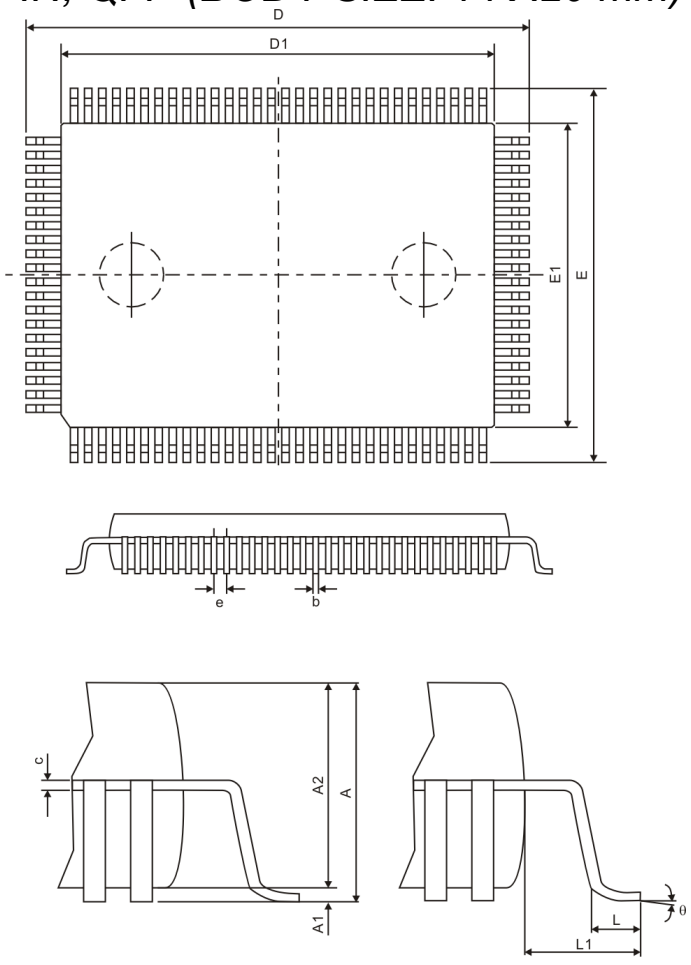
PAD LOCATION

Pad No.	Pad Name	Location
1	VDD2	[1217, 1510]
2	VSS2	[853, 1510]
3	HVO42	[763, 1510]
4	HVO43	[673, 1510]
5	HVO44	[583, 1510]
6	HVO45	[493, 1510]
7	HVO46	[403, 1510]
8	HVO47	[313, 1510]
9	HVO48	[223, 1510]
10	HVO49	[133, 1510]
11	HVO50	[43, 1510]
12	HVO51	[-47, 1510]
13	HVO52	[-137, 1510]
14	HVO53	[-227, 1510]
15	HVO54	[-317, 1510]
16	HVO55	[-407, 1510]
17	HVO56	[-497, 1510]
18	HVO57	[-587, 1510]
19	HVO58	[-677, 1510]
20	HVO59	[-767, 1510]
21	HVO60	[-857, 1510]
22	HVO61	[-947, 1510]
23	HVO62	[-1037, 1510]
24	HVO63	[-1127, 1510]
25	HVO64	[-1217, 1510]
26	VDD2	[-1217, 1287.2]
27	VSS2	[-1217, 1197.2]
28	LDIO	[-1217, 1011.8]
29	RDIO	[-1217, 735.5]
30	CLKB	[-1217, 479.3]
31	VSS1	[-1217, 283.7]
32	DIR	[-1217, 88.1]
33	VDD1	[-1217, -97.3]
34	LATB	[-1217, -479.3]
35	PCB	[-1217, -735.5]
36	BK	[-1217, -1011.8]
37	VSS2	[-1217, -1197.2]
38	VDD2	[-1217, -1287.2]
39	HVO1	[-1217, -1510]
40	HVO2	[-1127, -1510]
41	HVO3	[-1037, -1510]
42	HVO4	[-947, -1510]
43	HVO5	[-857, -1510]
44	HVO6	[-767, -1510]
45	HVO7	[-677, -1510]
46	HVO8	[-587, -1510]
47	HVO9	[-497, -1510]
48	HVO10	[-407, -1510]
49	HVO11	[-317, -1510]
50	HVO12	[-227, -1510]
51	HVO13	[-137, -1510]
52	HVO14	[-47, -1510]

Pad No.	Pad Name	Location
53	HVO15	[43, -1510]
54	HVO16	[133, -1510]
55	HVO17	[223, -1510]
56	HVO18	[313, -1510]
57	HVO19	[403, -1510]
58	HVO20	[493, -1510]
59	HVO21	[583, -1510]
60	HVO22	[673, -1510]
61	HVO23	[763, -1510]
62	VSS2	[853, -1510]
63	VDD2	[1217, -1510]
64	HVO24	[1213.9, -940.1]
65	HVO25	[1213.9, -829.5]
66	HVO26	[1213.9, -718.9]
67	HVO27	[1213.9, -608.3]
68	HVO28	[1213.9, -497.7]
69	HVO29	[1213.9, -387.1]
70	HVO30	[1213.9, -276.5]
71	HVO31	[1213.9, -165.9]
72	HVO32	[1213.9, -55.3]
73	HVO33	[1213.9, 55.3]
74	HVO34	[1213.9, 165.9]
75	HVO35	[1213.9, 276.5]
76	HVO36	[1213.9, 387.1]
77	HVO37	[1213.9, 497.7]
78	HVO38	[1213.9, 608.3]
79	HVO39	[1213.9, 718.9]
80	HVO40	[1213.9, 829.5]
81	HVO41	[1213.9, 940.1]

PACKAGE INFORMATION

100-PIN, QFP (BODY SIZE: 14 X20 mm)



Symbol	Min.	Nom.	Max.
A	-	-	3.40
A1	0.00	-	0.25
A2	2.55	2.80	3.05
b	0.22	0.30	0.33
c	0.13	-	0.17
e	0.65BSC.		
D	23.90BSC.		
D1	20.00BSC.		
E	17.90BSC.		
E1	14.00BSC.		
L	0.73	0.88	1.03
L1	0.95REF.		
θ	0°	-	7°

Notes:
1. Refer to JEDEC MO-112 CC-1
2. All dimensions are in millimeter.

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

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