1 Gb NAND Flash
H27U1G8F2B

Document Title

1 Gbit (128 M x 8 bit) NAND Flash Memory

Revision History

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<tr><td>0.0</td><td>Initial Draft.</td><td>May. 13. 2008</td><td>Preliminary</td></tr>
<tr><td>0.1</td><td>1) Correct Table 5. Mode Selection.
<table><tr><th>CLE</th><th>ALE</th><th>$\overline{CE}$</th><th>$\overline{WE}$</th><th>$\overline{RE}$</th><th>$\overline{WP}$</th><th>MODE</th></tr><tr><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>X</td><td>During Read (Busy)</td></tr><tr><td>↓</td><td>↓</td><td>↓</td><td></td><td></td><td></td><td></td></tr><tr><td>X</td><td>X</td><td>X</td><td>H</td><td>H</td><td>X</td><td>During Read (Busy)</td></tr></table></td><td>Jul. 4. 2008</td><td>Preliminary</td></tr>
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FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES
- Cost effective solutions for mass storage applications

NAND INTERFACE
- x8 bus width.
- Address / Data Multiplexing
- Pinout compatiblity for all densities

SUPPLY VOLTAGE
- 3.3 V device : Vcc = 2.7 V ~3.6 V

MEMORY CELL ARRAY
- (2 K + 64) bytes x 64 pages x 1024 blocks

PAGE SIZE
- (2 K + 64 spare) Bytes

BLOCK SIZE
- (128 K + 4 K spare) Bytes

PAGE READ / PROGRAM
- Random access : 25 us (max.)
- Sequential access : 25 ns (min.)
- Page program time : 200 us (typ.)

FAST BLOCK ERASE
- Block erase time: 2 ms (Typ)

ELECTRONIC SIGNATURE
- 1st cycle : Manufacturer Code
- 2nd cycle : Device Code
- 3rd cycle : Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
- 4th cycle : Page size, Block size, Organization, Spare size

COPY BACK PROGRAM
- Fast Data Copy without external buffering

CACHE READ
- Internal buffer to improve the read throughput

CHIP ENABLE DON'T CARE
- Simple interface with microcontroller

STATUS REGISTER
- Normal Status Register (Read/Program/Erase)

HARDWARE DATA PROTECTION
- Program/Erase locked during Power transitions.

DATA RETENTION
- 100,000 Program/Erase cycles (with 1 bit / 528 byte ECC)
- 10 years Data Retention

PACKAGE
- H27U1G8F2BTR-BX
  : 48-Pin TSOP1 (12 x 20 x 1.2 mm)
    - H27U1G8F2BTR-BX (Lead & Halogen Free)
- H27U1G8F2BFR-BX
  : 63-Ball FBGA (9 x 11 x 1.0 mm)
    - H27U1G8F2BFR-BX (Lead & Halogen Free)

1. SUMMARY DESCRIPTION

Hynix NAND H27U1G8F2B Series have 128 M x 8 bit with spare 4 M x 8 bit capacity. The device is offered in 3.3 V Vcc Power Supply, and with x8 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 1024 blocks, composed by 64 pages. A program operation allows to write the 2112 byte page in typical 200 us and an erase operation can be performed in typical 2.0 ms on a 128 K byte block.

Data in the page can be read out at 25ns cycle time per byte. The I/O pins serve as the ports for address and data input/ output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.

Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, ALE and CLE input pin. The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the $\overline{WP}$ input.

The chip supports $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.

The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.

Even the write-intensive systems can take advantage of the H27U1G8F2B Series extended reliability of 100 K program/ erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Data read out after copy back read is allowed.

This device includes also extra features like OTP/Unique ID area, Read ID2 extension.

The H27U1G8F2B is available in 48-TSOP1 12 x 20 mm and 63-FBGA 9 x 11 mm.

1.1 Product List

PART NUMBER	ORGANIZATION	Vcc RANGE	PACKAGE
H27U1G8F2B	x8	2.7V ~ 3.6V	48-TSOP1 / 63-FBGA

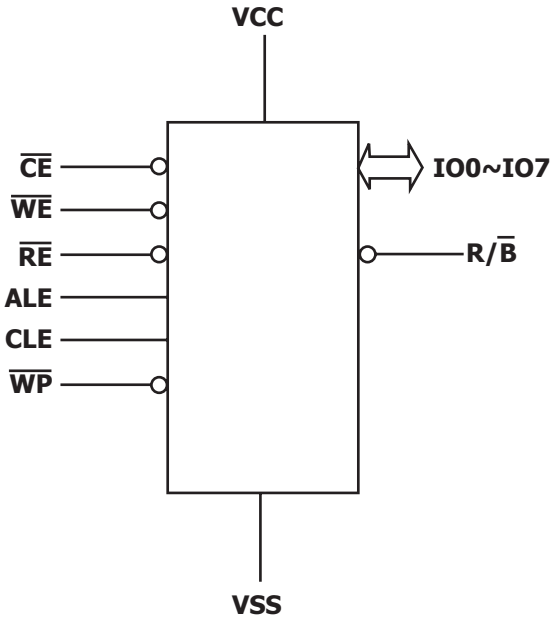


Figure 1 : Logic Diagram

IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1 : Signal Names

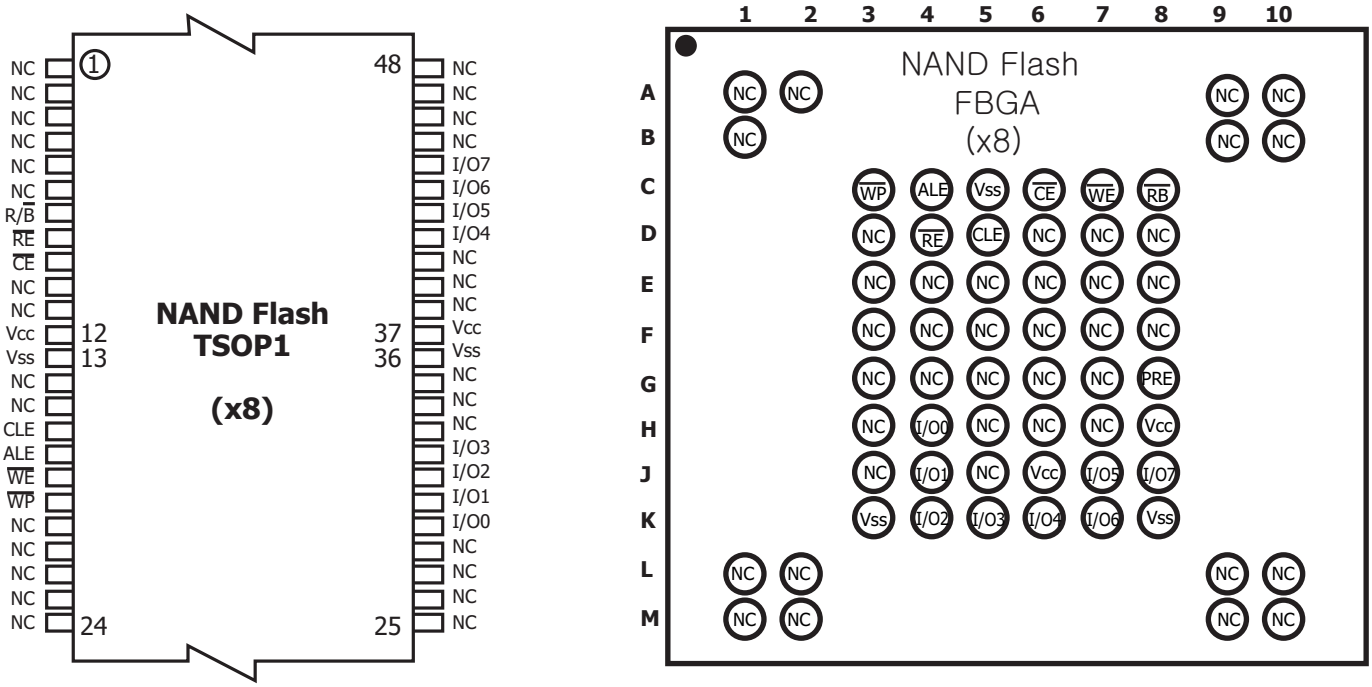


Figure 2 : 48-TSOP1 / 63-FBGA Contact, x8 Device

1.2 PIN DESCRIPTION

Pin Name	Description
IO0 ~ IO7	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$	**CHIP ENABLE** This input controls the selection of the device.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
Vcc	**SUPPLY VOLTAGE** The Vcc supplies the power for all the operations (Read, Write, Erase).
Vss	GROUND
NC	NO CONNECTION

Table 2 : Pin Description

NOTE :

1. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

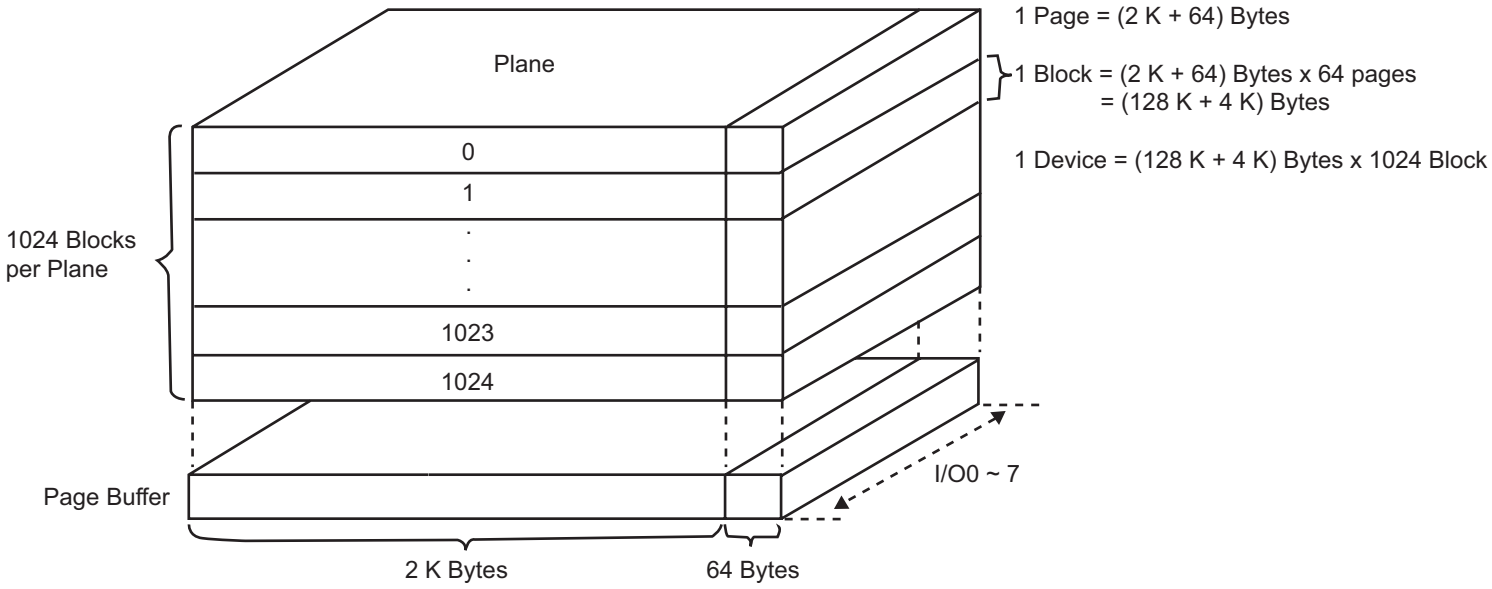


Figure 3 : Array Organization

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27

Table 3 : Address Cycle Map

NOTE:

1. L must be set to Low.
2. 1st & 2nd cycle are Column Address.
3. 3rd to 4th cycle are Row Address.

FUNCTION	1st	2nd	3rd	4th	Acceptable Command During Busy
PAGE READ	00h	30h	-	-	
READ FOR COPY-BACK	00h	35h	-	-	
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	Yes
PAGE PROGRAM	80h	10h	-	-	
COPY BACK PGM	85h	10h	-	-	
BLOCK ERASE	60h	D0h	-	-	
READ STATUS REGISTER	70h	-	-	-	Yes
RANDOM DATA INPUT	85h	-	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	-	
CACHE READ START	31h		-	-	
CACHE READ EXIT	3Fh	-	-	-	

Table 4 : Command Set

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input (4 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input (4 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L	H	Falling	X	Data Output	
X	X	X	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0 V / Vcc	Stand By	

NOTE : With the $\overline{CE}$ don't care option $\overline{CE}$ high during latency time does not stop the read operation

Table 5 : Mode Selection

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 5 and Table 12 for details of the timings requirements.

2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. To insert the 28 addresses needed to access the 1Gbit 4 clock cycles are needed. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 6 and Table 12 for details of the timings requirements.

2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 7 and Table 12 for details of the timings requirements.

2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 8, 9, 10 and Table 12 for details of the timings requirements.

2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby.

In Standby the device is deselected, outputs are disabled and Power Consumption reduced.

3. DEVICE OPERATION

3.1 Page Read.

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h and 30h to the command register along with four address cycles. In two consecutive read operations, the second one does need 00h command, which four address cycles and 30h command initiates that operation. Second read operation always requires setup command if first read operation was executed using also random data out command.

Two types of operations are available: random read , serial page read. The random read mode is enabled when the page address is changed. The 2112 bytes of data within the selected page are transferred to the data registers in less than 25 us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 25 ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command.

The column address of next data, which is going to be out, may be changed to the address which follows random data output command.

Random data output can be operated multiple times regardless of how many times it is done in a page.

After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.

Any operation other than read or random data output causes device to exit read mode.

Check Figure 11, Figure 12, and Figure 13 as references.

3.2 Page Program.

The device is programmed basically by page, but it does allow multiple partial page programming of a word or consecutive bytes up to 2112, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 8; for example, 4 times for main array (1time/512byte) and 4 times for spare array (1time/16byte).

A page program cycle consists of a serial data loading period in which up to 2112 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the four cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 14 and Figure 15 detail the sequence.

3.3 Block Erase.

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A18 to A27 is valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify.

Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

Figure 18 details the sequence.

3.4 Copy-Back Program.

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling $\overline{RE}$, or Copy Back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 17.

"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, two bit error correction is recommended for the use of Copy-Back operation."

Figure 16 and Figure 17 show the command sequence for the copy-back operation.

Please note that $\overline{WP}$ value is don't care during Read for copy back, while it must be set to Vcc when performing the program .

3.5 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to Table 13 for specific Status Register definitions, and Figure 10 for specific timings requirements. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

3.6 Read ID.

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code (ADh), and the device code and 00h, 4th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 19 shows the operation sequence, while Table 14 to Table 17 explain the byte meaning.

3.7 Reset.

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when $\overline{WP}$ is high. Refer to Table 13 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written (see Figure 20).

3.8 Read Cache

The Read Cache function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, as defined in 3.1, shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence.

The Read Cache function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Read Cache function. Issuing an additional Read Cache function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array.

The host shall not issue a sequential Read Cache (31h) command after the last page of the device is read.

Figure 21 defines the Read Cache behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register. Figure 21 also shows the Read Cache behavior and timings for the end of cache operation.

4. OTHER FEATURES

4.1 Data Protection.

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.8 V (3.3 V version). WP pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 22. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back, cache program and random read completion. The R/B pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B) and current drain during busy (I busy), an appropriate value can be obtained with the following reference chart (Figure 23). Its value can be determined by the following guidance.

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	1004		1024	Blocks

Table 6 : Number of Valid Blocks

NOTE:
1. The 1st block is guaranteed to be a valid block at the time of shipment.

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (Temperature Range Option 1)	0 to 70	°C
	Ambient Operating Temperature (Temperature Range Option 6)	– 40 to 85	°C
T_{BIAS}	Temperature Under Bias	– 50 to 125	°C
T_{STG}	Storage Temperature	– 65 to 150	°C
V_{IO} (2)	Input or Output Voltage	– 0.6 to 4.6	V
V_{CC}	Supply Voltage	– 0.6 to 4.6	V

Table 7 : Absulute maximum ratings

NOTE:
1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the HYNIX SURE Program and other relevant quality documents.

2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

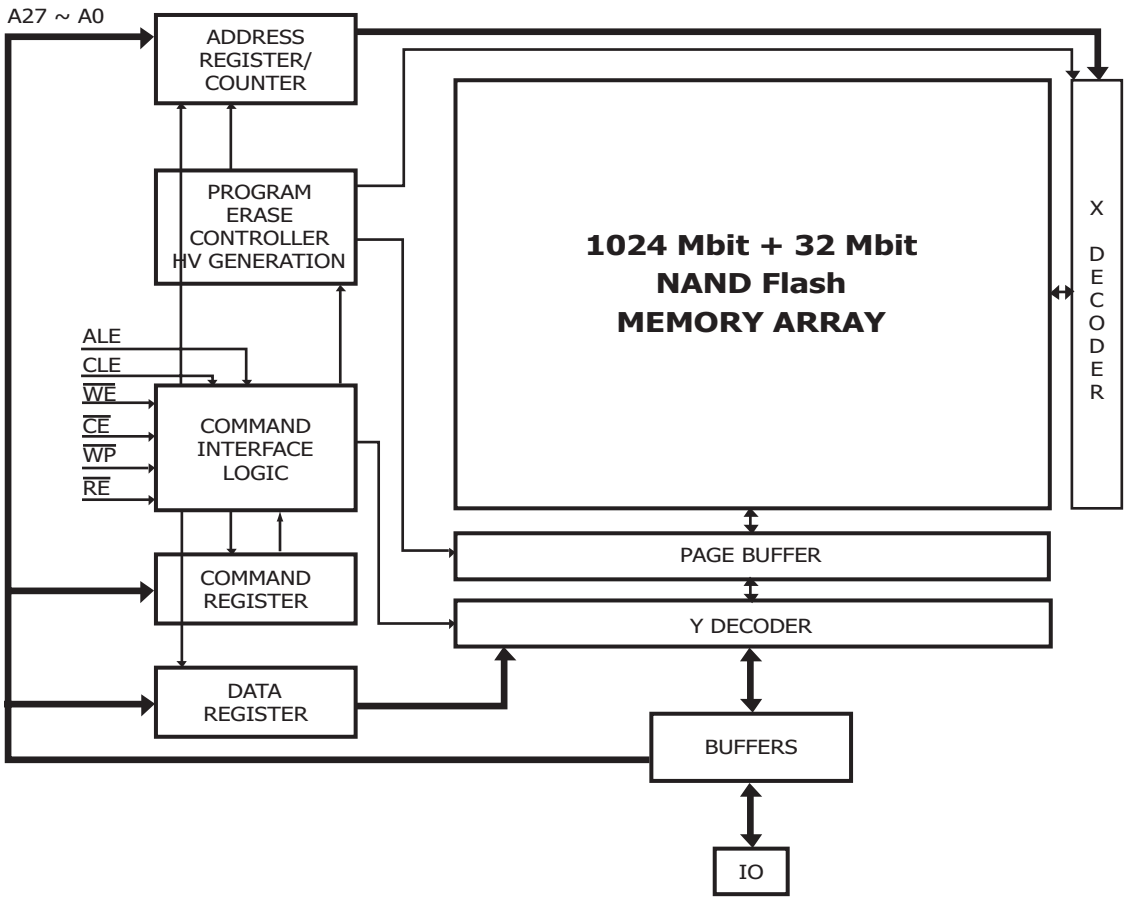


Figure 4 : Block Diagram

Parameter		Symbol	Test Conditions	3.3 Volt			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC} = 25 ns, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = 0 V/V_{CC}			1	mA
Stand-By Current (CMOS)		I_{CC5}	$\overline{CE}$ = V_{CC}-0.2, $\overline{WP}$ = 0/V_{CC}		10	50	uA
Input Leakage Current		I_{LI}	V_{IN} = 0 to Vc (max)		-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT} = 0 to Vcc(max)		-	±10	uA
Input High Voltage		V_{IH}	-	0.8 x V_{CC}	-	V_{CC} + 0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH} = - 400 uA	2.4	-	-	V
Outpul Low Voltage Level		V_{OL}	I_{OL} = 2.1 mA	-	-	0.4	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	V_{OL}= 0.4 V	8	10	-	mA
Vcc supply voltage (erase and program) lockout		V_{LKO}	-		1.8	-	V

Table 8 : DC and Opeating Characteristics

Parameter	Value
	3.3 Volt
Input Pulse Levels	0 V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} / 2
Output Load (1.65V – 1.95V & 2.5V - 3.6V)	1 TTL GATE and CL = 50 pF

Table 9 : AC Test Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF

Table 10 : Pin Capacitance (TA = 25 ℃, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	200	700	us
Dummy Busy Time for Cache Program	t_{CBSY}	-	3	700	us
Dummy Busy Time for the Lock or Lock-tight Block	t_{LBSY}	-	5	10	us
Number of partial Program Cycles in the same page	Nop	-	-	8	Cycle
Block Erase Time	t_{BERS}	-	2	3	ms

Table 11 : Program / Erase Characteristics

NOTE :
Typical program time is defined as the time when which more than 50 % of the whole pages are programmed at Vcc = 3.3 V and 25 ℃.

Parameter	Symbol	3.3 Volt		Unit
		Min	Max	
CLE Setup time	t_{CLS}	12		ns
CLE Hold time	t_{CLH}	5		ns
$\overline{CE}$ Setup time	t_{CS}	20		ns
$\overline{CE}$ Hold time	t_{CH}	5		ns
$\overline{WE}$ Pulse width	t_{WP}	12		ns
ALE Setup time	t_{ALS}	12		ns
ALE Hold time	t_{ALH}	5		ns
Data Setup time	t_{DS}	12		ns
Data Hold time	t_{DH}	5		ns
Write Cycle time	t_{WC}	25		ns
$\overline{WE}$ High Hold time	t_{WH}	10		ns
Address to Data Loading time	t_{ADL}	70		ns
Data Transfer from Cell to Register	t_{R}		25	us
ALE to $\overline{RE}$ Delay	t_{AR}	10		ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10		ns
Ready to RE Low	t_{RR}	20		ns
$\overline{RE}$ Pulse Width	t_{RP}	12		ns
$\overline{WE}$ High to Busy	t_{WB}		100	ns
Read Cycle Time	t_{RC}	25		ns
$\overline{RE}$ Access Time	t_{REA}		20	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}		100	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}		30	ns
$\overline{CE}$ High to ALE or CLE Don't care	t_{CSD}	10		ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15		ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5		ns
$\overline{CE}$ High to Output Hold	t_{COH}	15		ns
$\overline{RE}$ High Hold Time	t_{REH}	10		ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0		ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100		ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60		ns
Device Resetting Time (Read/Program/Erase)	t_{RST}		5/10/500 [1)]	us

Table 12 : AC Timing Characteristics

NOTE :

1) If Reset Command (FFh) is written at Ready State, the device goes into Busy for maximum 5 us

IO	Page Program	Block Erase	Read	Cache Read	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass: '0' Fail: '1'
1	NA	NA	NA	NA	-
2	NA	NA	NA	NA	-
3	NA	NA	NA	NA	-
4	NA	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	P/E/R Controller Bit	Active: '0' Idle:'1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy: '0' Ready:'1'
7	Write Protect	Write Protect	Write Protect	NA	Protected: '0' Not Protected: '1'

Table 13 : Status Register Coding

DEVICE IDENTIFIER BYTE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal Chip Number, Cell Type, etc.
4th	Page Size, Block Size, Spare Size, Organization

Table 14 : Device Identifier Coding

Part Number	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)	3rd cycle	4th cycle
H27U1G8F2B	3.3V	x8	ADh	F1h	00h	1Dh

Table 15 : Read ID Data Table

	Description	IO7	IO6	IO5 IO4	IO3 IO2	IO1 IO0
Die / Package	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave Program Between multiple chips	Not Supported		0 1			
Write Cache	Not Supported	0 1				

Table 16 : 3rd Byte of Device Identifier Description

	Description	IO7	IO6	IO5-4	IO3	IO2	IO1-0
Page Size (Without Spare Area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Spare Area Size (Byte / 512Byte)	8 16					0 1	
Serial Access Time	45 ns 25 ns Reserved Reserved	0 0 1 1			0 1 0 1		
Block Size (Without Spare Area)	64K 128K 256K 512KB			0 0 0 1 1 0 1 1			
Organization	X8 X16		0 1				

Table 17 : 4th Byte of Device Identifier Description

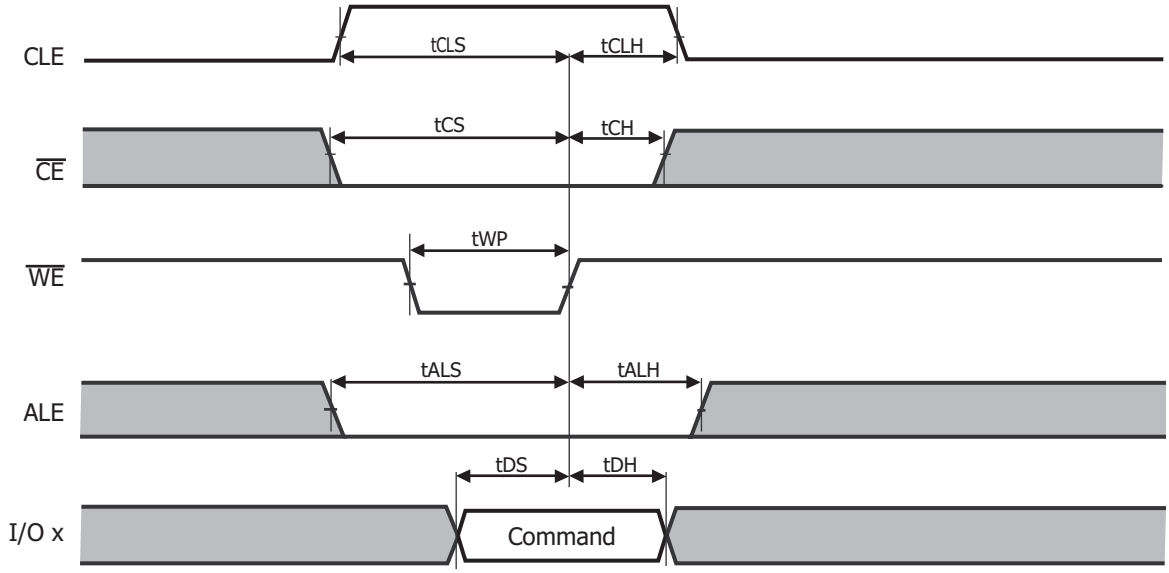


Figure 5 : Command Latch Cycle

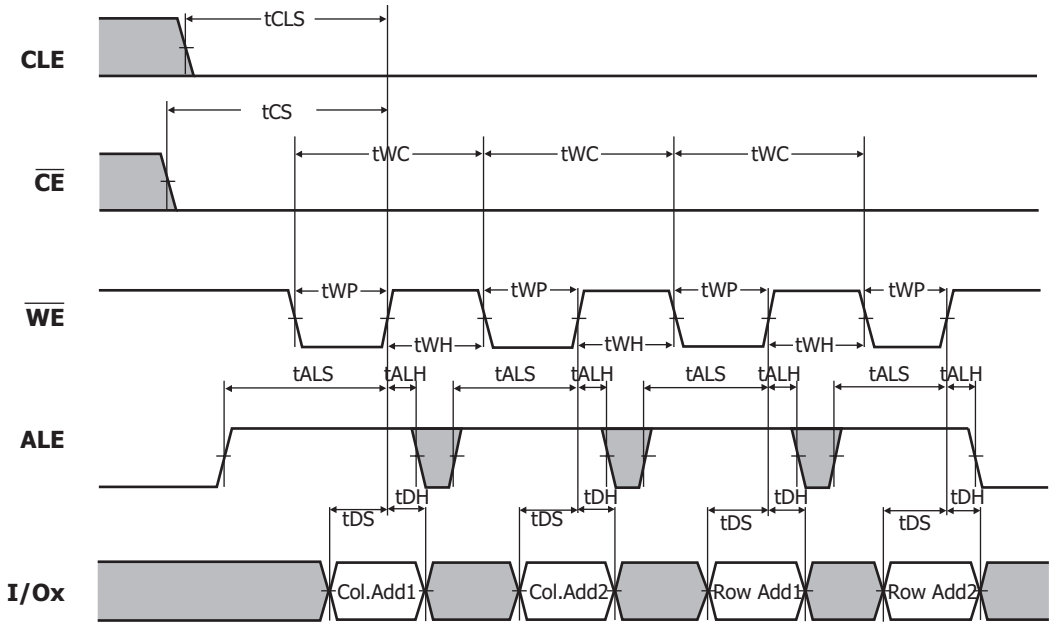


Figure 6 : Address Latch Cycle

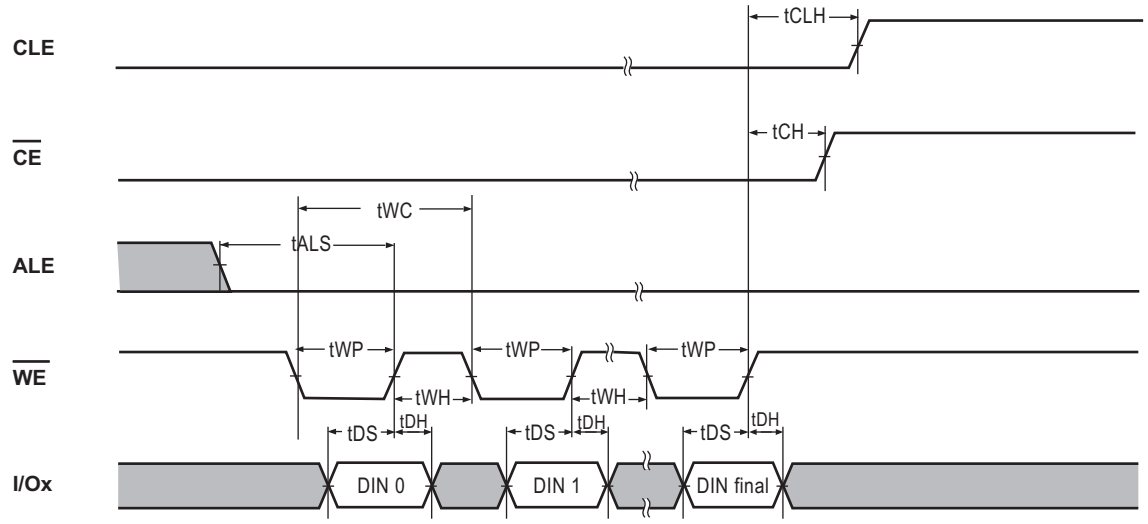
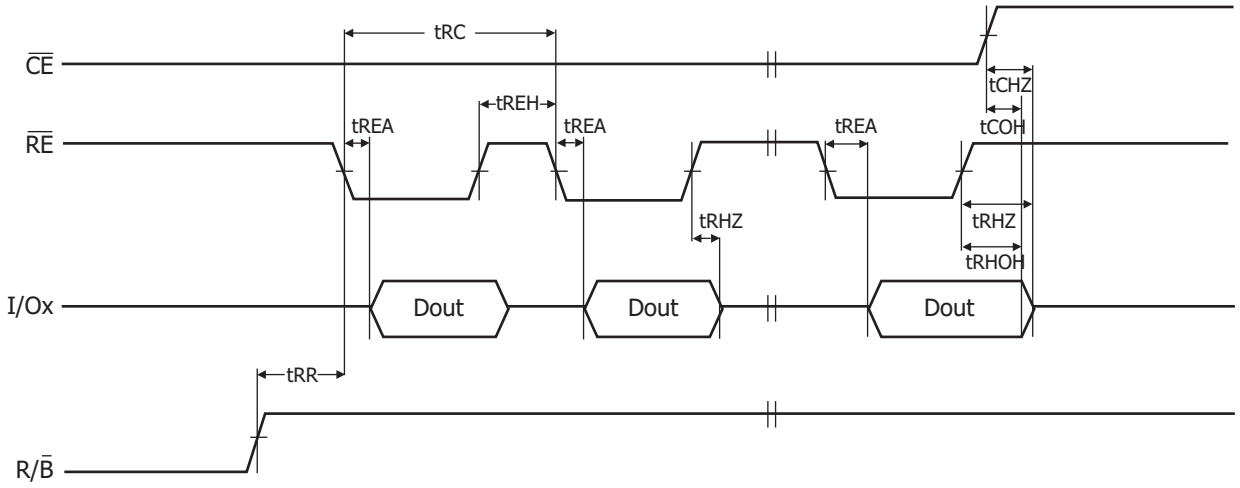
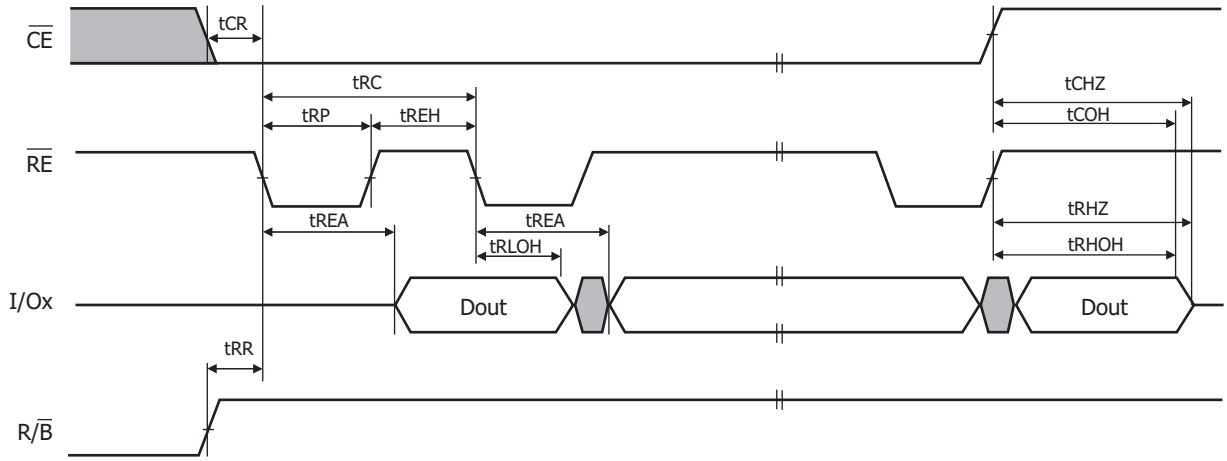


Figure 7 : Input Data Latch Cycle



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRHOH starts to be valid when frequency is lower than 33 MHz.
tRLOH is valid when frequency is higher than 33 MHz.

Figure 8 : Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 9 : Sequential Out Cycle after Read

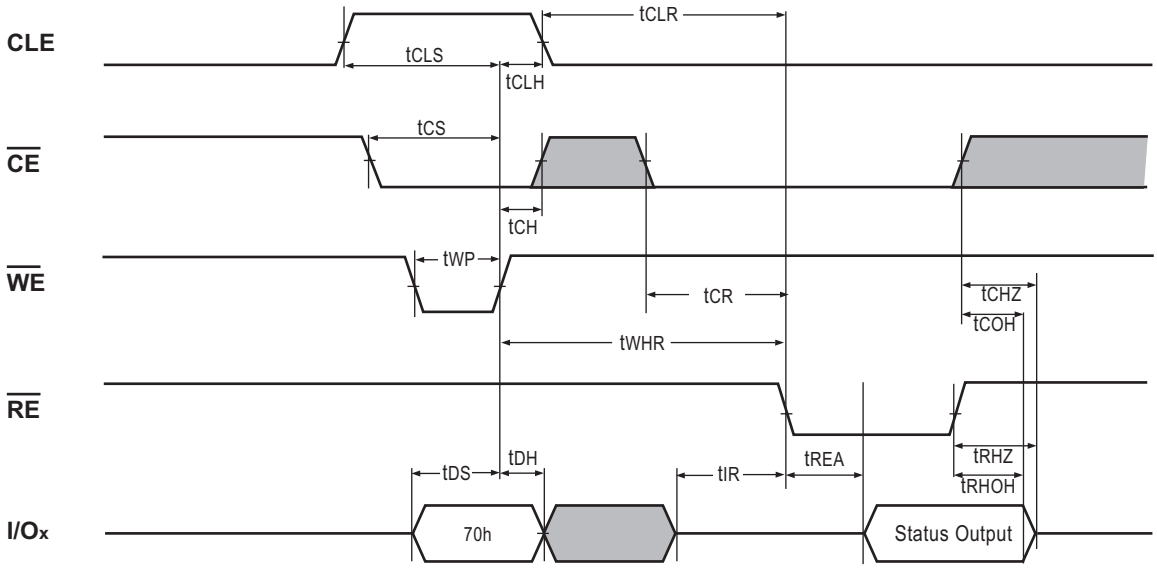


Figure 10 : Status Read Cycle

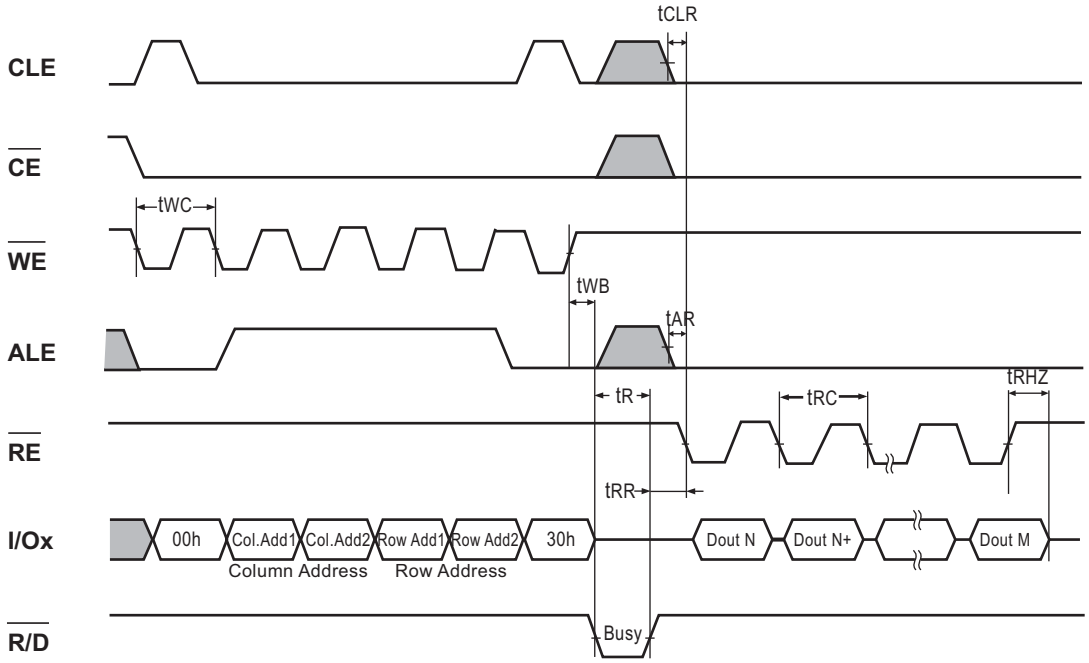


Figure 11 : Read Operation (Read One Page)

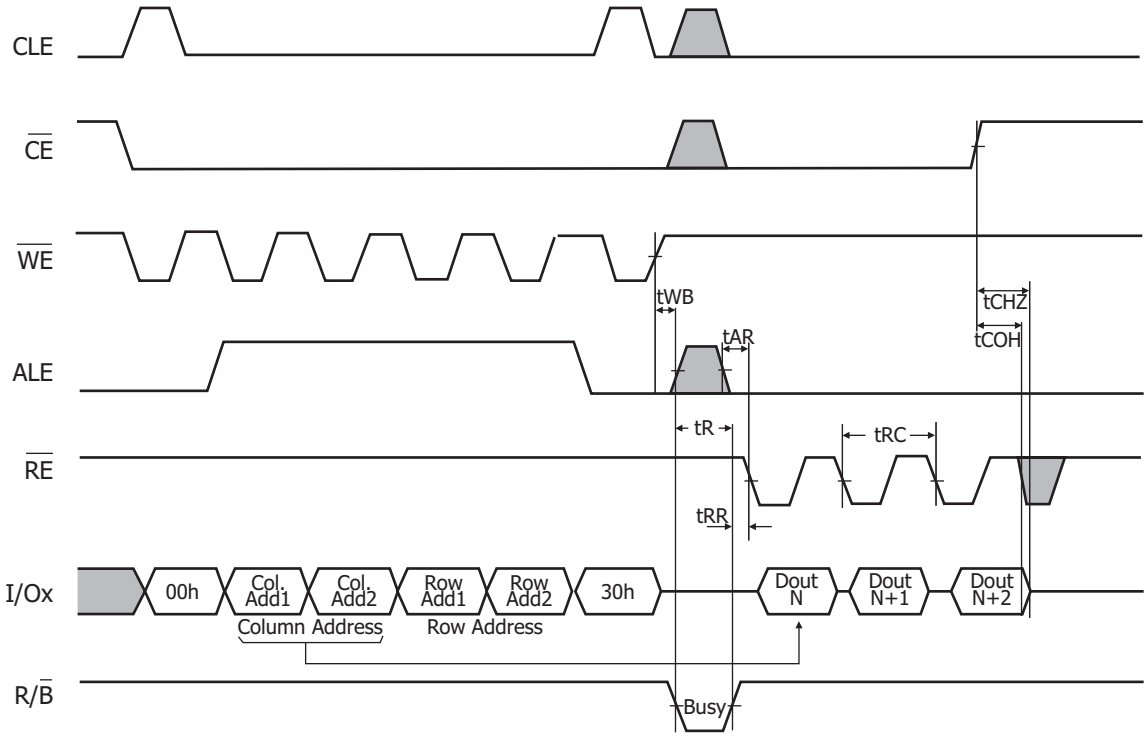


Figure 12 : Read Operation Intercepted by $\overline{CE}$

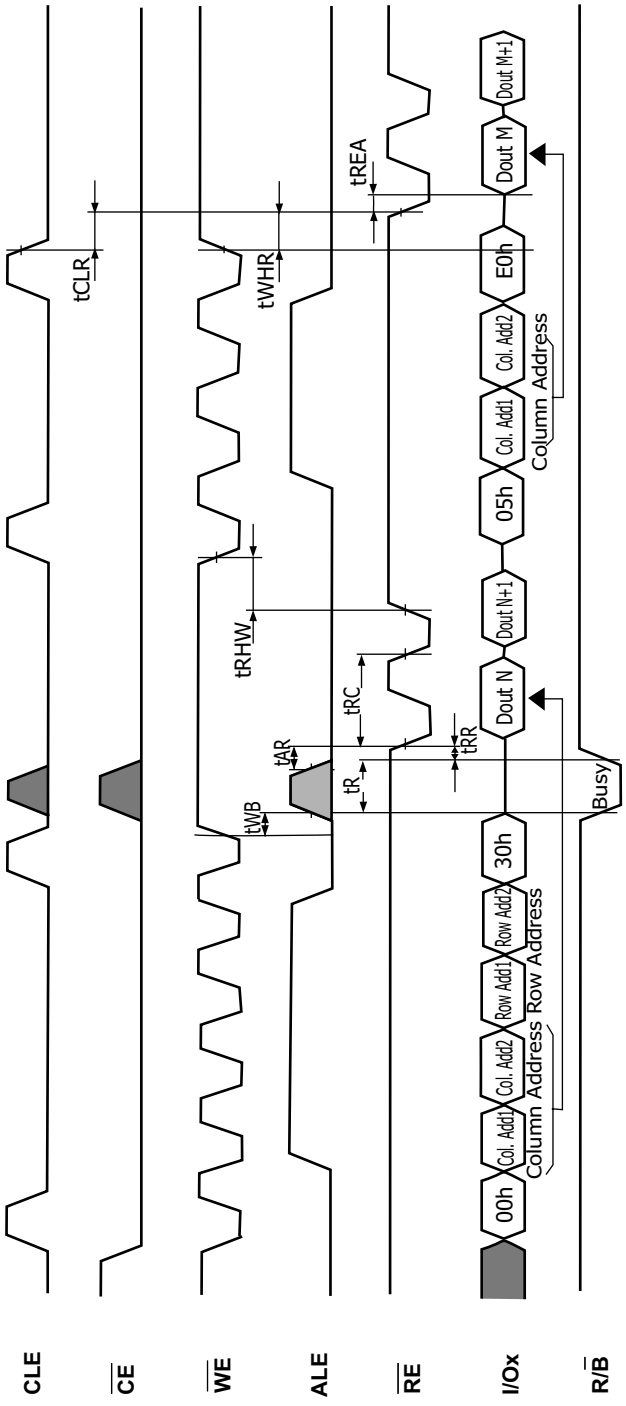
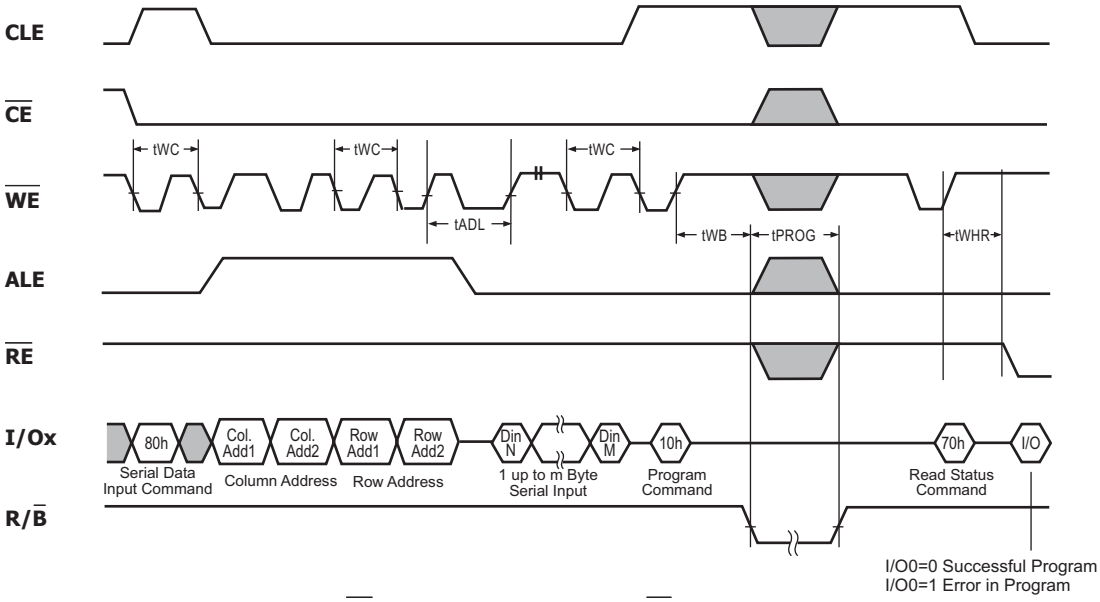


Figure 13 : Random Data Output



NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Figure 14 : Page Program Opeation

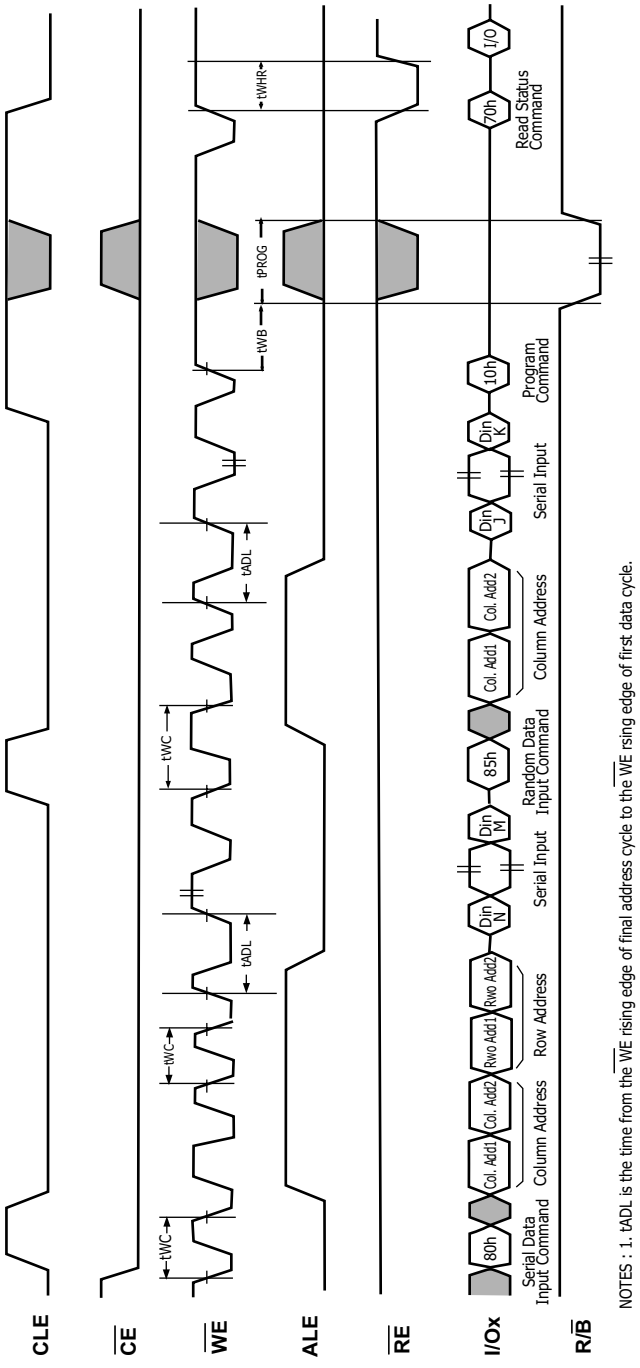


Figure 15 : Random Data In

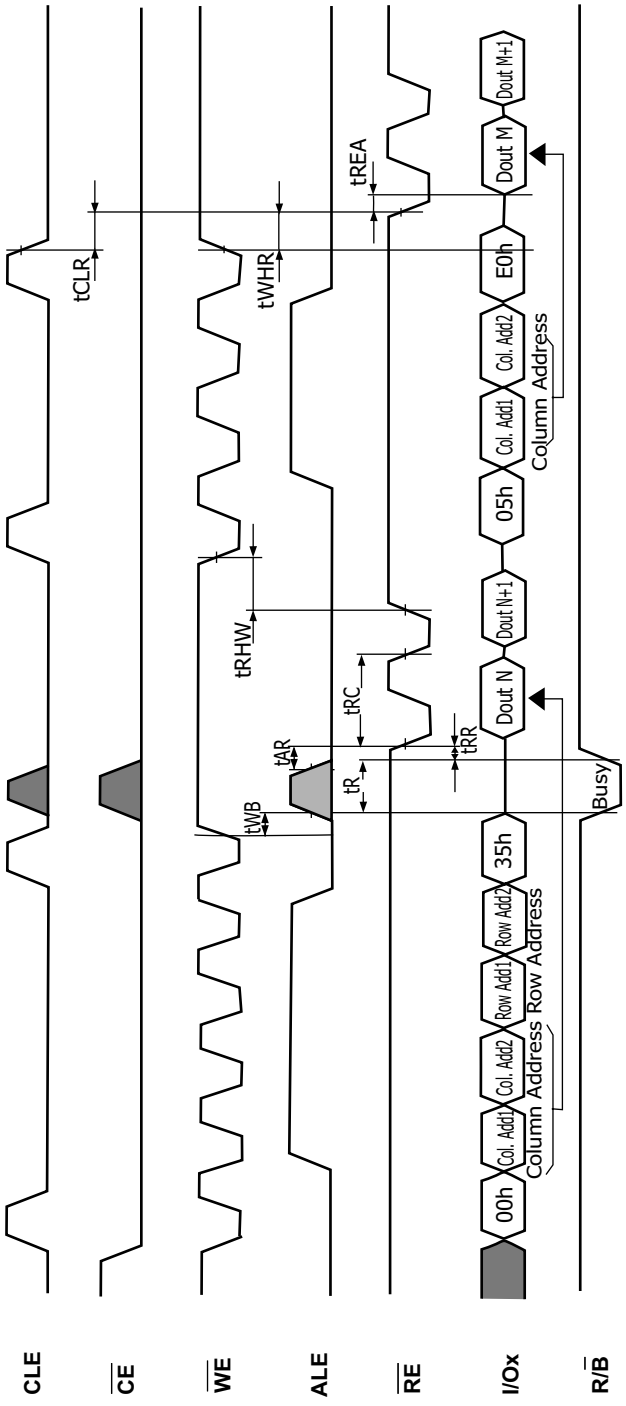


Figure 16 : Copy Back Read with Optional Data Readout

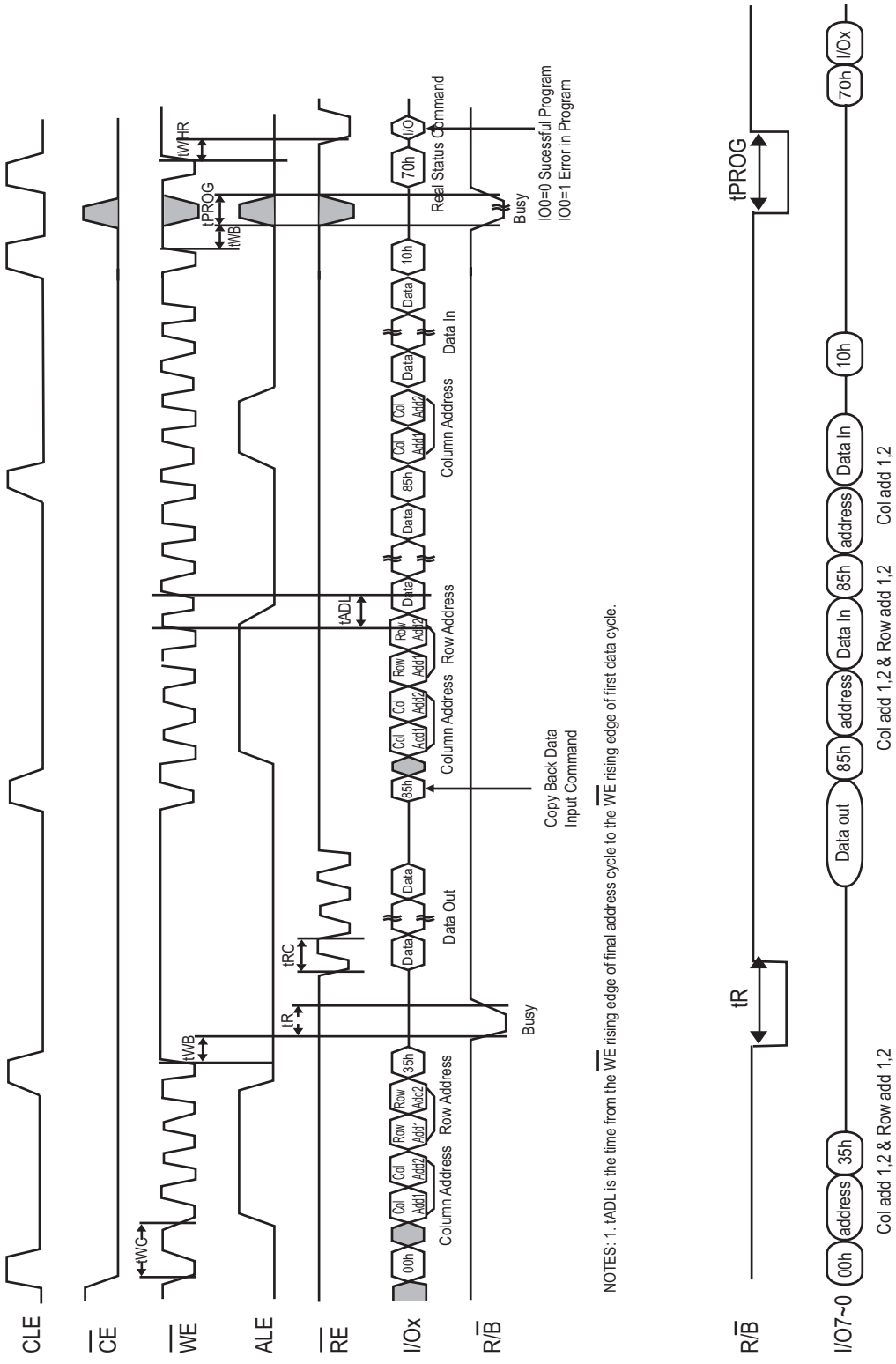


Figure 17 : Copy Back Program with Random Data Input

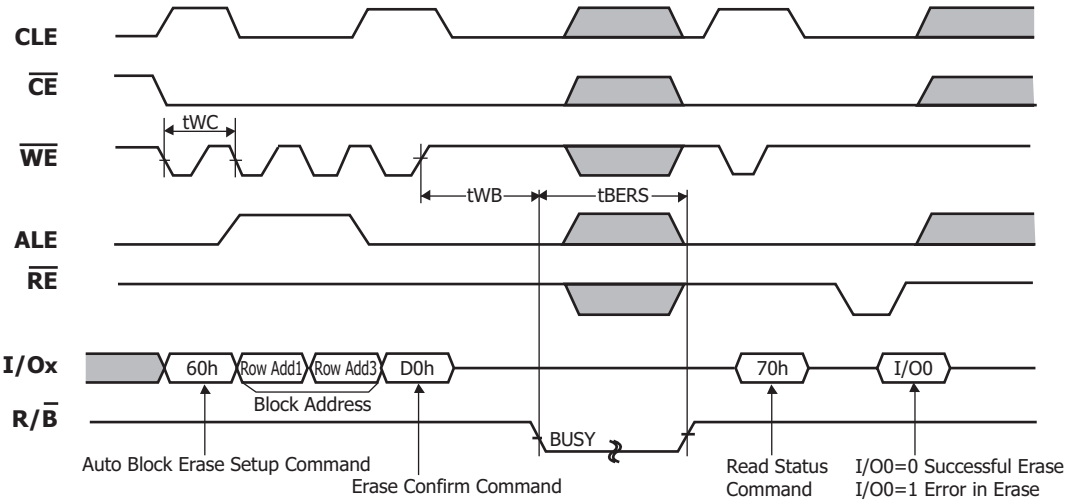


Figure 18 : Block Erase Operation (Erase One Block)

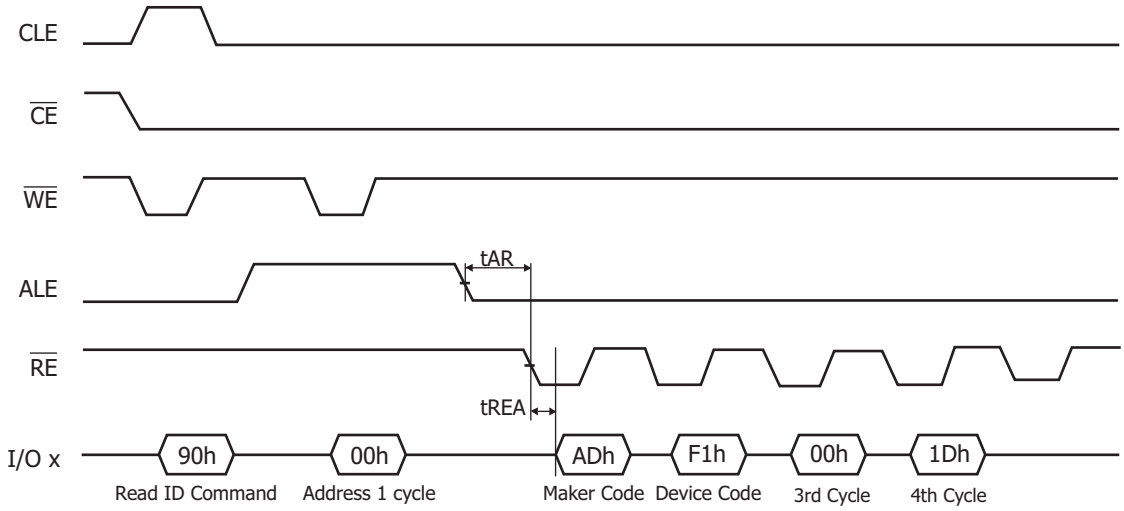


Figure 19 : Read ID Operation

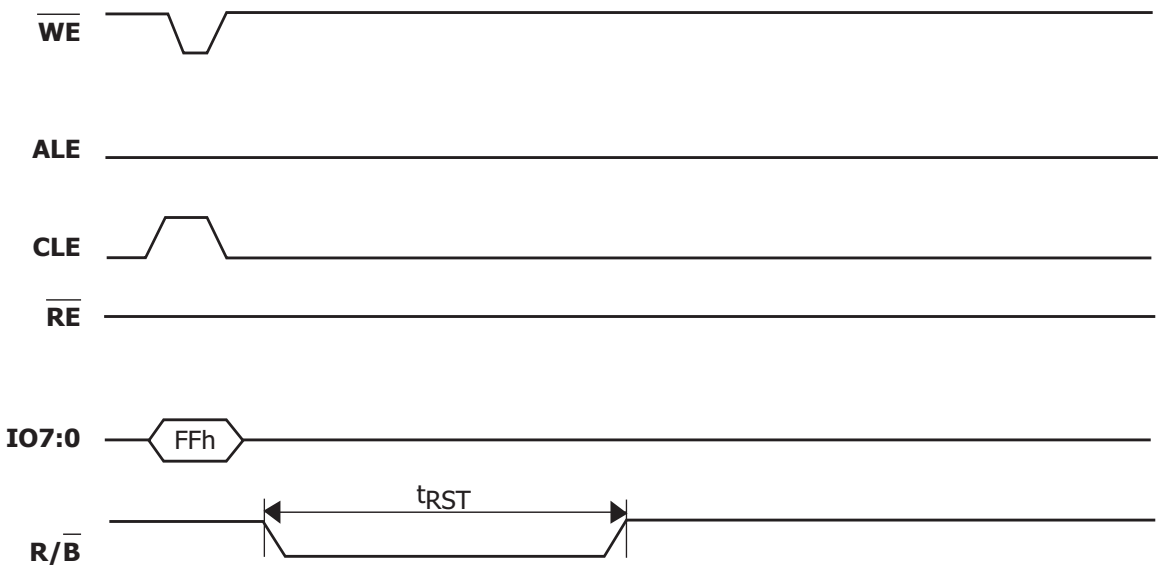


Figure 20 : Reset Operation Timing

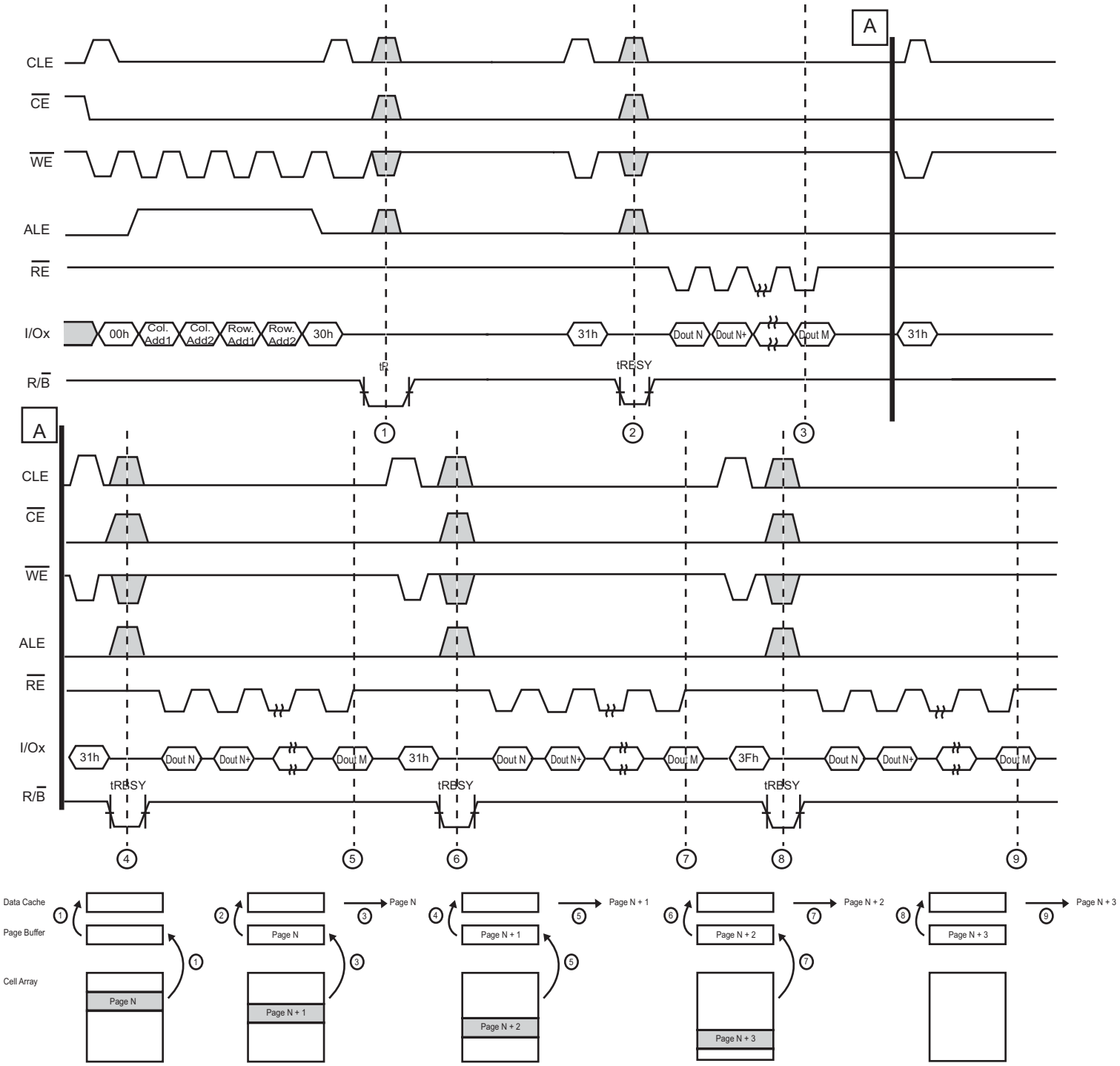


Figure 21 : Read Operation with Read Cache

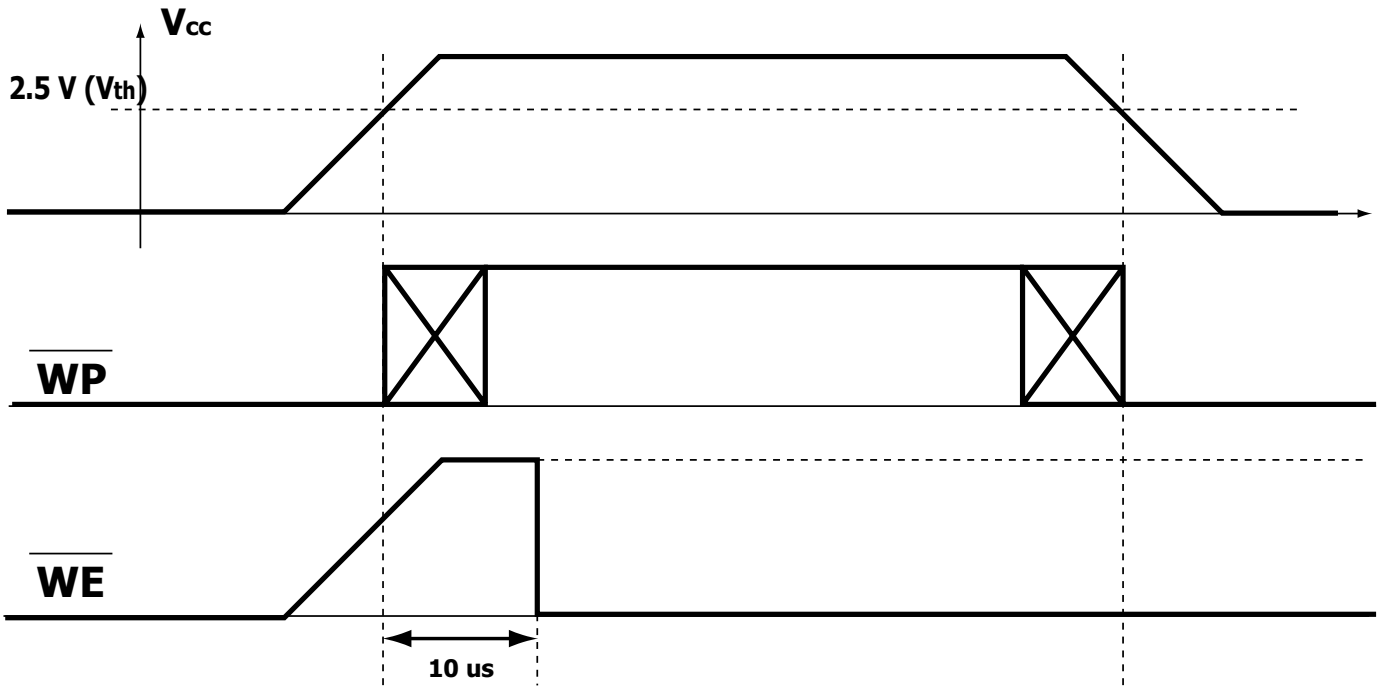


Figure 22 : Power on and Data Protection timings

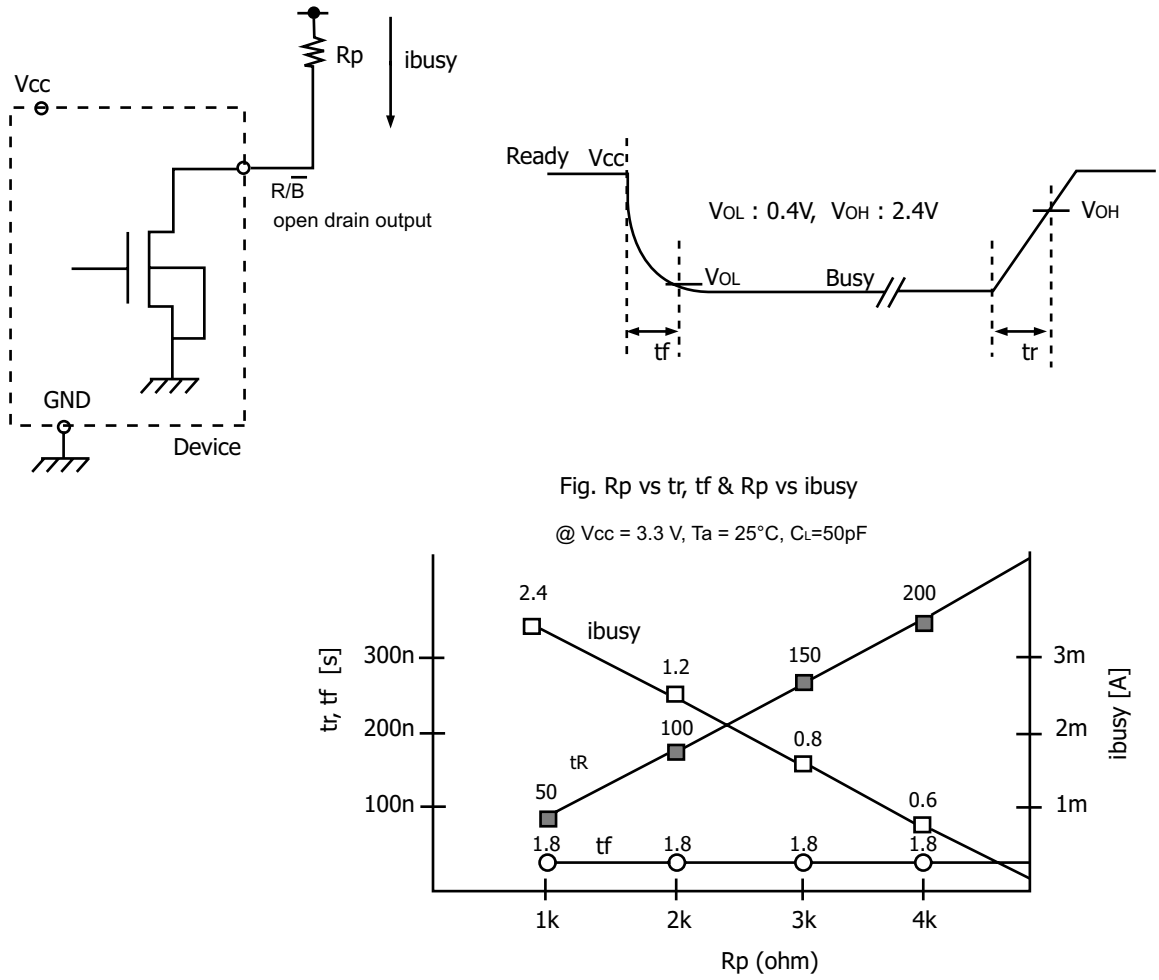


Fig. Rp vs tr, tf & Rp vs ibusy

Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 23 : Ready/Busy Pin Electrical Specifications

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd th page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 24. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

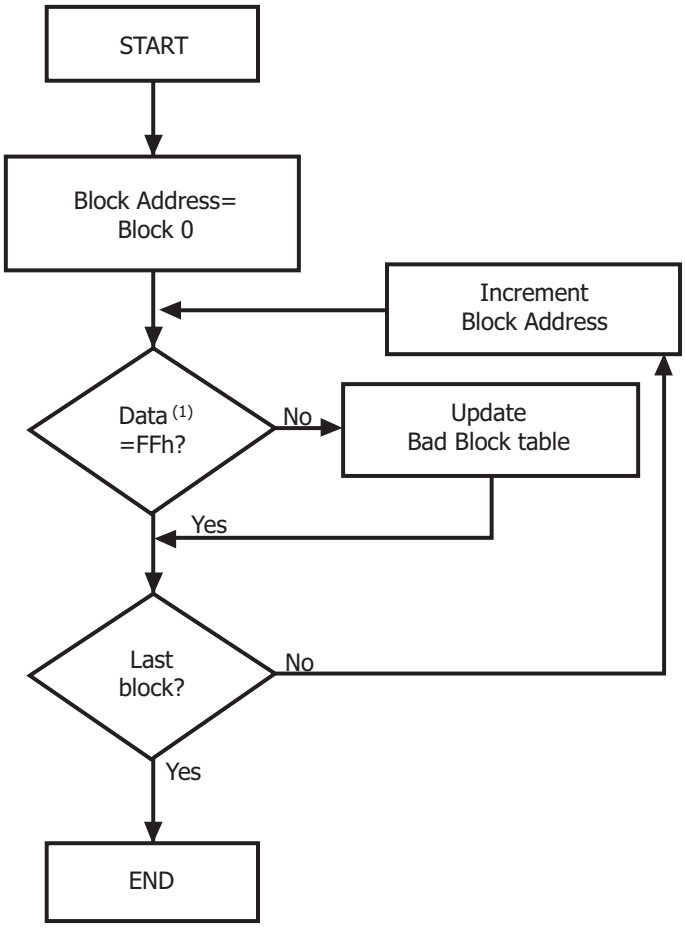


Figure 24 : Bad Block Management Flowchart

NOTE :

- Make sure that either the 1st or 2nd page of every initial block has not FFh data at the column address of 2048.

Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
The failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.
Refer to Table 18 and Figure 25 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (with 1bit/512byte)

Table 18 : Block Failure

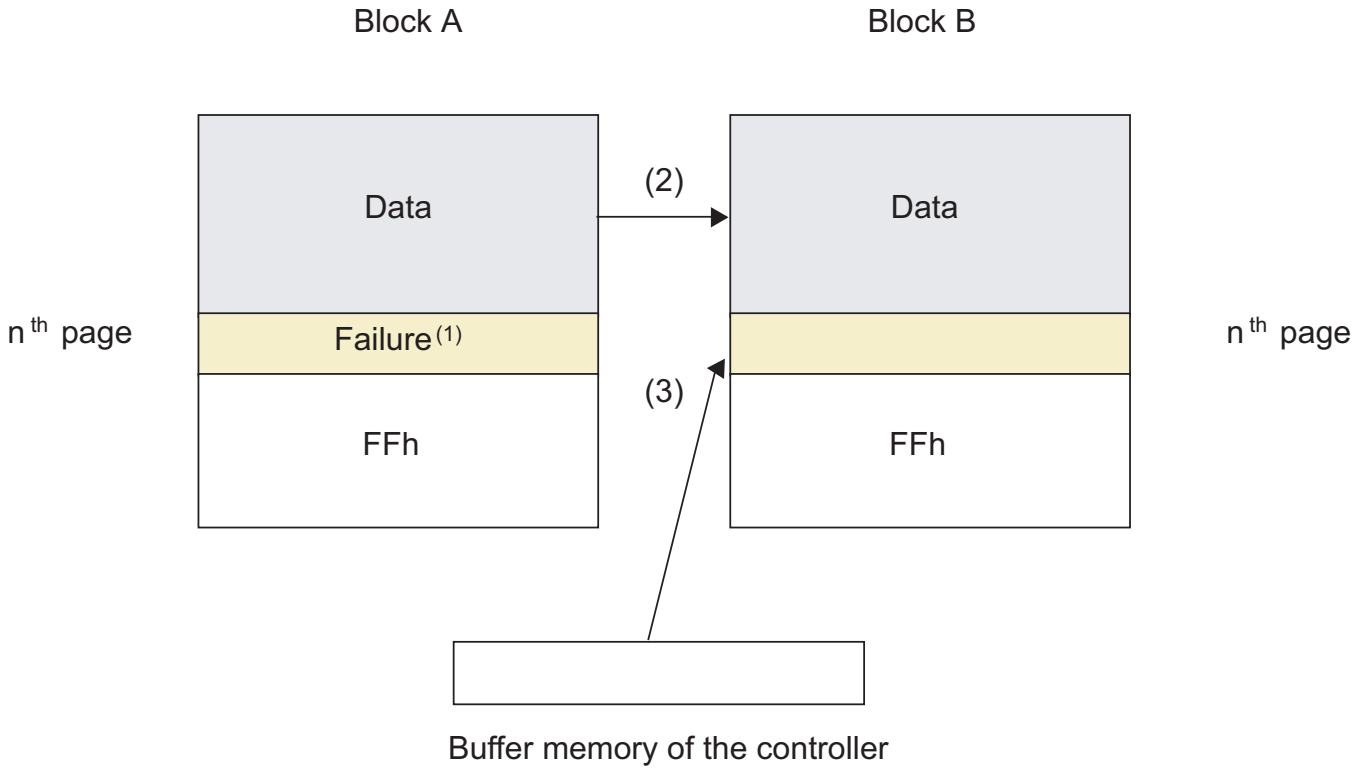


Figure 25 : Bad Block Replacement

NOTE :
1. An error occurs on the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. N^{th} data of block A which is in controller buffer memory is copied into n^{th} page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A

Write Protect Operation

The Erase and Program Operations are automatically reset when WP goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 26~29)

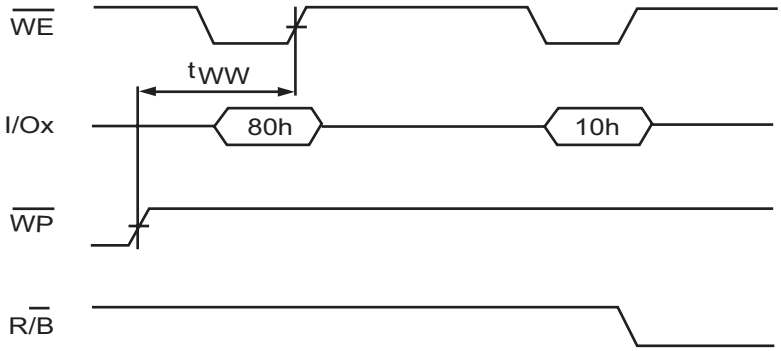


Figure 26 : Enable Programming

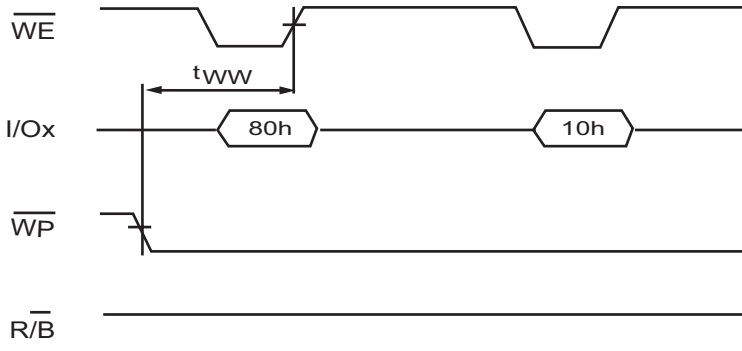


Figure 27 : Disable Programming

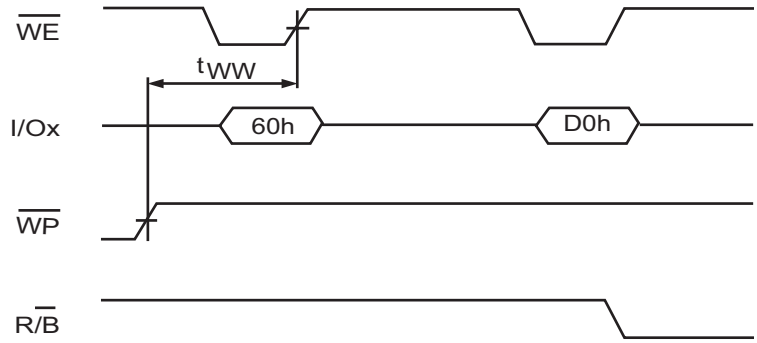


Figure 28 : Enable Erasing

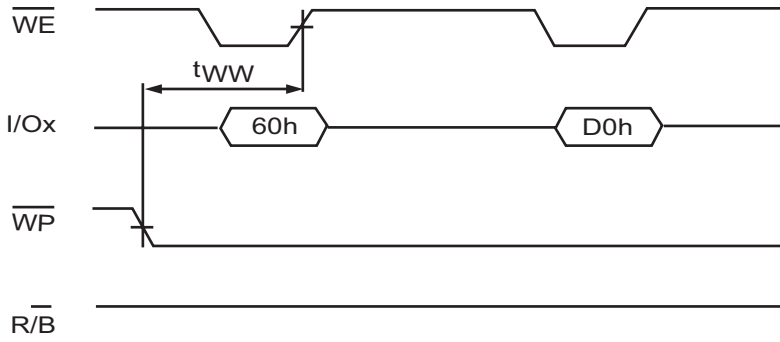


Figure 29 : Disable Erasing

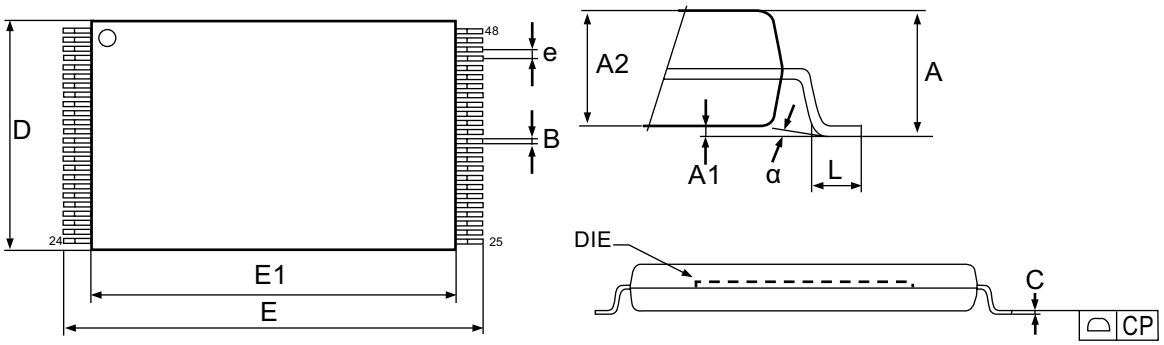


Figure 30. 48-TSOP1 - 12 x 20mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 19. 48-TSOP1 - 12 x 20mm, Package Mechanical Data

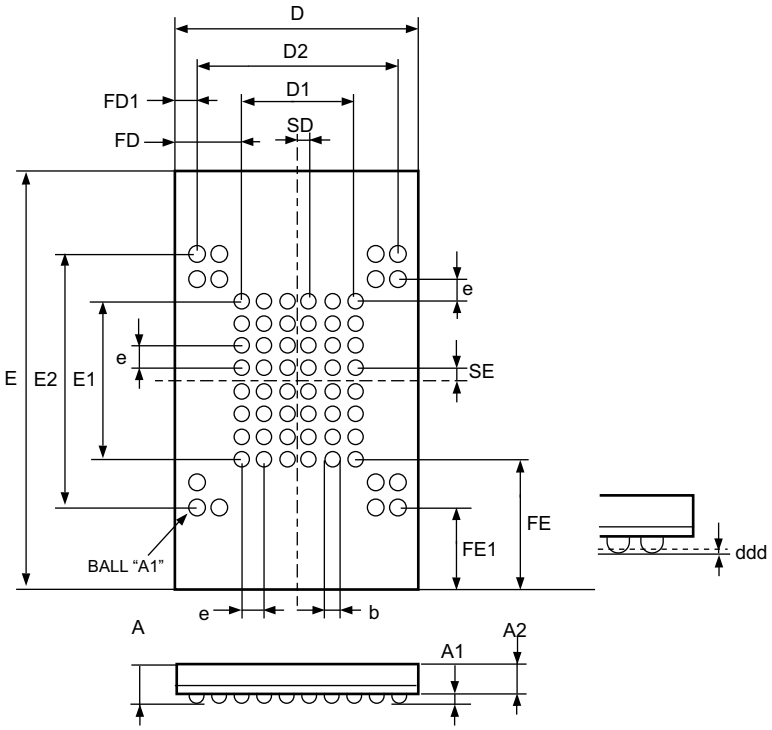


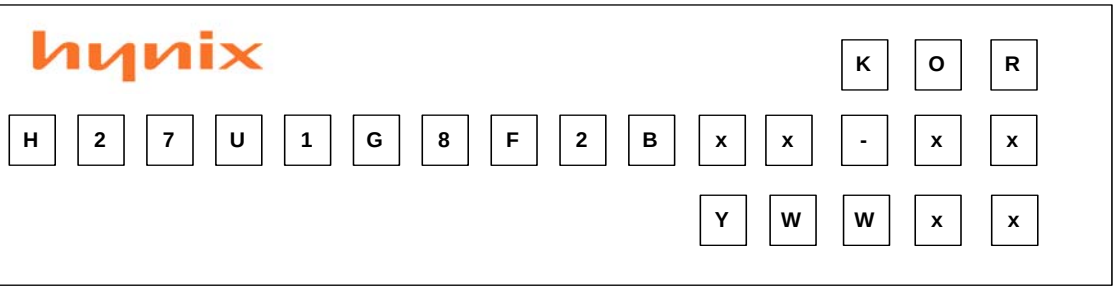
Figure 31. 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A	0.80	0.90	1.00
A1	0.25	0.30	0.35
A2	0.55	0.60	0.65
b	0.40	0.45	0.50
D	8.90	9.00	9.10
D1		4.00	
D2		7.20	
E	10.90	11.00	11.10
E1		5.60	
E2		8.80	
e		0.80	
FD		2.50	
FD1		0.90	
FE		2.70	
FE1		1.10	
SD		0.40	
SE		0.40	

Table 20. 63-ball FBGA - 9 x 11 ball array 0.8mm pitch, Package Mechanical Data

MARKING INFORMATION - TSOP1 / FBGA

Marking Example



- hynix	: Hynix Symbol
- KOR	: Origin Country
- H27U1G8F2Bxx-xx	: Part Number
H: Hynix	
27: NAND Flash	
U: Power Supply	: U (2.7 V~3.6 V)
1G: Density	: 1 Gbit
8 : Bit Organization	: 8(x8)
F: Classification	: Single Level Cell+Single Die+Large Block
2: Mode	: 2(1nCE & 1R/nB; Sequential Row Read Disable)
B: Version	: 3rd Generation
x: Package Type	: T(48-TSOP1), F(63-FBGA)
x: Package Material	: Blank(Normal), R(Lead & Halogen Free)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)
x: Operating Temperature	: C(0℃~70℃), I(-40℃~85℃)
- Y: Year (ex: 8=year 2008, 9= year 2009)	
- ww: Work Week (ex: 12= work week 12)	
- xx: Process Code	
Note	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item