N-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The ME2306A is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

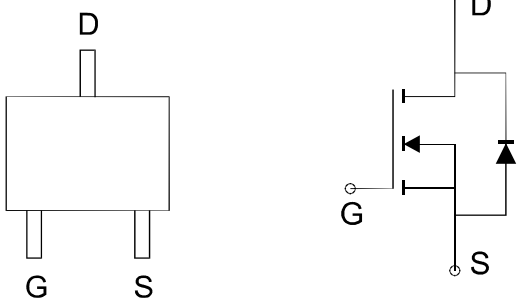
FEATURES

- $R_{DS(ON)} \leqq 30m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 35m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 52m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

PIN CONFIGURATION

(SOT-23)

Top View



Ordering Information: ME2306A (Pb-free)

ME2306A-G (Green product)

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	5 sec	Steady State	Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±12		V
Continuous Drain Current(Tj=150℃)	T_A=25℃	I_D	4	3.16	A
	T_A=70℃		3.5	2.7	
Pulsed Drain Current		I_{DM}	20		
Maximum Body-Diode Continuous Current		I_S	1.04	0.62	A
Maximum Power Dissipation	T_A=25℃	P_D	1.25	0.75	W
	T_A=70℃		0.8	0.48	
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T≦10 sec	70	℃/W
			Steady State	95	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	65		℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC PARAMETERS						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.7		1.4	
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		V_{DS}=30V, V_{GS}=0V T_J=55℃			10	
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D= 4A		24	30	mΩ
		V_{GS}=4.5V, I_D= 3.5A		27	35	
		V_{GS}=2.5V, I_D= 2.8A		37	52	
V_{SD}	Diode Forward Voltage	I_S=1.25A, V_{GS}=0V		0.8	1.2	V
DYNAMIC PARAMETERS						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=4A		15.5	18	nC
Qgs	Gate-Source Charge			3.2		
Qgd	Gate-Drain Charge			3.5		
Rg	Gate Resistance	f =1MHz		0.7		Ω
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		480	550	pF
Coss	Output Capacitance			70		
Crss	Reverse Transfer Capacitance			18		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V, R_G=6Ω		8.5	11	ns
t_r	Rise Time			17	21	
$t_{d(off)}$	Turn-Off Delay Time			31	40	
t_f	Fall Time			3	6	

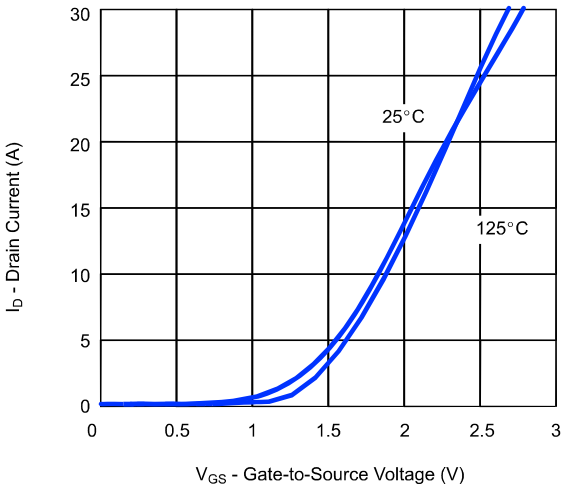
Notes: a. Pulse test; pulse width ≦ 380us, duty cycle≦ 2%

Matsuki reserves the right to improve product design, functions and reliability without notice.

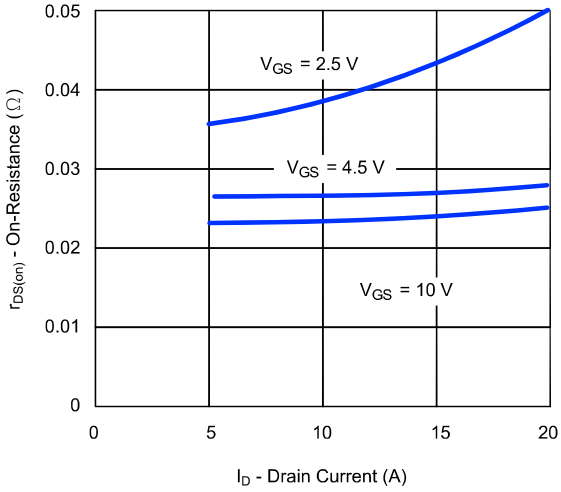
N-Channel Enhancement Mode MOSFET

Typical Characteristics (T_J =25℃ Noted)

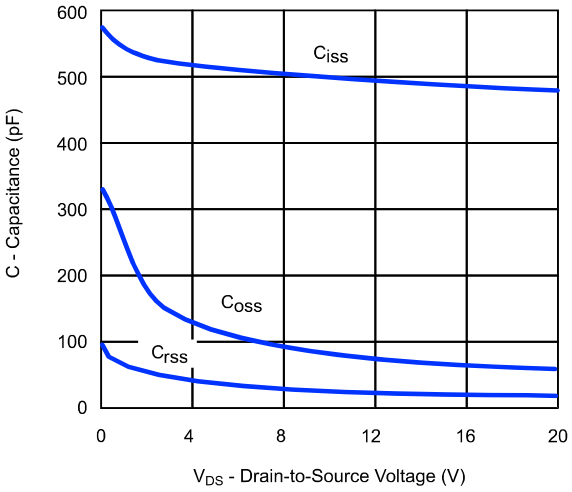
Transfer Characteristics



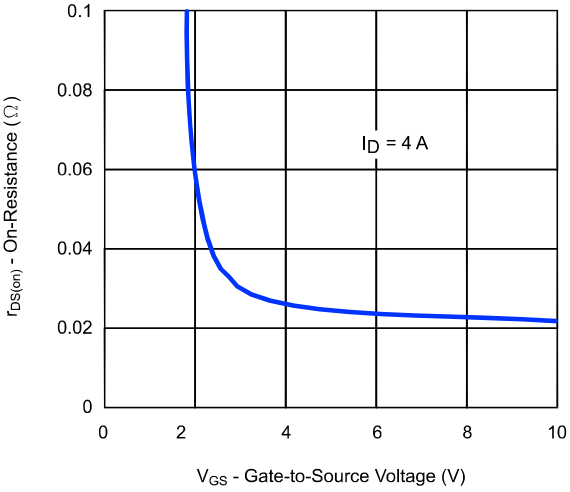
On-Resistance vs. Drain Current



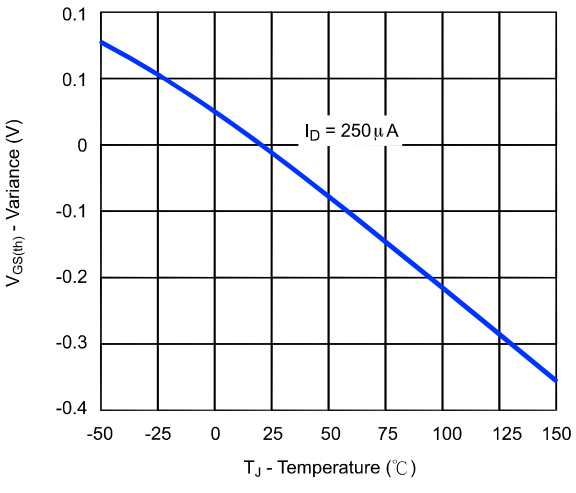
Capacitance



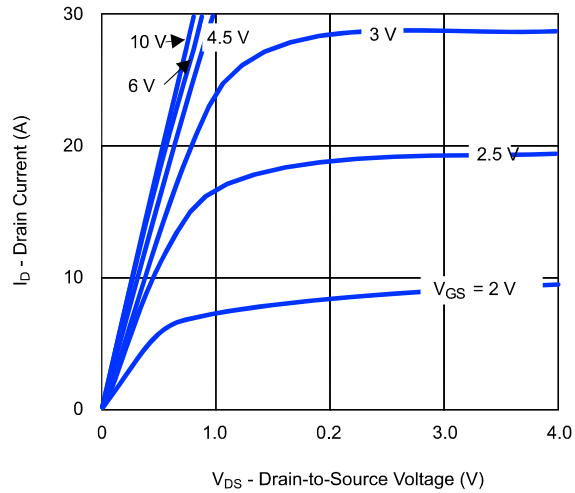
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



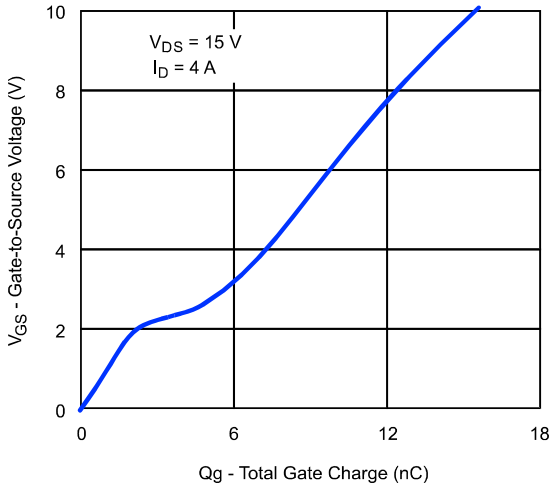
On-Region Characteristics



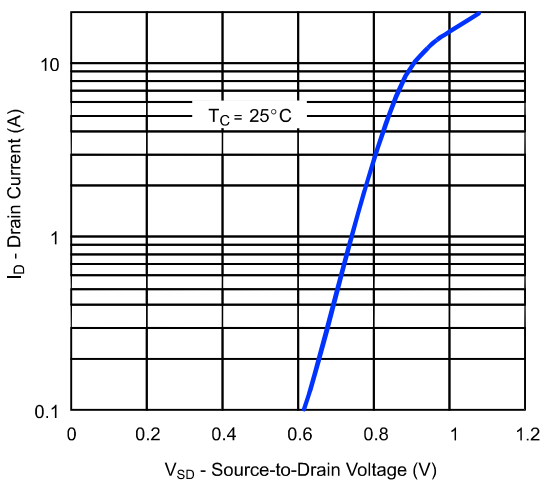
N-Channel Enhancement Mode MOSFET

Typical Characteristics (T_J =25℃ Noted)

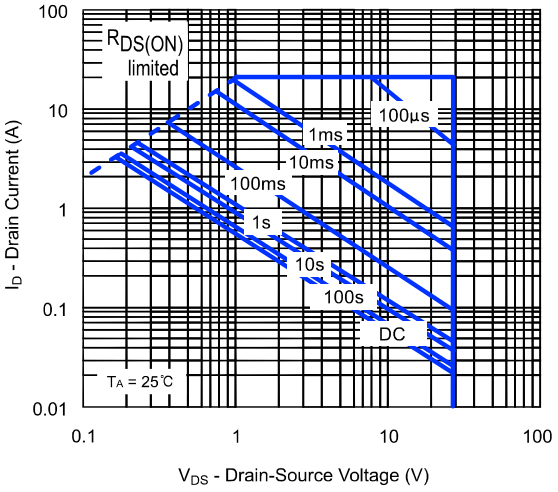
Gate Charge



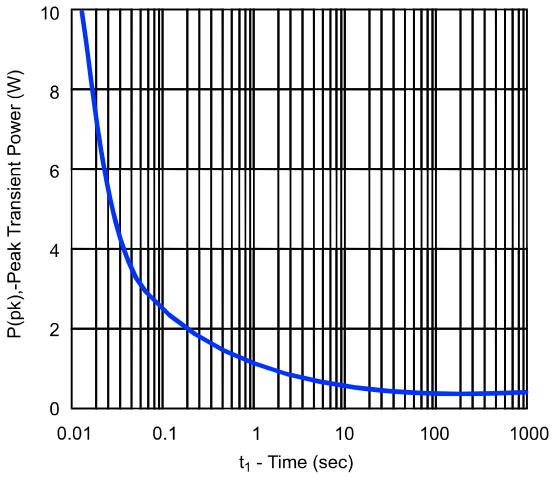
On-Resistance vs. Drain Current



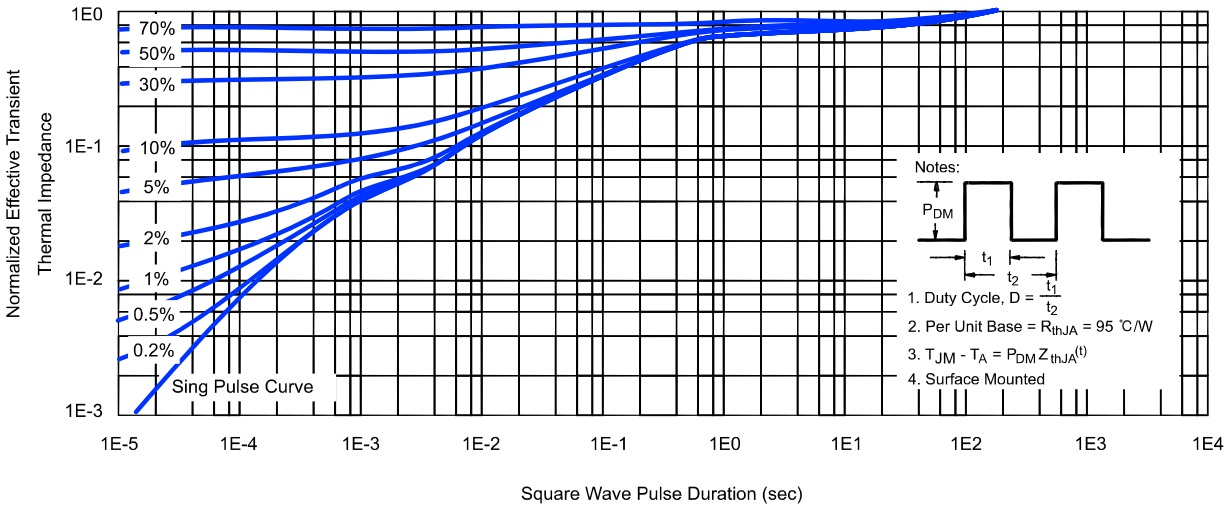
Maximum Forward Biased Safe Operating Area



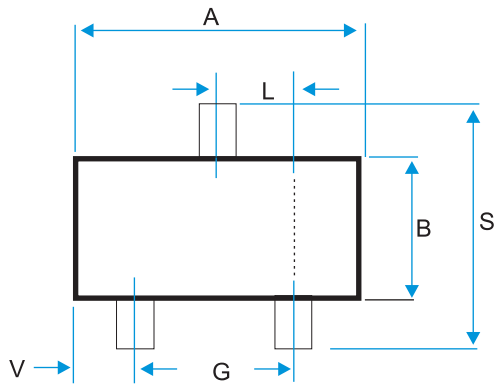
Single Pulse Maximum Power Dissipation

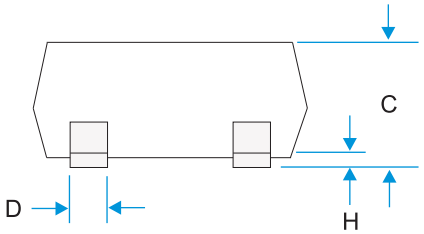


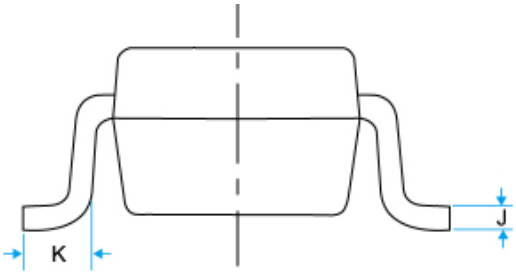
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60