INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8209R

Extended PCI Arbiter and Clock Buffer

Preliminary Specification V0.2

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Revision History

Section	Revision	Page No.
1	• Revised Feature #1 Extended PCI Arbiter descriptions.	1
2	• The descriptions of 2nd paragraph were revised. • Added one sentence at the end of the 2nd paragraph: The algorithm of this arbiter uses a rotation arbitration priority that is illustrated in Figure 2-1. • Added Figure 2-1. Arbitration Scheme of IT8209R.	3
6	• Added section 6 DC Characteristics.	11
7	• Added section 7 AC Characteristics.	13

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1. Features

- **Extended PCI Arbiter**
  - Utilizes 1 set of SYSGNT# and SYSREQ# to support 3 PCI Masters
- **Input PCI Clock**
  - Supports input clock frequency from 25MHz to 66MHz
- **Clock Buffer**
  - Provides 4 zero delay clock sources
  - Supports output clock frequency from 25MHz to 66MHz
- **28-pin SSOP**

2. General Description

The IT8209R incorporates an extended PCI arbiter and a clock buffer.

The extended PCI arbiter utilizes one set of SYSGNT# and SYSREQ# to support 3 PCI Masters, so that two more PCI Masters can be supported for the system. PCISTOP# input signal is useful to facilitate the fairness arbitration. The algorithm of this arbiter uses a rotation arbitration priority that is illustrated in Figure 2-1.

The clock buffer provides 4 zero delay and low jitter clock sources. PCICLKI is the clock input of the clock buffer, and PCICLKOUT is the clock output fed back internally to the input of the built-in PLL to reduce the clock skew. If zero clock skew is required, PCICLKOUT and PCICLK1 to PCICLK4 must be equally loaded.

When PCICLKI input becomes inactive, the IT8209R will enter power down mode. In power down mode, all clock outputs are low and other control outputs are deasserted.

The IT8209R is available in 28-pin SSOP package.

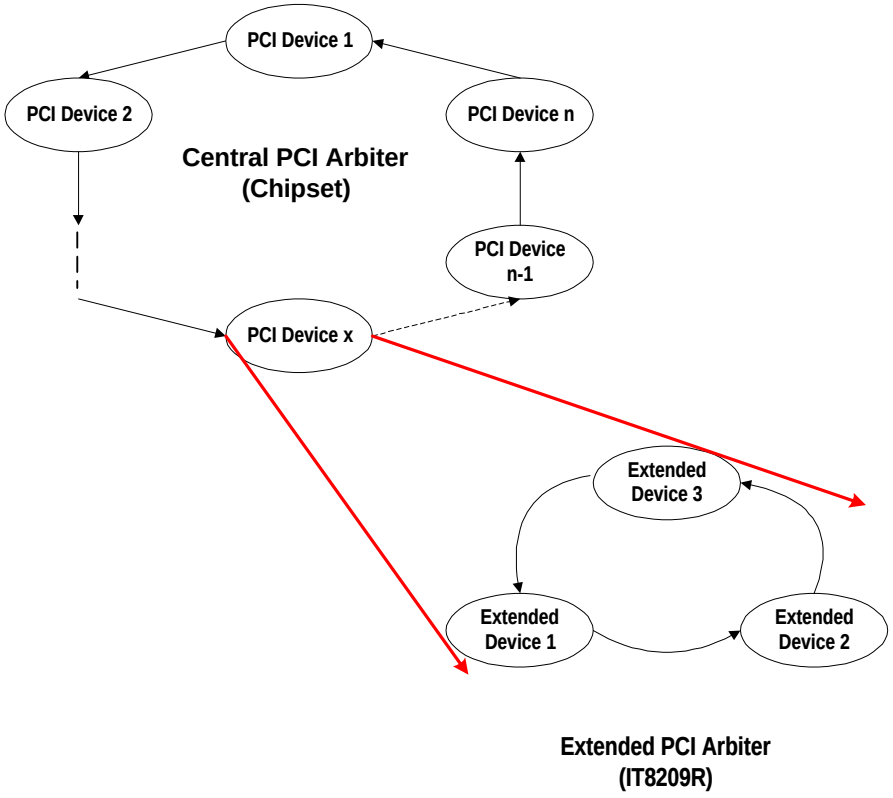


Figure 2-1. Arbitration Scheme of IT8209R

3. Block Diagram

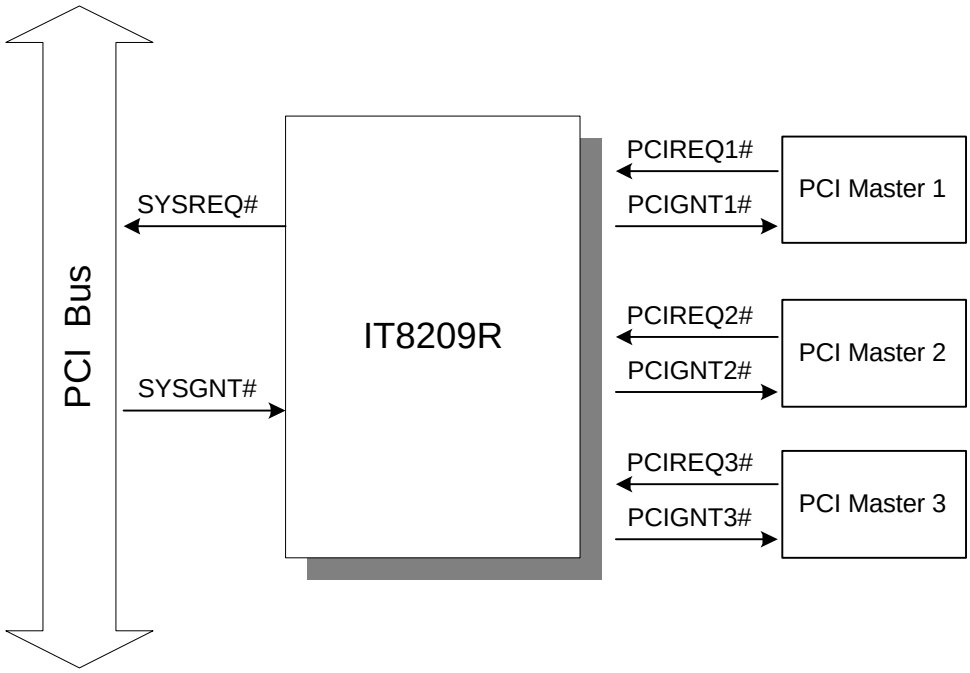


Figure 3-1. Extended PCI Arbiter Scheme

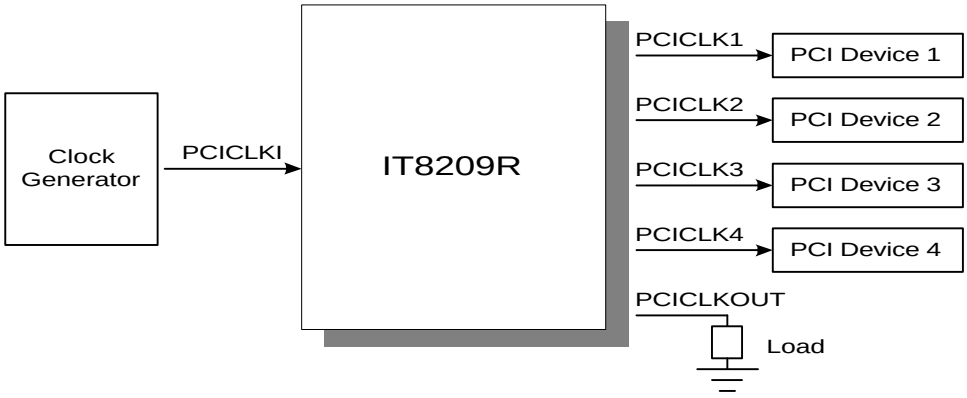
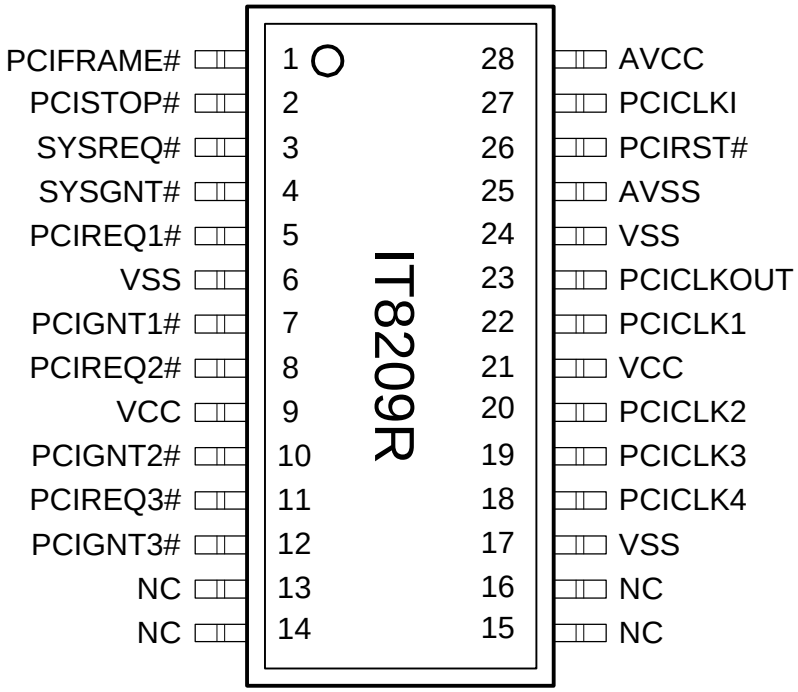


Figure 3-2. Clock Buffer Scheme

4. Pin Configuration



Pin	Signal	Pin	Signal
1	PCIFRAME#	15	NC
2	PCISTOP#	16	NC
3	SYSREQ#	17	VSS
4	SYSGNT#	18	PCICLK4
5	PCIREQ1#	19	PCICLK3
6	VSS	20	PCICLK2
7	PCIGNT1#	21	VCC
8	PCIREQ2#	22	PCICLK1
9	VCC	23	PCICLKOUT
10	PCIGNT2#	24	VSS
11	PCIREQ3#	25	AVSS
12	PCIGNT3#	26	PCIRST#
13	NC	27	PCICLKI
14	NC	28	AVCC

Table 4-1. Pins Listed in Numeric Order

5. IT8209R Pin Descriptions

Table 5-1. Pin Descriptions of Extended PCI Arbiter

Signal	Pin(s) No.	Attribute	Description
Extended PCI Arbiter Signals (3.3V CMOS I/F, 5V tolerant)			
PCIFRAME#	**1**	PIU	***PCI Bus FRAME# Signal*** The pin can be connected to PCI Bus FRAME# signal or not connected to any signals.
PCISTOP#	**2**	PIU	***PCI Bus STOP# Signal***
SYSREQ#	**3**	O12	***PCI Bus Request***
SYSGNT#	**4**	PIU	***PCI Bus Grant***
PCIREQ1#	**5**	PIU	***Request Signal from Extended PCI Master 1***
PCIGNT1#	**7**	O12	***Grant Signal to Extended PCI Master 1***
PCIREQ2#	**8**	PIU	***Request Signal from Extended PCI Master 2***
PCIGNT2#	**10**	O12	***Grant Signal to Extended PCI Master 2***
PCIREQ3#	**11**	PIU	***Request Signal from Extended PCI Master 3***
PCIGNT3#	**12**	O12	***Grant Signal to Extended PCI Master 3***
PCIRST#	**26**	IK	***PCI Bus RST# Signal***

Table 5-2. Pin Descriptions of Clock Buffer

Signal	Pin(s) No.	Attribute	Description
Clock Buffer Signals (3.3V CMOS I/F)			
PCICLK4	**18**	O12	***PCICLK Output 4***
PCICLK3	**19**	O12	***PCICLK Output 3***
PCICLK2	**20**	O12	***PCICLK Output 2***
PCICLK1	**22**	O12	***PCICLK Output 1***
PCICLKOUT	**23**	O12	***PCICLK Output (for internal feedback)***
PCICLKI	**27**	I	***PCICLK Input***

Table 5-3. Pin Descriptions of Power/Ground Signals

Signal	Pin(s) No.	Attribute	Description
Power Ground Signals			
VSS	**6, 17, 24**	I	***Ground***
VCC	**9, 21**	I	***Power Supply of 3.3V***
AVSS	**25**	I	***Analog Ground for analog PLL***
AVCC	**28**	I	***Analog VCC for analog PLL***

Notes: IO cell types are described as below:

I: Input PAD.
IK: Schmitt Trigger Input PAD.
PIU: PCI Bus Specified Input PAD (integrated a 75K ohms pull-up resistor).
O12: 12mA Output PAD.

6. DC Characteristics (VCC, AVCC = 3.3V±0.3V. Ta=0°C to 70°C)

Absolute Maximum Ratings*

Applied Voltage of VCC, AVCC ..... -0.3V to +4.6V

Input Voltage of 3.3V Interface ..... -0.3V to VCC+0.3V

Input Voltage of 5V tolerant Interface … -0.3V to 5.25V

Tcase ..... 0°C to +70°C

Storage Temperature ..... -40°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Ta = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Conditions
V_{IL}	Input Low Voltage	- 0.3V		VCC x 0.2	VCC=3.0 ~ 3.6V
V_{IH}	Input High Voltage	VCC x 0.7		VCC + 0.3V	VCC=3.0 ~ 3.6V
V_{OL}	Output Low Voltage			0.5	I_{OL}= -12mA
V_{OH}	Output High Voltage	2.4			I_{OH}= 12mA
I_{IL}	Input Low Current	-1µA		1µA	V_{IL}= V_{SS} no pull-up or pull-down
I_{IH}	Input High Current	-1µA		1µA	V_{IH}= VCC no pull-up or pull-down
I_{OZ}	Tri-state Leakage Current	-10µA		10µA	
Cin	Input Capacitance		3pF		
Cout	Output Capacitance		3pF		
Cbld	Bi-directional Buffer		3pF		
R_I	Input Pull-Up Resistance	40KΩ	75KΩ	170KΩ	V_{IL} =0V

7. AC Characteristics

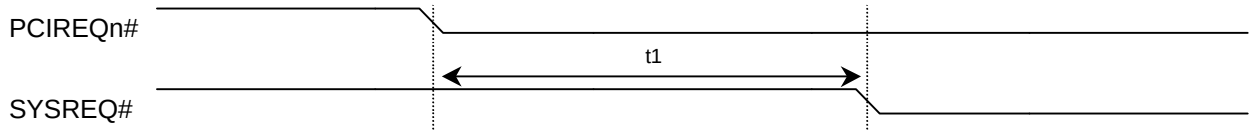


Figure 7-1. PCI Request Delay Timing

Table 7-1. PCI Request Delay Timing Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PCIREQn# (n=1, 2, 3) to SYSREQ# asserted	0	-	7	ns

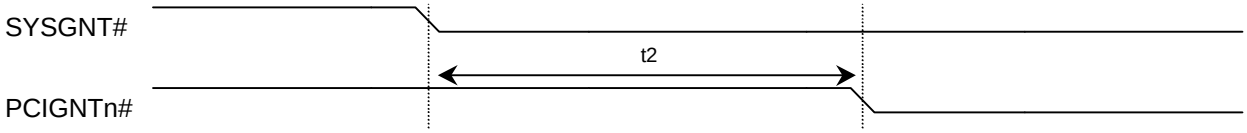


Figure 7-2. PCI Grant Delay Timing

Table 7-2. PCI Grant Delay Timing Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_2	SYSGNT# to PCIGNTn# (n=1, 2, 3) asserted	0	-	8.5	ns

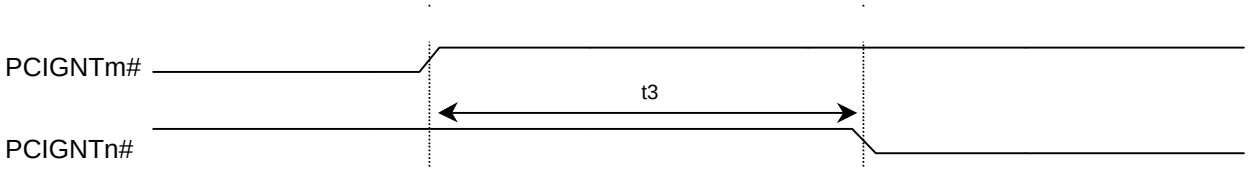


Figure 7-3. PCI Grant Separation Timing

Table 7-3. PCI Grant Separation Timing Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_3	PCIGNTm# (m=1, 2, 3) deasserted to PCIGNTn# (n=1, 2, 3) asserted (n != m)	1	-	-	Clock Period

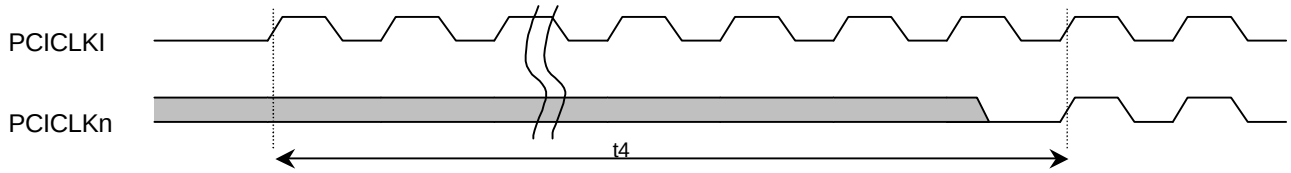


Figure 7-4. PCI Clock Acquisition Timing

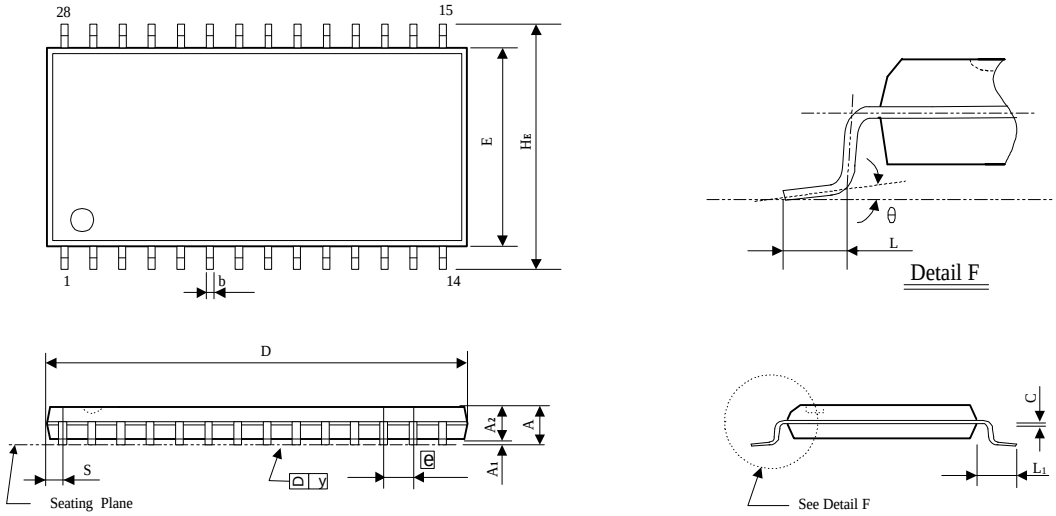
Table 7-4. PCI Clock Acquisition Timing Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_4	PCICLKI stable to PCICLKn (n=1, 2, 3, 4, out) stable	-	-	60	us

8. Package Information

SSOP28L Outline Dimensions

unit: inches/mm



Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.053	0.064	0.069	1.35	1.63	1.75
A_1	0.004	0.006	0.010	0.10	0.152	0.25
A_2	-	-	0.059	-	-	1.50
b	0.008	0.010	0.012	0.203	0.254	0.305
C	0.007	-	0.010	0.178	-	0.250
D	0.386	0.390	0.394	9.80	9.91	10.00
E	0.150	0.154	0.157	3.80	3.91	4.00
e	0.025BSC			0.635BSC		
H_E	0.228	0.236	0.244	5.80	5.99	6.20
L	0.016	0.025	0.050	0.40	0.635	1.27
L_1	0.041REF.			1.04REF.		
S	0.033REF.			0.838REF.		
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

9. Ordering Information

Part No.	Package
IT8209R	28 SSOP