FPD750SOT89

Datasheet 3.0

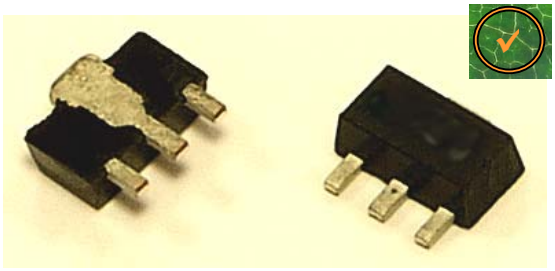
LOW NOISE HIGH LINEARITY PACKAGED PHEMT

FEATURES (1.85GHZ):

- 25 dBm Output Power (P1dB)
- 18 dB Small-Signal Gain (SSG)
- 0.6 dB Noise Figure
- 39 dBm Output IP3
- 55% Power-Added Efficiency
- FPD750SOT89E: RoHS compliant (Directive 2002/95/EC)

PACKAGE:

RoHS



GENERAL DESCRIPTION:

The FPD750SOT89 is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25 µm x 750 µm Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The double recessed gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and i/p power levels.

TYPICAL APPLICATIONS:

- Drivers or output stages in PCS/Cellular base station transmitter amplifiers
- High intercept-point LNAs
- WLL and WLAN systems, and other types of wireless infrastructure systems.

ELECTRICAL SPECIFICATIONS:

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power at 1dB Gain Compression	P1dB	VDS = 5 V; IDS = 50% IDSS	23	25		dBm
Small-Signal Gain	SSG	VDS = 5 V; IDS = 50% IDSS	16.5	18		dB
Power-Added Efficiency	PAE	VDS = 5 V; IDS = 50% IDSS; POUT = P1dB		50		%
Noise Figure	NF	VDS = 5 V; IDS = 50% IDSS VDS = 5 V; IDS = 25% IDSS		0.8 0.6	1.0	dB
Output Third-Order Intercept Point (from 15 to 5 dB below P1dB)	IP3	VDS = 5V; IDS = 50% IDSS Matched for optimal power Matched for best IP3	36	38 39		dBm
Saturated Drain-Source Current	IDSS	VDS = 1.3 V; VGS = 0 V	185	230	280	mA
Maximum Drain-Source Current	IMAX	VDS = 1.3 V; VGS ≅ +1 V		375		mA
Transconductance	GM	VDS = 1.3 V; VGS = 0 V		200		mS
Gate-Source Leakage Current	IGSO	VGS = -5 V		1	15	µA
Pinch-Off Voltage	|VP|	VDS = 1.3 V; IDS = 0.75 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	|VBDGS|	IGS = 0.75 mA	12	16		V
Gate-Drain Breakdown Voltage	|VBDGD|	IGD = 0.75 mA	12	16		V
Thermal Resistance	RθJC			83		°C/W

Note: $T_{AMBIENT}$ = 22°C; RF specification measured at f = 1850 MHz using CW signal (except as noted)

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ABSOLUTE MAXIMUM RATING[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS	-3V < VGS < +0V	8V
Gate-Source Voltage	VGS	0V < VDS < +8V	-3V
Drain-Source Current	IDS	For VDS < 2V	IDSS
Gate Current	IG	Forward or reverse current	7.5mA
RF Input Power[2]	PIN	Under any acceptable bias state	175mW
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-55°C to 150°C
Total Power Dissipation	PTOT	See De-Rating Note below	1.8W
Gain Compression	Comp.	Under any bias conditions	5dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits	

Notes:
[1]$T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device
[2]Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3]Users should avoid exceeding 80% of 2 or more Limits simultaneously
[4]Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$,
where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power
Total Power Dissipation to be de-rated as follows above 22°C:
P_{TOT}= 1.8 - (0.012W/°C) x T_{PACK}
where T_{PACK}= source tab lead temperature above 22°C
(coefficient of de-rating formula is the Thermal Conductivity)
Example: For a 65°C carrier temperature: P_{TOT} = 1.8W – (0.012 x (65 – 22)) = 1.28W

BIASING GUIDELINES:

- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.
- For standard class A operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. A class A/B Bias of 25-33% of IDSS to achieve better OIP3, and Noise Figure performance is suggested.

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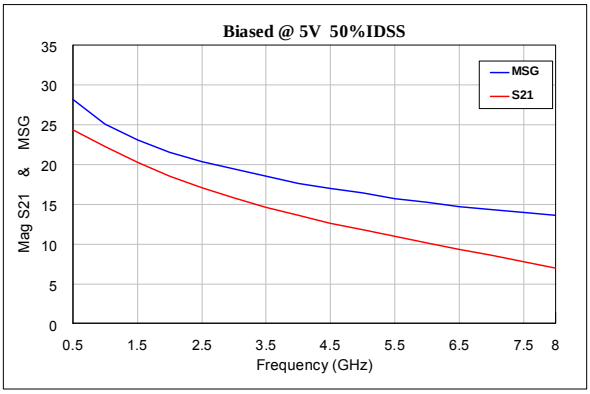
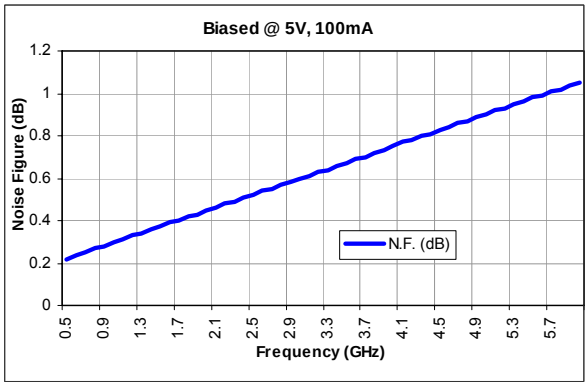
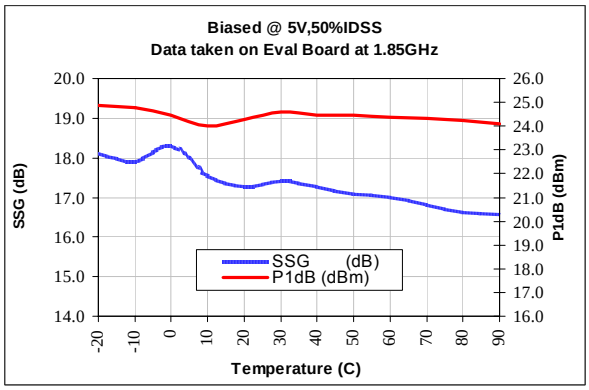
FREQUENCY RESPONSE:

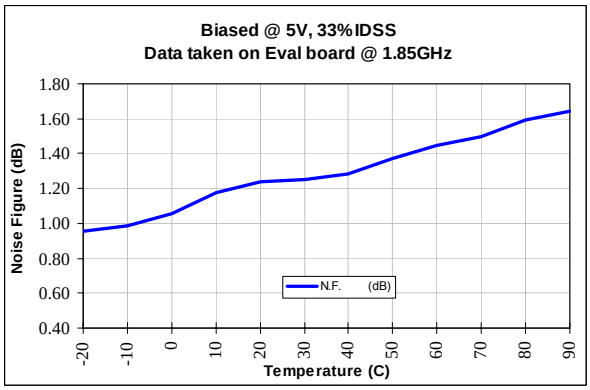




Note: Device tuned for minimum noise figure

TEMPERATURE RESPONSE:





Note: Data Taken on Evaluation board tuned for maximum power. Achievable noise figure is lower when optimized.

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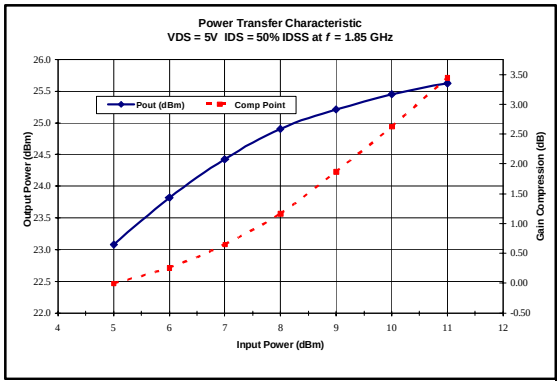
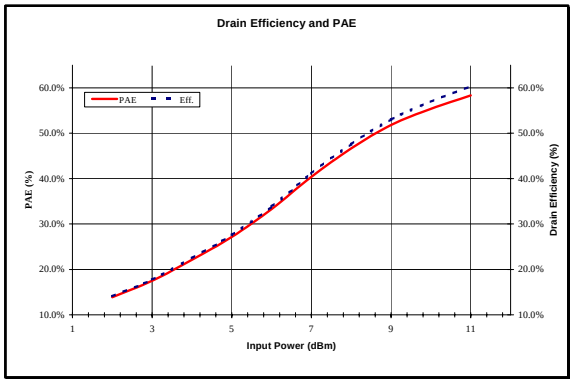
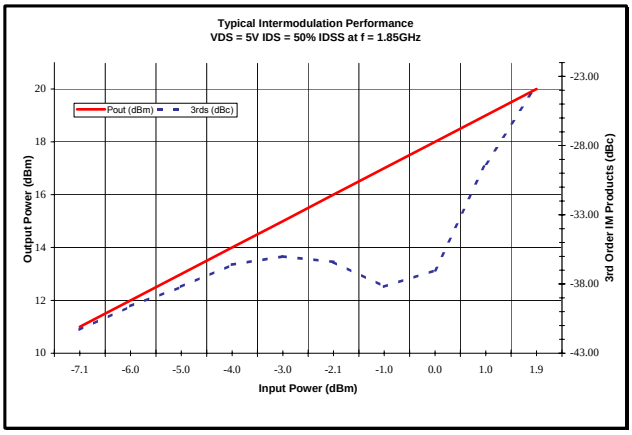
TYPICAL TUNED RF PERFORMANCE:

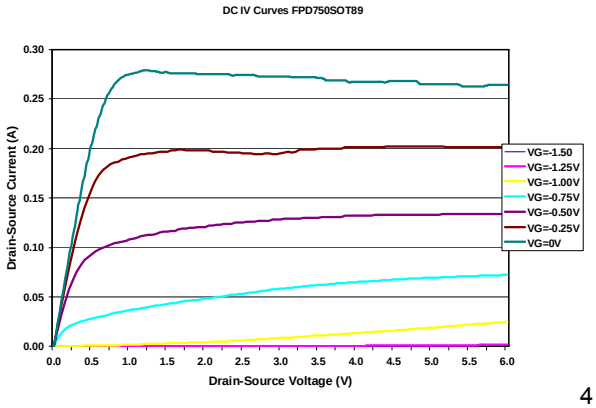




NOTE: Typical power and efficiency is shown above. The devices were biased nominally at V_{DS} = 5V, I_{DS} = 50% of I_{DSS}, at a test frequency of 1.85 GHz. The test devices were tuned (input and output tuning) for maximum output power at 1dB gain compression.



Note: pHEMT devices have enhanced intermodulation performance. This yields OIP3 values of about P_{1dB} + 14dBm. This IMD enhancement is affected by the quiescent bias and the matching applied to the device.



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the V_{DS} > 1.3V will generally cause errors in the current measurements, even in stabilized circuits.

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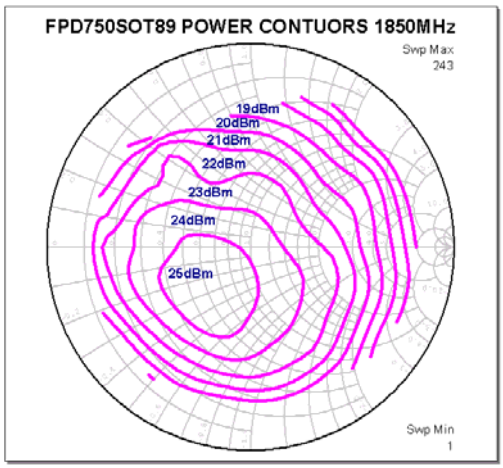
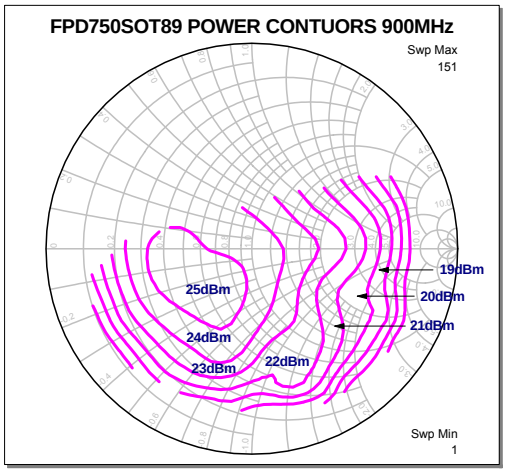
TYPICAL OUTPUT PLANE POWER CONTOURS (VDS = 5v, IDS = 50%IDSS):



1850 MHz

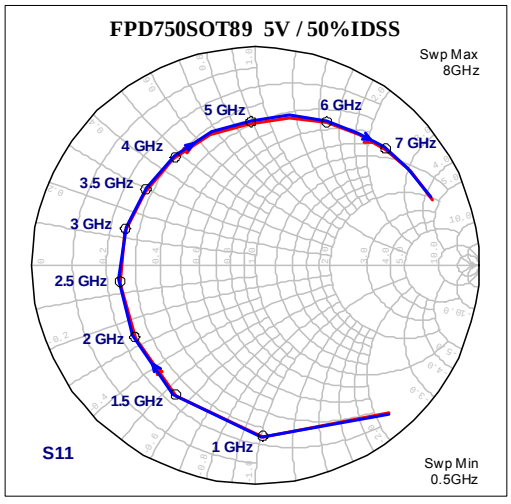
Contours swept with a constant input power, set so that optimum P_{1dB} is achieved at the point of output match.
Input (Source plane) Γ_s:
0.50 ∠ 142.8º
0.37 + j0.35 (normalized)
18.5 + j17.5 Ω
Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

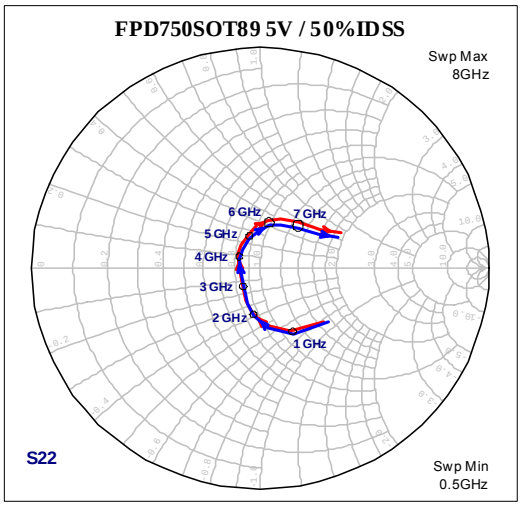


900 MHz

Contours swept with a constant input power, set so that optimum P_{1dB} is achieved at the point of output match.
Input (Source plane) Γ_s:
0.79 ∠ 36.9º
1.0 + j 2.6(normalized)
50 + j130 Ω
Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

TYPICAL SCATTERING PARAMETERS (50Ω SYSTEM):





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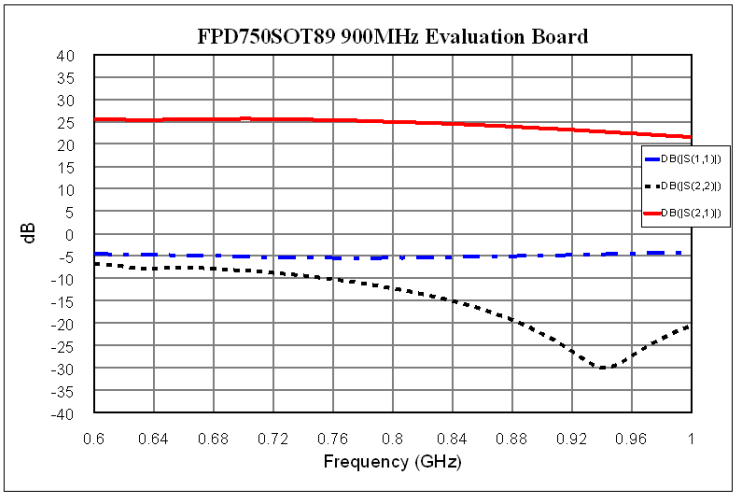
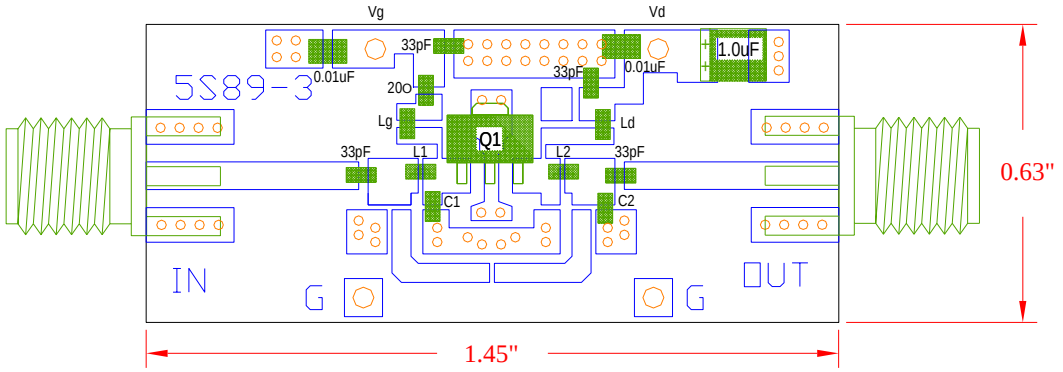
REFERENCE DESIGN (0.9GHZ):

FREQUENCY	GHZ	0.9
Gain	dB	23
P1dB	dBm	23.5
OIP3[1]	dBm	35
N.F.	dB	0.6
S11	dB	-5
S22	dB	-20
Vd	V	5
Vg	V	-0.4 to -0.6
Id	mA	100

1. Measured at 10dBm per tone



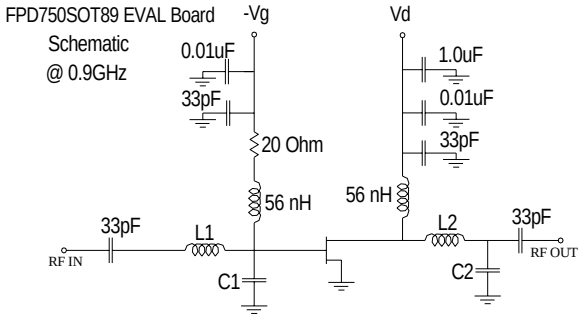
Board Layout



Component Values

Component	Value	Description
Lg	56nH	LL1608 Toko chip inductor
Ld	56nH	LL1608 Toko chip inductor
L1	12nH	LL1608 Toko chip inductor
L2	6.8nH	LL1608 Toko chip inductor
C1	0.5pF	ATC 600S chip capacitor
C2	1.2pF	ATC 600S chip capacitor

Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides



D.C. Blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20 Ohm Chip resistor from Vishay is used on the gate D.C. bias line for stability.

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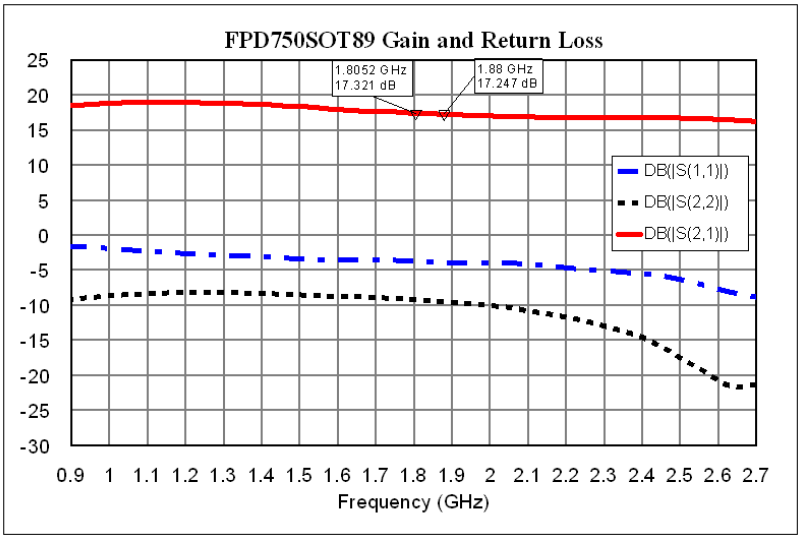
REFERENCE DESIGN (1.85GHZ):

FREQUENCY	GHZ	1.85
Gain	dB	17.2
P1dB	dBm	24
OIP3[1]	dBm	35
N.F.	dB	0.7
S11	dB	-5
S22	dB	-10
Vd	V	5
Vg	V	-0.4 to -0.6
Id	mA	100

1. Measured at 10dBm per tone



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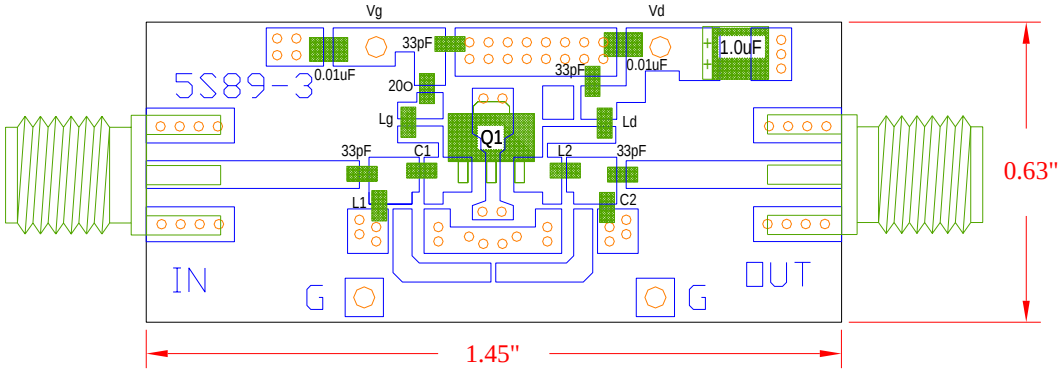
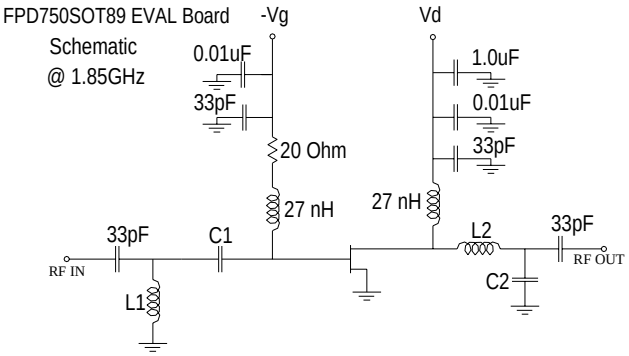


Component Values

Component	Value	Description
Lg	27nH	LL1608 Toko chip inductor
Ld	27nH	LL1608 Toko chip inductor
L1	6.8nH	LL1005 Toko chip inductor
L2	1.8nH	LL1005 Toko chip inductor
C1	2.7pF	ATC 600S chip capacitor
C2	0.5pF	ATC 600S chip capacitor

Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides



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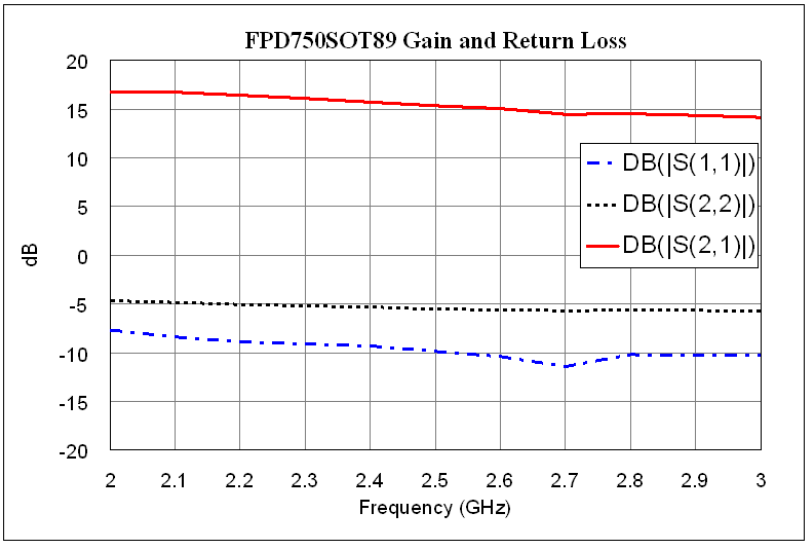
REFERENCE DESIGN (2.4GHZ TO 2.6GHZ):

Frequency (GHz)	2.4	2.5	2.6
SSG (dB)	15.4	15.2	15.0
P1dB (dBm)	24.3	24.3	24.4
OIP3 (dBm)[1]	34.0	35.0	34.0
N.F. (dB)	0.95	0.95	1.0
S11 (dB)	-5.0	-5.5	-6.0
S22 (dB)	-9.5	-10.0	-10.0
VD (V)	5		
VG (V)	-0.4 to -0.6		
ID (mA)	100		

1. Measured at 10dBm per tone



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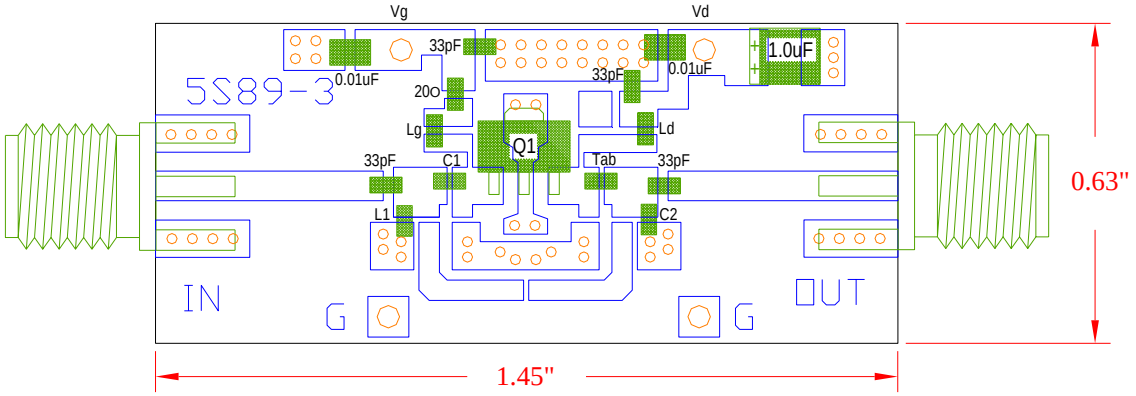
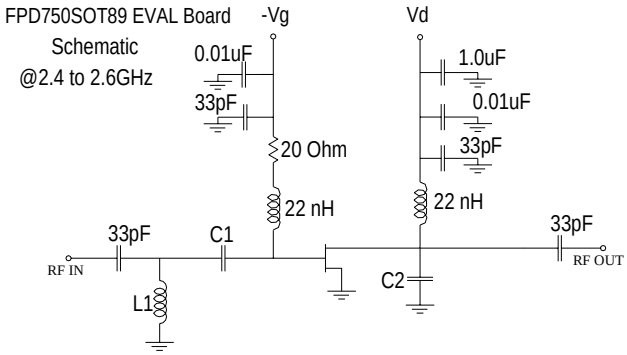


Component Values

Component	Value	Description
Lg	22nH	LL1608 Toko chip inductor
Ld	22nH	LL1608 Toko chip inductor
L1	8.2nH	LL1005 Toko chip inductor
C1	2.0pF	ATC 600S chip capacitor
C2	0.8pF	ATC 600S chip capacitor
Tab		Copper tab (no component)

Eval board material - 31mil thick FR4 with 1/2 Ounce Cu on both sides



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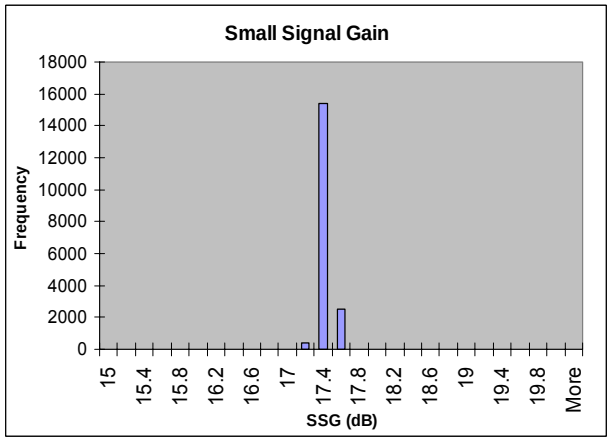
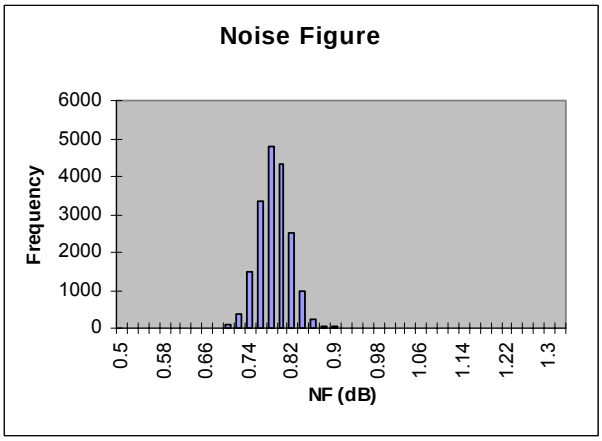
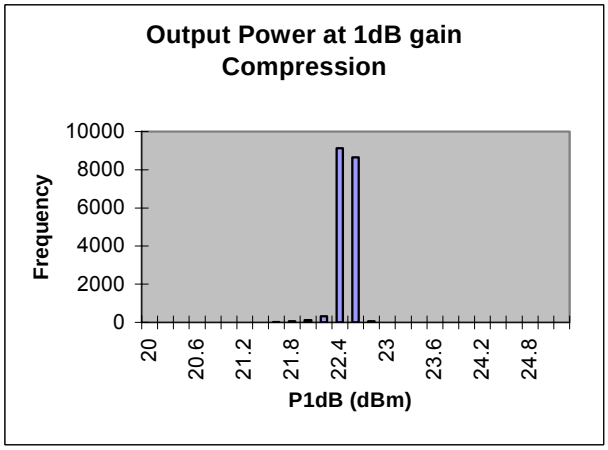
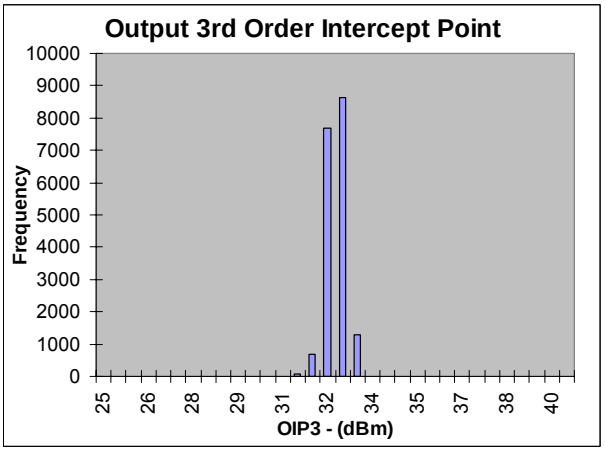
STATISTICAL SAMPLE OF RF PERFORMANCE:









Note: The devices were tested by a high-speed automatic test system, in a matched circuit based on an Evaluation Board design. This circuit is a dual-bias single-pole low pass topology, and the devices were biased at **V_{DS} = 4.0V, I_{DS} = 100mA, Test frequency = 2.0GHz.**

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S-PARAMETERS: BIASED @ 5V, 50%IDSS:

FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.050	0.998	-5.6	19.465	172.4	0.003	94.4	0.448	-8.1
0.300	0.959	-30.9	16.931	154.5	0.016	77.5	0.438	-20.6
0.550	0.868	-52.5	15.126	137.7	0.028	64.7	0.406	-37.7
0.800	0.809	-72.3	13.452	124.3	0.038	55.2	0.379	-51.8
1.050	0.755	-90.2	12.024	112.1	0.046	47.2	0.352	-64.3
1.300	0.713	-106.5	10.762	101.4	0.052	40.7	0.324	-74.4
1.550	0.679	-121.5	9.707	91.8	0.057	35.1	0.294	-83.0
1.800	0.653	-135.6	8.828	82.7	0.062	29.2	0.267	-91.1
2.050	0.634	-148.8	8.080	74.1	0.066	24.3	0.241	-98.8
2.300	0.62	-161.8	7.441	66.0	0.069	19.4	0.214	-106.3
2.550	0.613	-173.5	6.890	58.1	0.073	14.9	0.188	-115.6
2.800	0.603	175.0	6.407	50.2	0.076	10.5	0.169	-125.9
3.050	0.611	164.6	5.948	43.0	0.078	6.0	0.14	-140.7
3.300	0.614	154.5	5.557	35.7	0.080	2.2	0.123	-156.6
3.550	0.619	145.1	5.194	28.7	0.082	-2.4	0.113	-175.2
3.800	0.627	136.2	4.873	21.9	0.084	-6.0	0.11	164.9
4.050	0.636	127.9	4.594	15.4	0.085	-10.3	0.114	146.6
4.300	0.659	119.7	4.345	8.8	0.086	-13.3	0.133	132.4
4.550	0.663	110.6	4.138	1.8	0.089	-17.5	0.138	115.2
4.800	0.666	104.1	3.892	-4.8	0.090	-21.4	0.153	107.8
5.050	0.68	96.9	3.690	-11.0	0.091	-25.1	0.167	99.7
5.300	0.695	89.7	3.511	-17.4	0.092	-29.2	0.182	92.6
5.550	0.706	82.6	3.342	-23.7	0.093	-32.6	0.196	85.4
5.800	0.719	75.9	3.190	-30.1	0.094	-36.8	0.208	78.5
6.050	0.732	69.2	3.041	-36.5	0.095	-41.0	0.222	71.6
6.300	0.741	62.7	2.898	-42.8	0.096	-45.1	0.237	65.0
6.550	0.754	56.9	2.766	-49.1	0.096	-49.1	0.252	58.0
6.800	0.766	51.1	2.634	-55.3	0.095	-53.0	0.27	51.3
7.050	0.779	45.4	2.507	-61.6	0.095	-57.4	0.291	44.6
7.300	0.793	39.9	2.387	-67.8	0.095	-61.4	0.314	38.5
7.550	0.809	34.4	2.267	-73.9	0.093	-65.7	0.337	33.2
7.800	0.823	28.9	2.151	-79.9	0.092	-70.0	0.363	28.4
8.050	0.839	23.6	2.036	-85.7	0.091	-74.0	0.387	24.3
8.300	0.851	18.8	1.925	-91.3	0.089	-78.3	0.412	20.3
8.550	0.86	14.2	1.825	-96.7	0.087	-81.9	0.436	17.1
8.800	0.871	9.8	1.728	-102.0	0.084	-85.5	0.457	14.0
9.050	0.881	5.7	1.640	-106.9	0.083	-89.4	0.477	11.0
9.300	0.889	2.0	1.563	-111.8	0.082	-93.9	0.496	8.6
9.550	0.895	-1.5	1.494	-116.6	0.081	-98.4	0.514	6.0
9.800	0.904	-4.6	1.433	-121.2	0.080	-101.8	0.531	3.1
10.050	0.913	-8.3	1.384	-126.5	0.078	-107.1	0.548	-0.1
10.300	0.909	-12.0	1.323	-132.0	0.075	-111.9	0.552	-3.6
10.550	0.903	-15.2	1.264	-136.8	0.074	-116.6	0.557	-6.7

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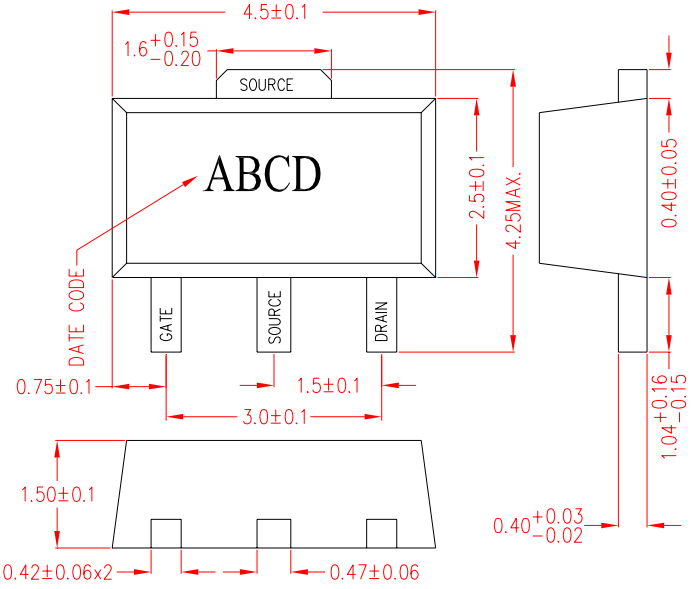
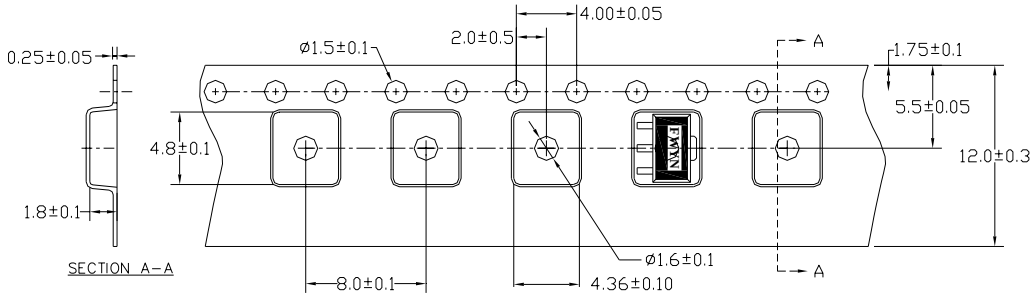
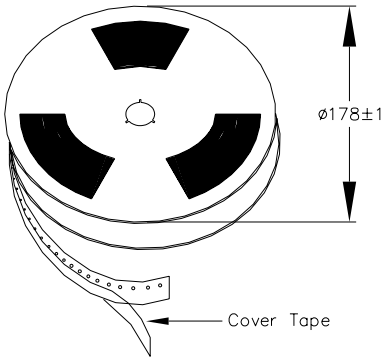
PACKAGE OUTLINE:
(dimensions in millimeters – mm)



TAPE DIMENSIONS AND PART ORIENTATION:



DIMENSIONS ARE IN MM



- Also available with horizontal part orientation
- Hub diameter = 80mm
- Devices per reel = 1000

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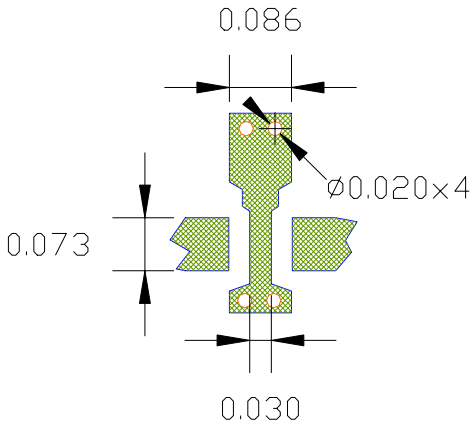
DEVICE FOOT PRINT:



Units in inches

NOTE: Drawing available on Website

PREFERRED ASSEMBLY INSTRUCTIONS:

This package is compatible with both lead free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020C. The maximum package temperature should not exceed 260°C.

HANDLING PRECAUTIONS:

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD/MSL RATING:

These devices should be treated as Class 1A (250-500 V) using the human body model as defined in JEDEC Standard No. 22-A114.

The device has a MSL rating of Level 2. To determine this rating, preconditioning was performed to the device per, the Pb-free solder profile defined within IPC/JEDEC J-STD-020C, Moisture / Reflow sensitivity classification for non-hermatic solid state surface mount devices.

APPLICATION NOTES & DESIGN DATA:

Application Notes and design data including S-parameters, noise parameters and device model are available on request.

RELIABILITY:

A MTTF of 7.4 million hours at a channel temperature of 150°C is achieved for the process used to manufacture this device.

DISCLAIMERS:

This product is not designed for use in any space based or life sustaining/supporting equipment.

ORDERING INFORMATION:

PART NUMBER	DESCRIPTION
FPD750SOT89	Packaged pHEMT
FPD750SOT89E	Lead free Packaged pHEMT
FPD750SOT89CE	RoHS Compliant Packaged pHEMT with enhanced passivation (Recommended for New Designs)
EB750SOT89(E)-BB	0.9 GHz evaluation board
EB750SOT89(E)-BA	1.85 GHz evaluation board
EB750SOT89(E)-BC	2.0 GHz evaluation board
EB750SOT89(E)-BE	2.4 GHz evaluation board
EB750SOT89(E)-BG	2.6 GHz evaluation board
EB750SOT89(E)-AH	3.5 GHz evaluation board
EB750SOT89(E)-AJ	5.0 – 5.75 GHz evaluation board

Specifications subject to change without notice
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