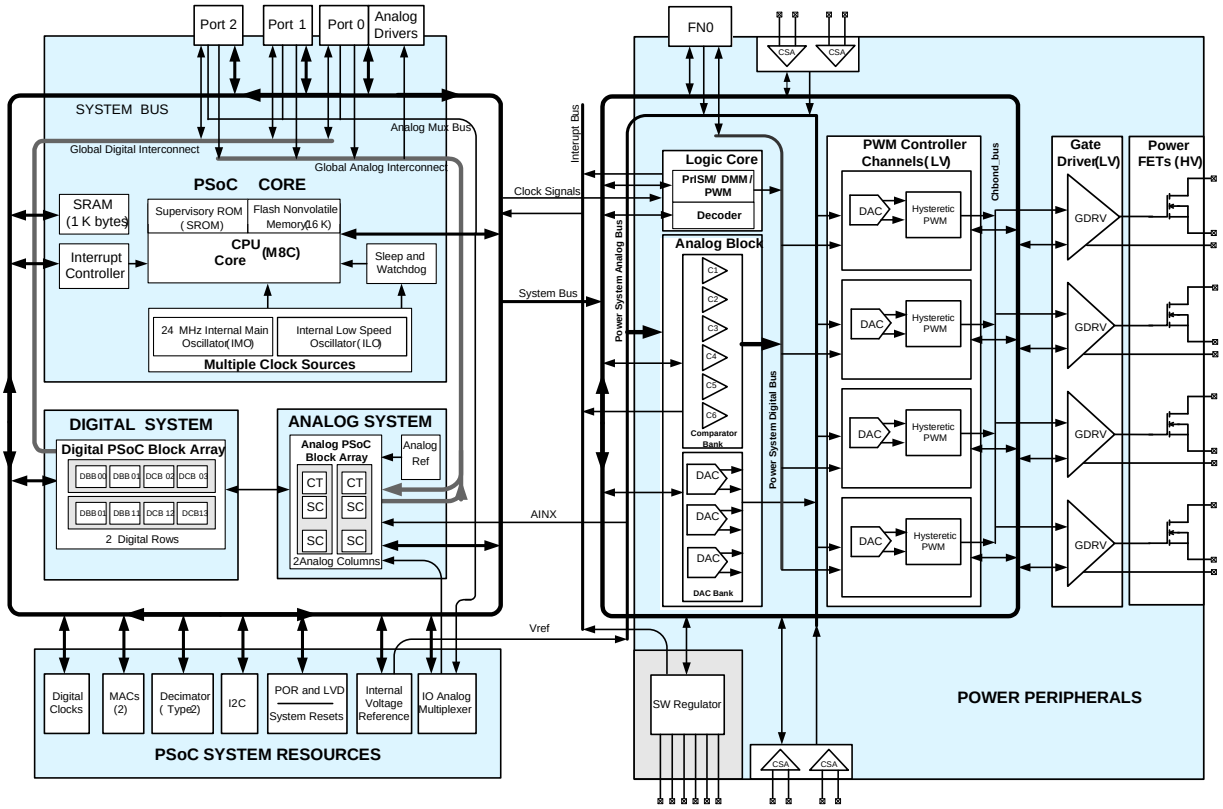
PowerPSoC® Intelligent LED Driver

1. Features

- **Integrated Power Peripherals**
  - Four internal 32V low side N-Channel power FETs
    - $R_{DS(ON)}$– 0.5Ω for 1.0A devices
    - Up to 2 MHz configurable switching frequency
  - Four hysteretic controllers
    - Independently programmable upper and lower thresholds
    - Programmable minimum on/off timers
  - Four low side gate drivers with programmable drive strength
  - Four precision high side current sense amplifiers
  - Three 16-bit LED dimming modulators: PrISM, DMM, and PWM
  - Six fast response (100 ns) voltage comparators
  - Six 8-bit reference DACs
  - Built-in switching regulator eliminates external 5V supply
  - Multiple topologies including floating load buck, floating load buck-boost, and boost
- **M8C CPU Core**
  - Processor speeds up to 24 MHz
- **Advanced Peripherals (PSoC® Blocks)**
  - Capacitive sensing application capability
  - DMX512 interface
  - DALI interface
  - I2C master or slave
  - Full-duplex UARTs
  - Multiple SPI masters or slaves
  - Integrated temperature sensor
  - Up to 12-bit ADCs
  - 6 to 12-bit incremental ADCs
  - Up to 9-bit DACs
  - Programmable gain amplifiers
  - Programmable filters and comparators
  - 8 to 32-bit timers and counters
  - Complex peripherals by combining blocks
  - Configurable to all GPIO pins
- **Programmable Pin Configurations**
  - 25 mA sink on all GPIO and function pins
  - Pull up, pull down, high Z, strong, or open drain drive modes on all GPIO and function pins
  - Up to 10 analog inputs on GPIO
  - Two 30 mA analog outputs on GPIO
  - Configurable interrupt on all GPIO
- **Flexible On-chip Memory**
  - 16K Flash program storage 50,000 erase and write cycles
  - 1K SRAM data storage
  - In-System Serial Programming (ISSP)
  - Partial Flash updates
  - Flexible protection modes
  - EEPROM emulation in Flash
- **Complete Development Tools**
  - Free development software: PSoC Designer 5.0™
  - Full featured, In-Circuit Emulator and Programmer
  - Full speed emulation
  - Complex breakpoint structure
  - 128 kBytes trace memory
- **Visual Embedded Design**
  - LED based express drivers
  - Binning compensation
  - Temperature feedback
- **Applications**
  - Stage LED lighting
  - Architectural LED lighting
  - General purpose LED lighting
  - Automotive and emergency vehicle LED lighting
  - Landscape LED lighting
  - Display LED lighting
  - Effects LED lighting
  - Signage LED lighting
- **Device Options**
  - CY8CLED04D0x
    - Four internal FETs with 0.5A and 1.0A options
    - Four external gate drivers
  - CY8CLED04G01
    - Four external gate drivers
  - CY8CLED03D0x
    - Three internal FETs with 0.5A and 1.0A options
    - Three external gate drivers
  - CY8CLED03G01
    - Three external gate drivers
  - CY8CLED02D01
    - Two 1.0A internal FETs
    - Two external gate drivers
  - CY8CLED01D01
    - One 1.0A internal FET
    - One external gate driver
- **56-pin QFN Package**

Figure 1-1. PowerPSoC Architectural Block Diagram



2. Logic Block Diagrams

Figure 2-1. CY8CLED04D0x Logic Block Diagram

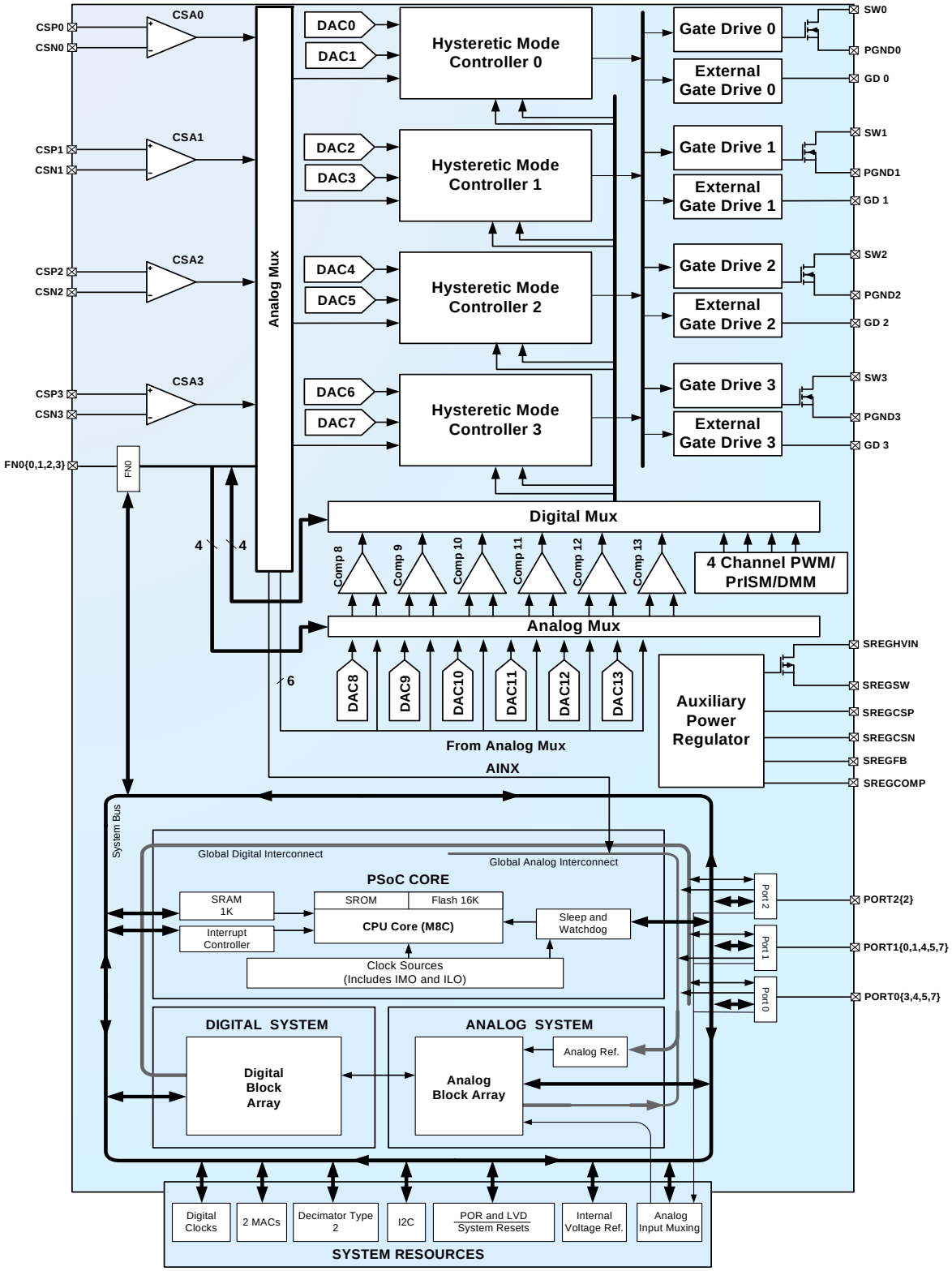


Figure 2-2. CY8CLED04G01 Logic Block Diagram

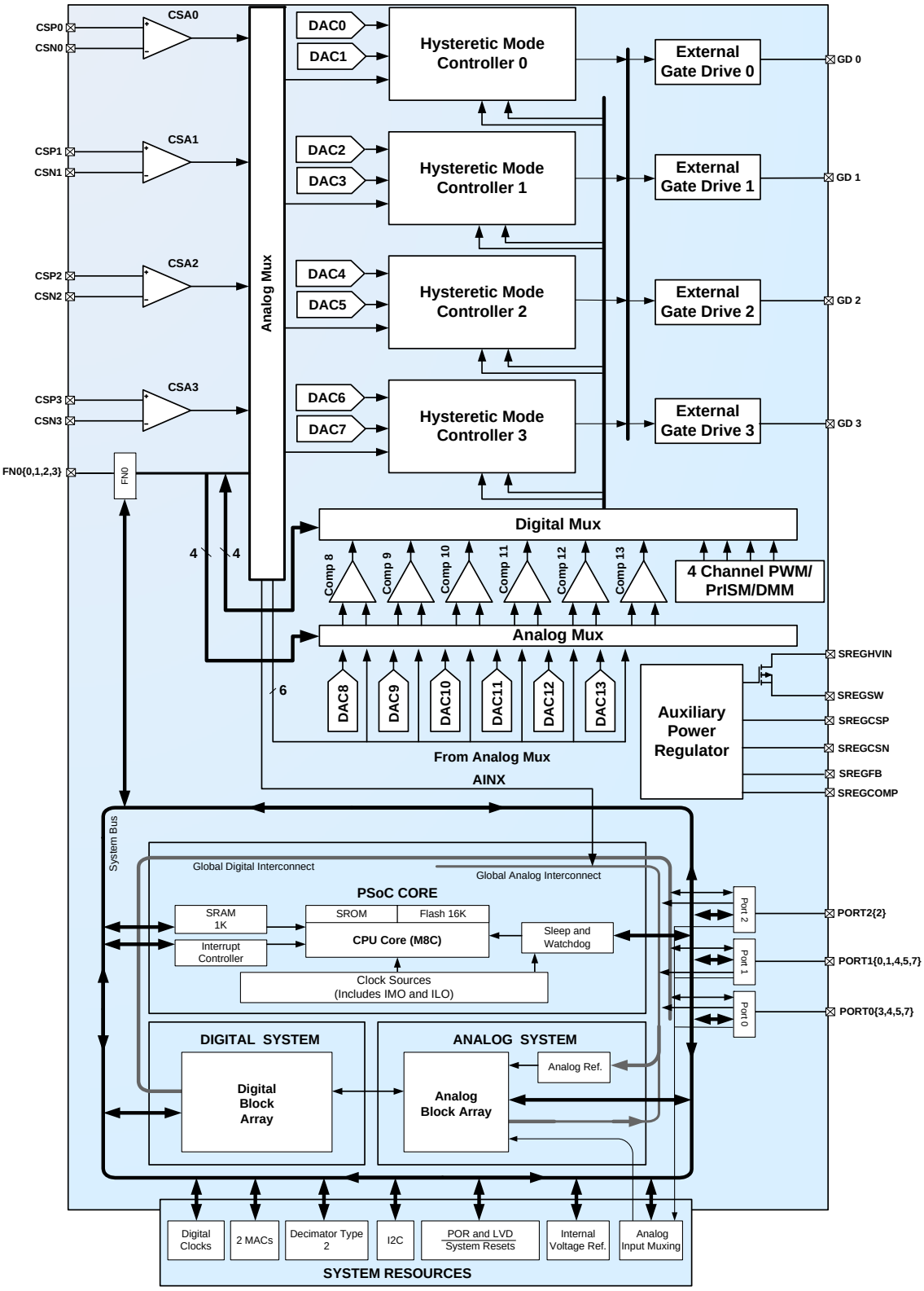


Figure 2-3. CY8CLED03D0x Logic Block Diagram

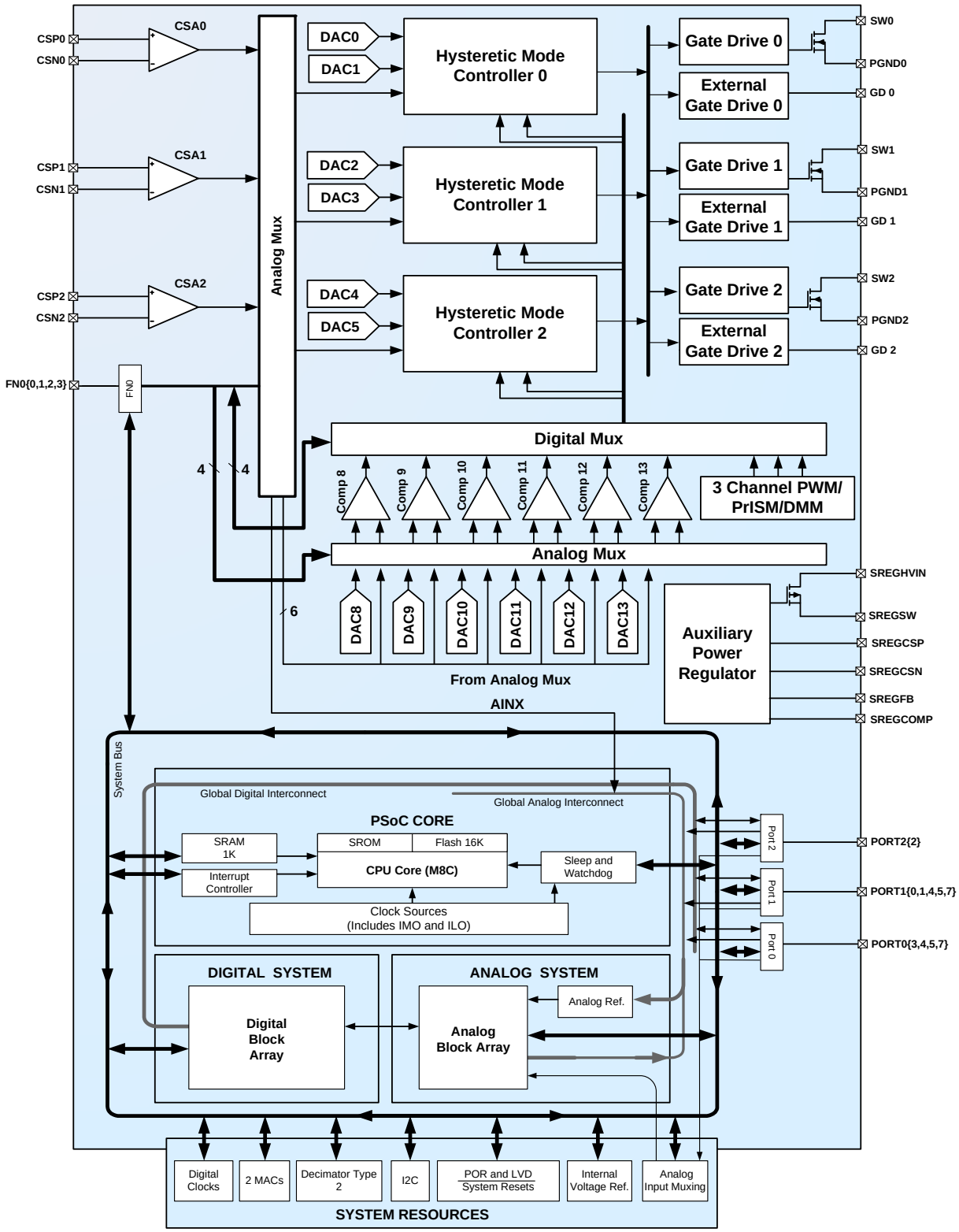


Figure 2-4. CY8CLED03G01 Logic Block Diagram

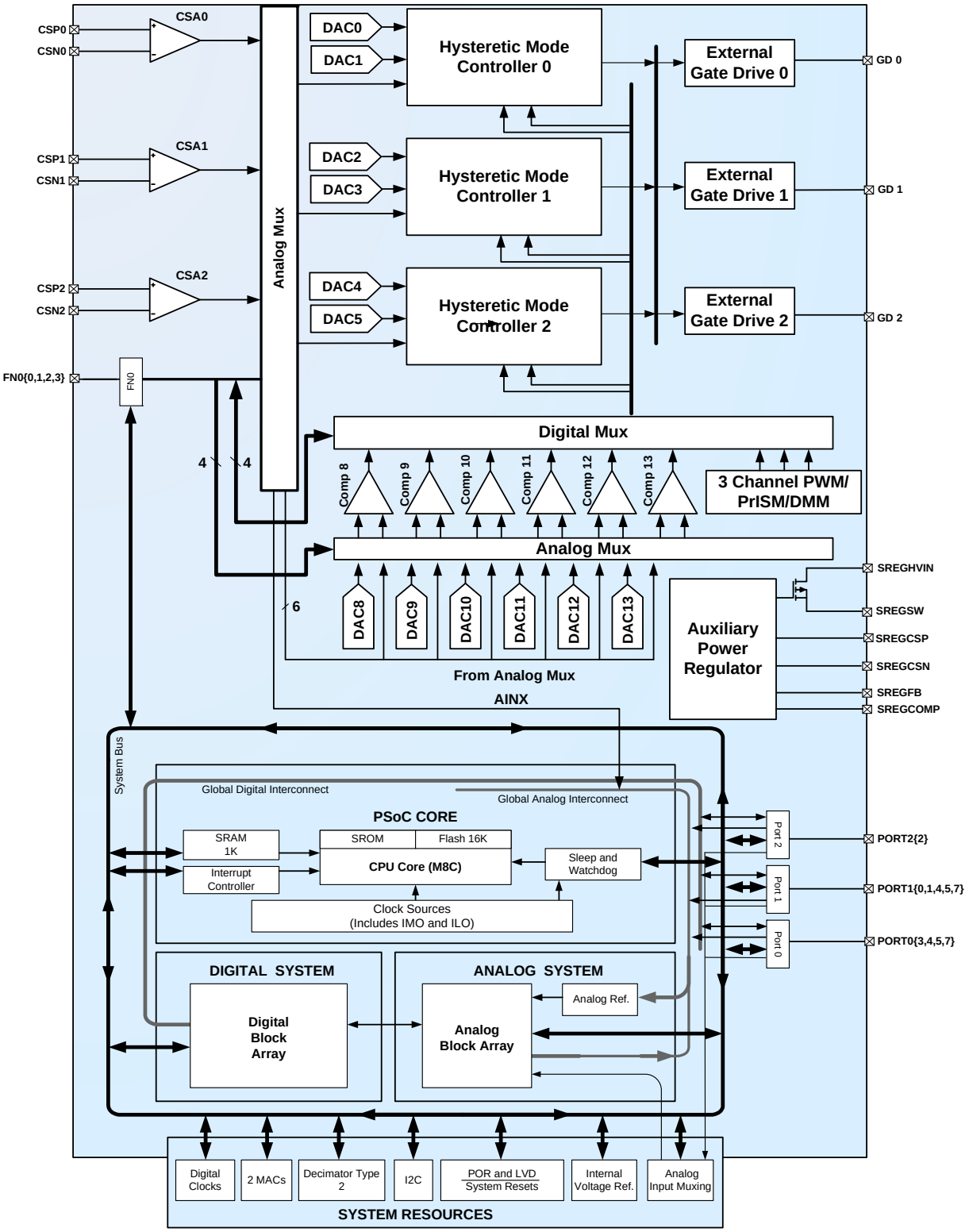


Figure 2-5. CY8CLED02D01 Logic Block Diagram

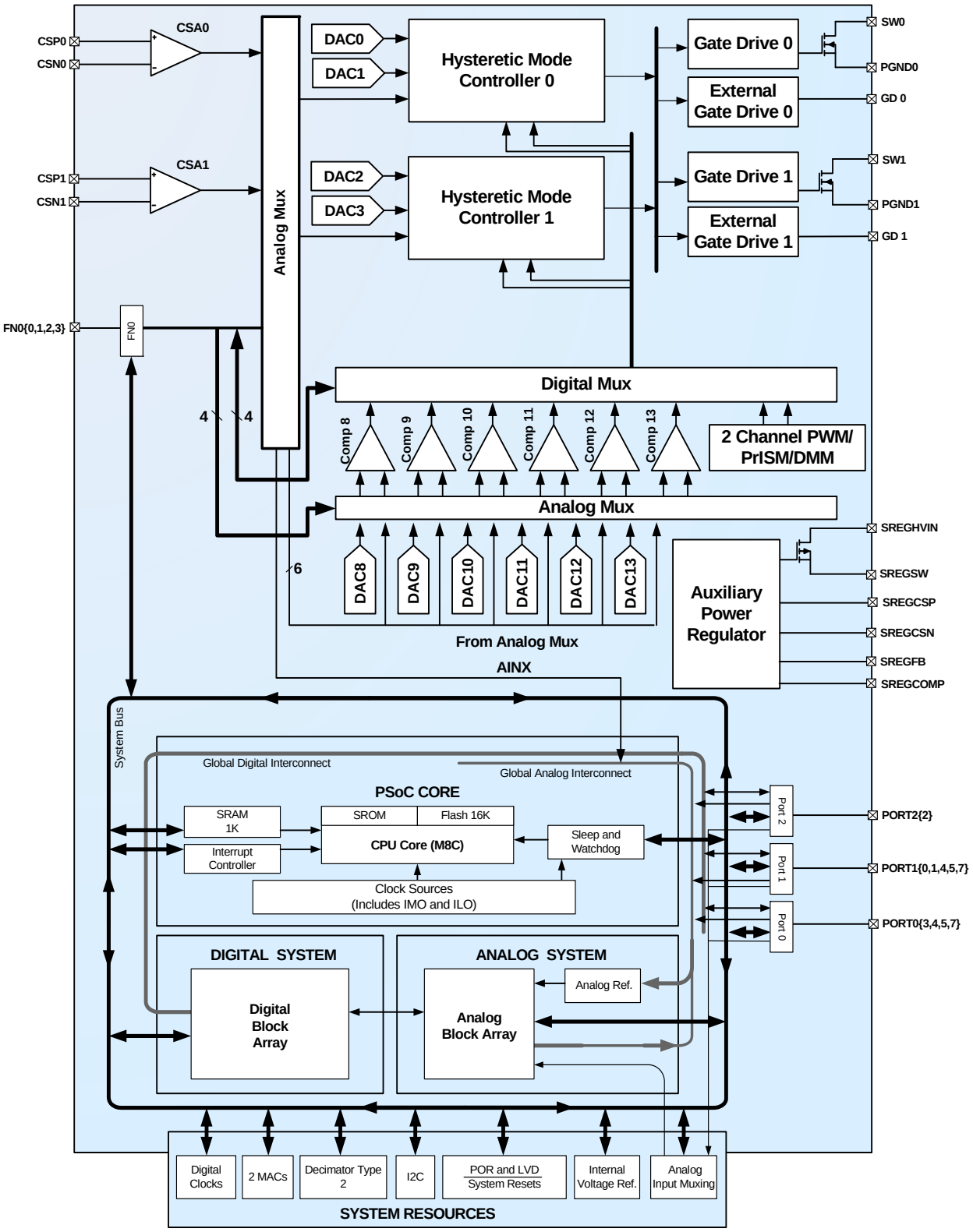
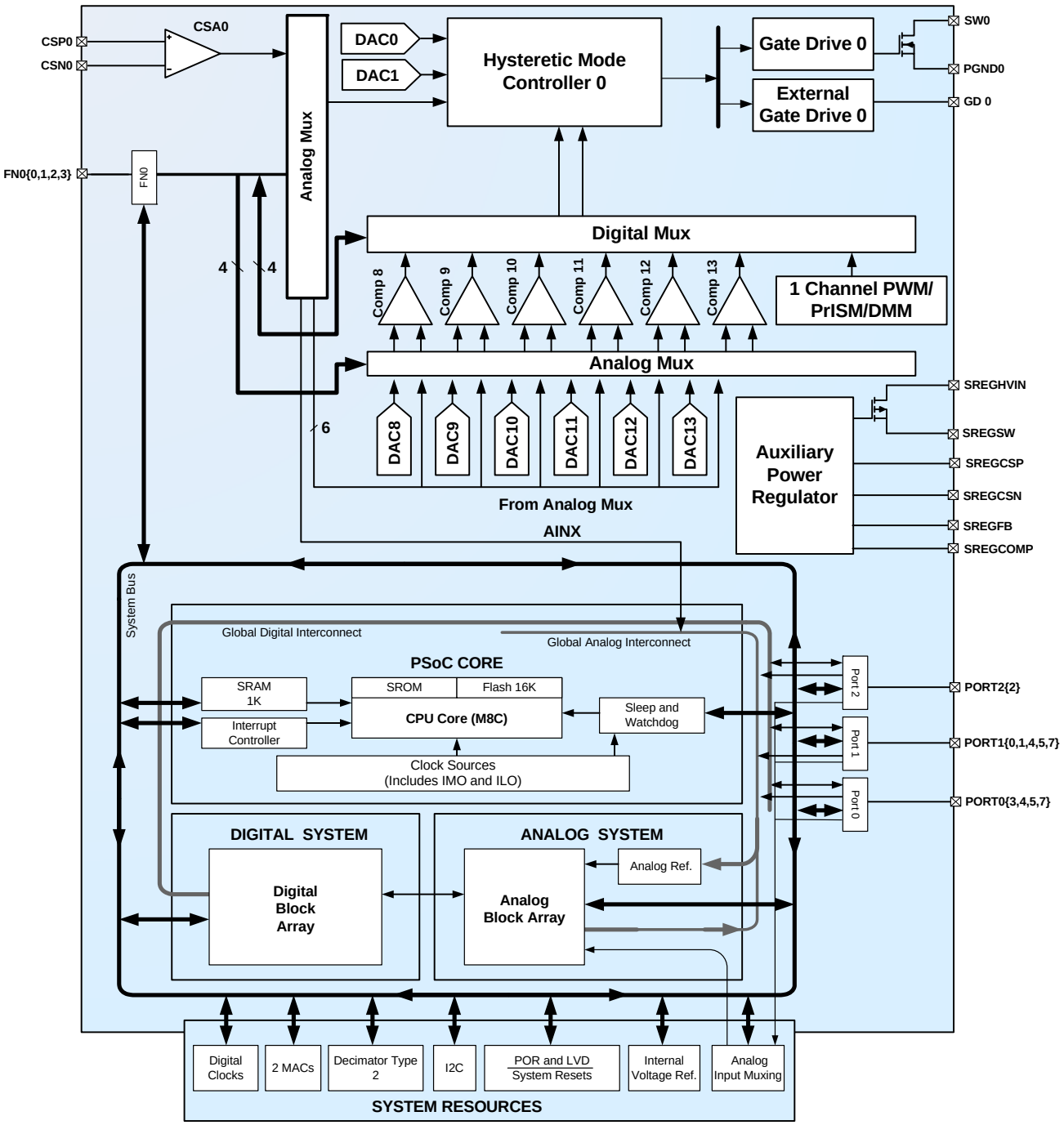


Figure 2-6. CY8CLED01D01 Logic Block Diagram



3. PowerPSoC® Functional Overview

The PowerPSoC family incorporates programmable system-on-chip technology with the best in class power electronics controllers and switching devices to create easy to use power-system-on-chip solutions for lighting applications.

All PowerPSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. PowerPSoC devices feature high performance power electronics including 1A 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators to create a complete power electronics solution for LED power management. Configurable power, analog, digital, and interconnect circuitry enables a high level of integration in a host of industrial, commercial, and consumer LED lighting applications.

This architecture integrates programmable analog and digital blocks to enable the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, the device includes a fast CPU, Flash program memory, SRAM data memory, and configurable I/O in a range of convenient pinouts and packages.

The PowerPSoC architecture, as illustrated in the block diagrams, comprises five main areas: PSoC core, digital system, analog system, system resources, and power peripherals which include power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. Configurable global busing combines all the device resources into a complete custom system. The PowerPSoC family of devices have 10-port I/Os that connect to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

4. Power Peripherals

The CY8CLED04D0X is the first product in the PowerPSoC family to integrate power peripherals to add further integration for your power electronics applications.The PowerPSoC family of intelligent power controller ICs are used in lighting applications that need traditional MCUs and discrete power electronics support. The power peripherals of the CY8CLED04D0X include four 32V power MOSFETs with current ratings up to 1A each. It also integrates gate drivers that enable applications to drive external MOSFETs for higher current and voltage capabilities. The controller is a programmable threshold hysteretic controller, with user-selectable feedback paths that uses the IC in current mode floating load buck, boost, and floating load buck/boost configurations.

4.1 Hysteretic Controllers

The hysteretic controllers provide cycle by cycle switch control with fast transient response which simplifies system design by requiring no external compensation. The hysteretic controllers include the following key features:

- Four independent channels
- DAC configurable thresholds
- Wide switching frequency range from 20 kHz to 2 MHz
- Programmable minimum on and off time
- Floating load buck, boost, and floating load buck-boost topology controller

The PowerPSoC contains four hysteretic controllers. There is one hysteretic controller for each channel of the device. The reference inputs of the hysteretic controller are provided by the reference DACs as illustrated in the top level block diagram on page 2 (see Figure 2-1).

The hysteretic control function output is generated by comparing the feedback value to two thresholds. Going below the lower threshold turns the switch ON and exceeding the upper threshold turns the switch OFF as shown in Figure 4-1 The output current waveforms are shown in Figure 4-2.

Figure 4-1. Generating Hysteretic Control Function Output

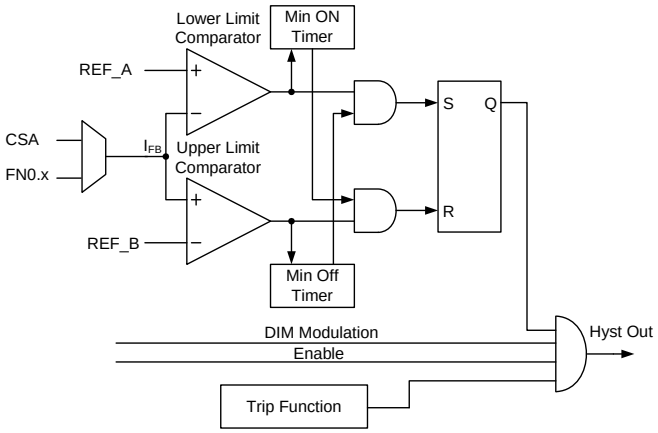
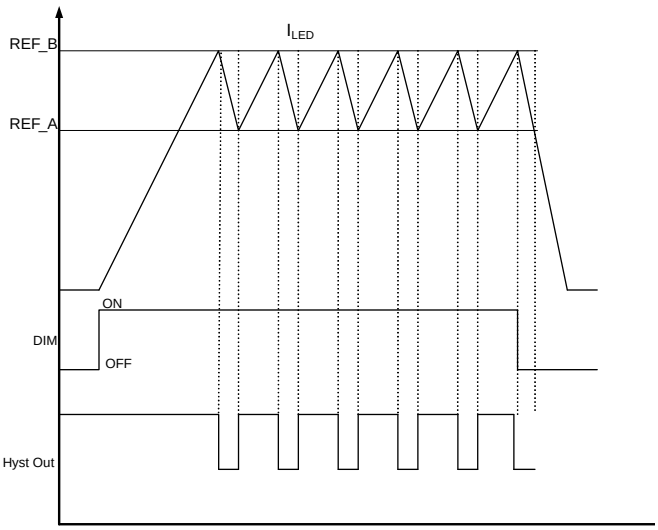


Figure 4-2. Current Waveforms



The minimum on-time and off-time circuits in the PowerPSoC prevent oscillations at very high frequencies, which can be very destructive to output switches.

4.2 Low Side N-Channel FETs

The internal low side N-Channel FETs are designed to enhance system integration. The low side N-Channel FETs include the following key features:

- Drive capability up to 1A
- Switching times of 20 ns (rise and fall times) to ensure high efficiency (more than 90%)
- Drain source voltage rating 32V
- Low $R_{DS(ON)}$ to ensure high efficiency
- Switching frequency up to 2 MHz

4.3 External Gate Drivers

These gate drivers enable the use of external FETs with higher current capabilities or lower $R_{DS(ON)}$. The external gate drivers directly drive MOSFETS that are used in switching applications. The gate driver provides multiple programmable drive strength steps to enable improved EMI management. The external gate drivers include the following key features.

- Programmable drive strength options (25%, 50%, 75%, 100%) for EMI management
- Rise and fall times at 55 ns with 4 nF load

4.4 Dimming Modulation Schemes

There are three dimming modulation schemes available with the PowerPSoC. The configurable modulation schemes are:

- Precise Intensity Signal Modulation (PrISM)
- Delta Sigma Modulation Mode (DMM)
- Pulse Width Modulation (PWM)

4.4.1 PrISM Mode Configuration

- High resolution operation up to 16 bits
- Dedicated PrISM module enables customers to use core PSoC digital blocks for other needs
- Clocking up to 48 MHz
- Selectable output signal density
- Reduced EMI

The PrISM mode compares the output of a pseudo-random counter with a signal density value. The comparator output asserts when the count value is less than or equal to the value in the signal density register.

4.4.2 DMM Mode Configuration

- High resolution operation up to 16 bits
- Configurable output frequency and delta sigma modulator width to trade off repeat rates versus resolution
- Dedicated DMM module enables customers to use PSoC digital blocks for other uses
- Clocking up to 48 MHz

The DMM modulator consists of a 12-bit PWM block and a 4-bit DSM (Delta Sigma Modulator) block. The width of the PWM, the width of the DMM, and the clock defines the output frequency. The duty cycle of the PWM output is dithered by using the DSM block which has a user selectable resolution up to 4 bits.

4.4.3 PWM Mode Configuration

- High resolution operation up to 16 bits
- User programmable period from 1 to 65535 clocks
- Dedicated PWM module enables customers to use core PSoC digital blocks for other use
- Interrupt on rising edge of the output or terminal count
- Precise PWM phase control to manage system current edges
- Phase synchronization among the four channels
- PWM output can be aligned to left, right, or center

The PWM features a down counter and a pulse width register. A comparator output is asserted when the count value is less than or equal to the value in the pulse width register.

4.5 Current Sense Amplifier

Four high side current sense amplifiers provide a differential sense capability to sense the voltage across current sense resistors in lighting systems. The current sense amplifier includes the following key features:

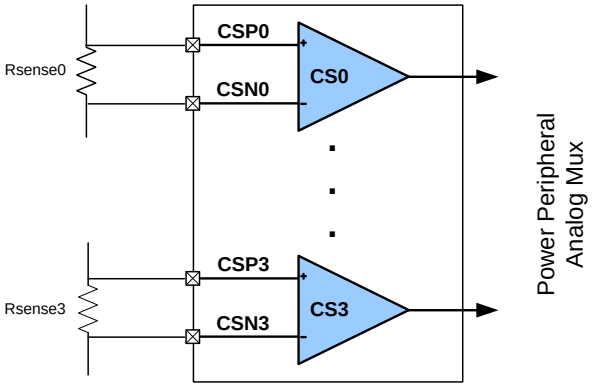
- Operation with high common mode voltage to 32V
- High common mode rejection ratio
- Programmable bandwidth to optimize system noise immunity

An off-chip resistor R_{sense} is used for high side current measurement as shown in Figure 4-3 on page 10. The output of the current sense amplifier goes to the Power Peripherals Analog Multiplexer where the user selects which hysteretic controller to route to. Table 4-1 illustrates example values of R_{sense} for different currents.

Table 4-1. R_{sense} Values for Different Currents

Max Load Current (mA)	Typical R_{sense} (mΩ)
1000	100
750	130
500	200
350	300

Figure 4-3. High Side Current Measurement



4.6 Voltage Comparators

There are six comparators that provide high speed comparator operation for over voltage, over current, and various other system event detections. For example, the comparators may be used for zero crossing detection for an AC input line or monitoring total DC bus current. Programmable internal analog routing enables these comparators to monitor various analog signals. These comparators include the following key features:

- High speed comparator operation: 100 ns response time
- Programmable interrupt generation
- Low input offset voltage and input bias currents

Six precision voltage comparators are available. The differential positive and negative inputs of the comparators are routed from the analog multiplexer and the output goes to the digital multiplexer. A programmable inverter is used to select the output polarity. User selectable hysteresis can be enabled or disabled to trade-off noise immunity versus comparator sensitivity.

4.7 Reference DACs

The reference DACs are used to generate set points for various analog modules such as Hysteretic controllers and comparators. The reference DACs include the following key features:

- 8-bit resolution
- Guaranteed monotonic operation
- Low gain errors
- 10 us settling time

These DACs are available to provide programmable references for the various analog and comparator functions and are controlled by memory mapped registers.

DAC[0:7] are embedded in the hysteretic controllers and are required to set the upper and lower thresholds for channel 0 to 3.

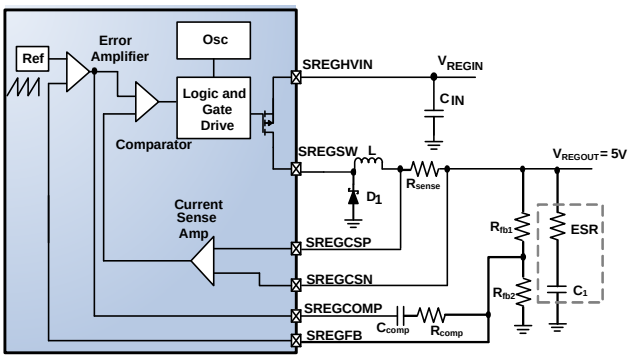
DAC [8:13] are connected to the Power Peripherals Analog Multiplexer and provide programmable references to the comparator bank. These are used to set trip points which enable over voltage, over current, and other system event detection.

4.8 Built-in Switching Regulator

The switching regulator is used to power the low voltage (5V portion of the PowerPSoC) from the input line. This regulator is based upon a peak current control loop which can support up to 250 mA of output current. The current not being consumed by PowerPSoC is used to power additional system peripherals. The key features of the built-in switching regulator include:

- Ability to self power device from input line
- Small filter component sizes
- Fast response to transients

Figure 4-4. Built-in Switching Regulator



4.9 Analog Multiplexer

The analog multiplexer is used to multiplex signals between the power peripheral blocks. The CPU configures the Power Peripherals Analog Multiplexer connections using memory mapped registers. The analog multiplexer includes the following key features:

- Connect signals to ensure needed flexibility
- Ensure signal integrity for minimum signal corruption
- Configurability through Cypress PSoC Designer 5.0

4.10 Digital Multiplexer

The digital multiplexer is used to multiplex signals between the power peripheral blocks.The Power Peripherals Digital Multiplexer is a configurable switching matrix that connects the power peripheral digital resources. This Power Peripheral Digital Multiplexer is independent of the main PSoC digital buses or global interconnect of the PSoC core. The digital multiplexer includes the following key features:

- Connect signals to ensure needed flexibility
- Configurability through Cypress PSoC Designer 5.0

4.11 Function Pins (FN0[0:3])

The function I/O pins are a set of dedicated control pins used to perform system level functions with the power peripheral blocks of the PowerPSoC. These pins are dynamically configurable, enabling them to perform a multitude of input and output functions. These I/Os have direct access to the input and output of the voltage comparators, input of the hysteretic controller, and output of the digital PWM blocks for the device. The function I/O pins are register mapped. The microcontroller can control and read the state of these pins and the interrupt function.

Some of the key system benefits of the function I/O are:

- Enabling higher voltage current-sense amplifier as shown in Figure 4-5
- Synchronizing dimming of multiple PowerPSoC controllers as shown in Figure 4-6
- Programmable fail-safe monitor and dedicated shutdown of hysteretic controller as shown in Figure 4-7

Along with the above functionality, these I/Os also provide interrupt functionality enabling intelligent system responses to power control lighting system status.

Figure 4-5. External CSA and FET Application

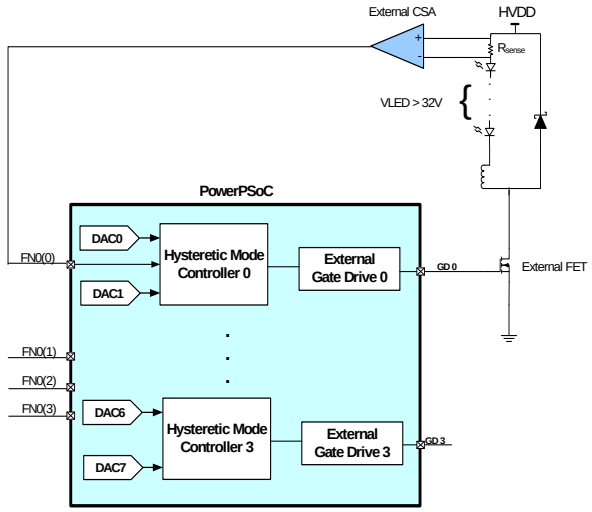


Figure 4-6. PowerPSoC in Master/Slave Configuration

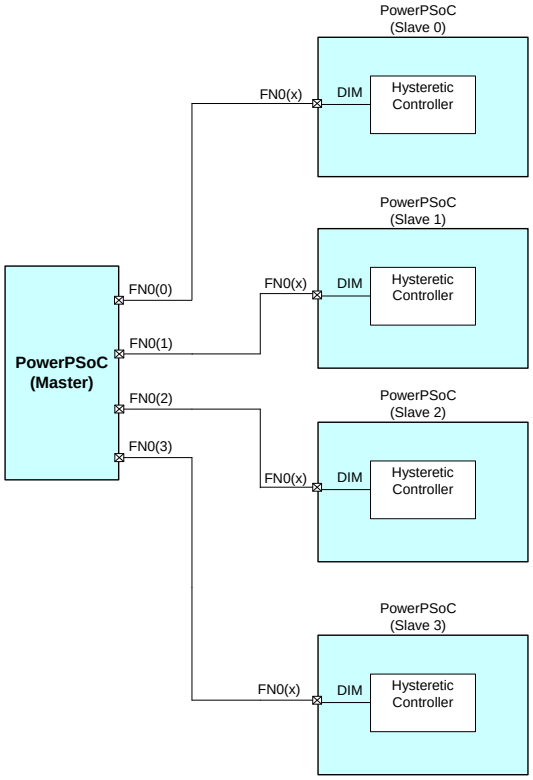
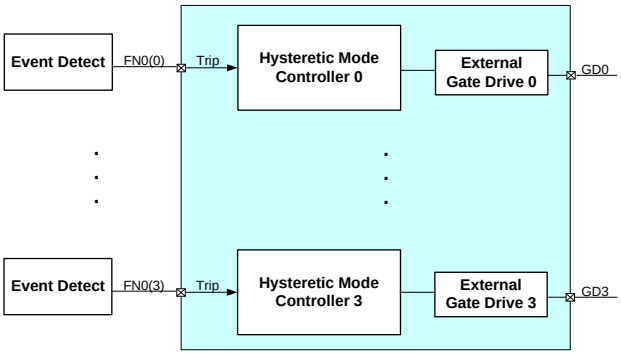


Figure 4-7. Event Detection



5. The PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors to simplify programming of real time embedded events. The program execution is timed and protected using the included Sleep and Watchdog Timers (WDT) time and protect program execution.

Memory encompasses 16K of Flash for program storage, 1K of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 4 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PowerPSoC device.

PowerPSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

5.1 The Digital System

The digital system contains eight digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

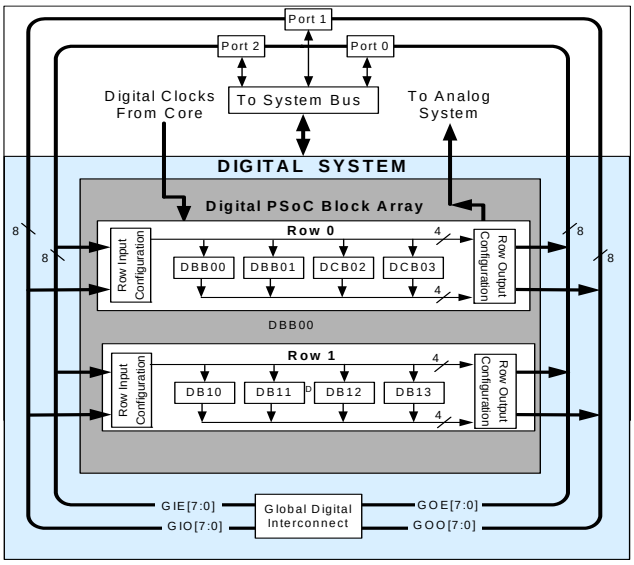
Digital peripheral configurations include those listed below.

- DALI
- DMX512
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I2C slave and multi-master
- Cyclical redundancy checker/generator (8 to 32 bit)
- IrDA
- Pseudo random sequence generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

There are four digital blocks in each row. This allows optimum choice of system resources for your application.

Figure 5-1. Digital System Block Diagram



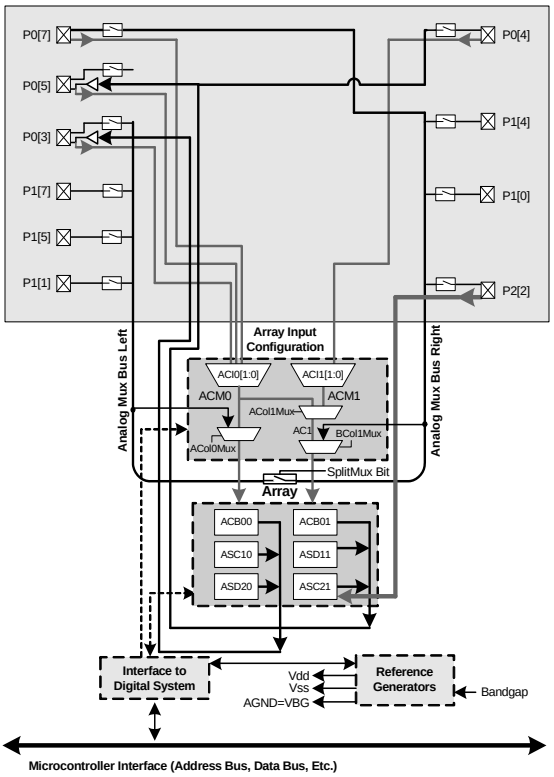
5.2 The Analog System

The analog system contains six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PowerPSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 2, with 6 to 12-bit resolution, selectable as incremental, Delta Sigma, and SAR)
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to 2, with 16 selectable thresholds)
- DACs (up to 2, with 6 to 9-bit resolution)
- Multiplying DACs (up to 2, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3V reference (as a system resource)
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in Figure 5-2 on page 13.

Figure 5-2. Analog System Block Diagram



5.3 The Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin in ports 0 to 2. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Crosspoint connection between any I/O pin combinations

When designing capacitive sensing applications, refer to the latest signal-to-noise signal level requirements application notes, found at http://www.cypress.com > Design Resources > Application Notes. In general, and unless otherwise noted in the relevant application notes, the minimum signal-to-noise ratio (SNR) for CapSense applications is 5:1.

5.4 Additional System Resources

System resources provide additional capability useful in complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- A decimator provides a custom hardware filter for digital signal processing applications including creation of Delta Sigma ADCs.
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. The designer can generate additional clocks using digital PSoC blocks as clock dividers.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master applications are supported.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

6. Applications

The following figures show examples of applications in which the PowerPSoC family of devices adds intelligent power control for power applications.

Figure 6-1. LED Lighting with RGGB Color Mixing Configured as Floating Load Buck Converter

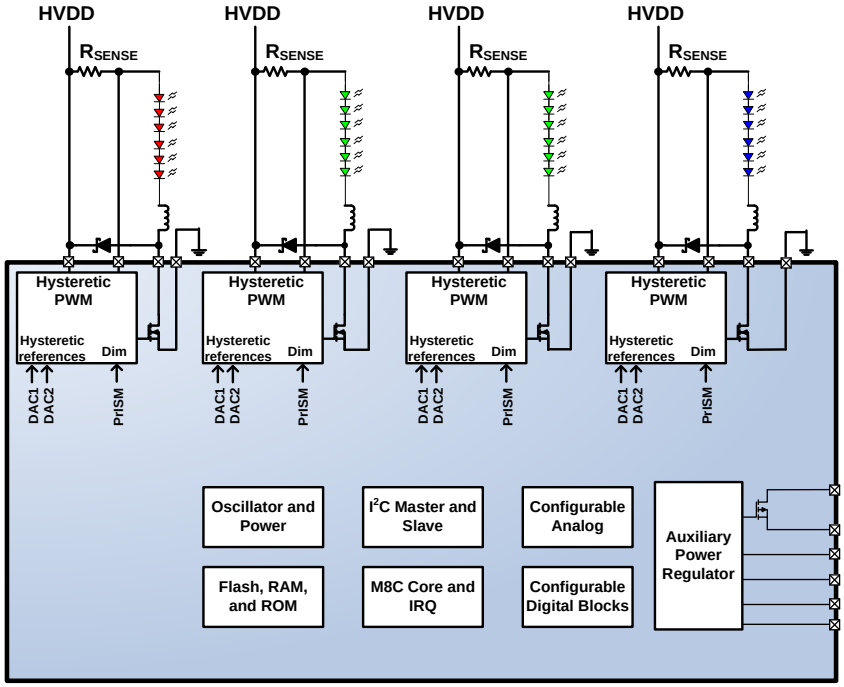


Figure 6-2. LED Lighting with RGBA Color Mixing Driving External MOSFETS as Floating Load Buck Converter

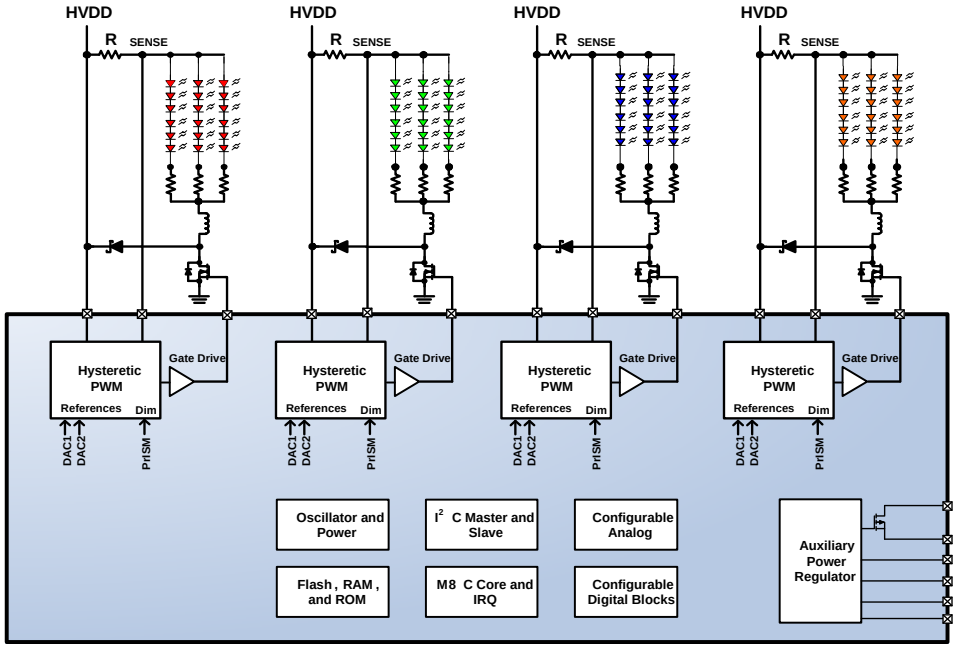
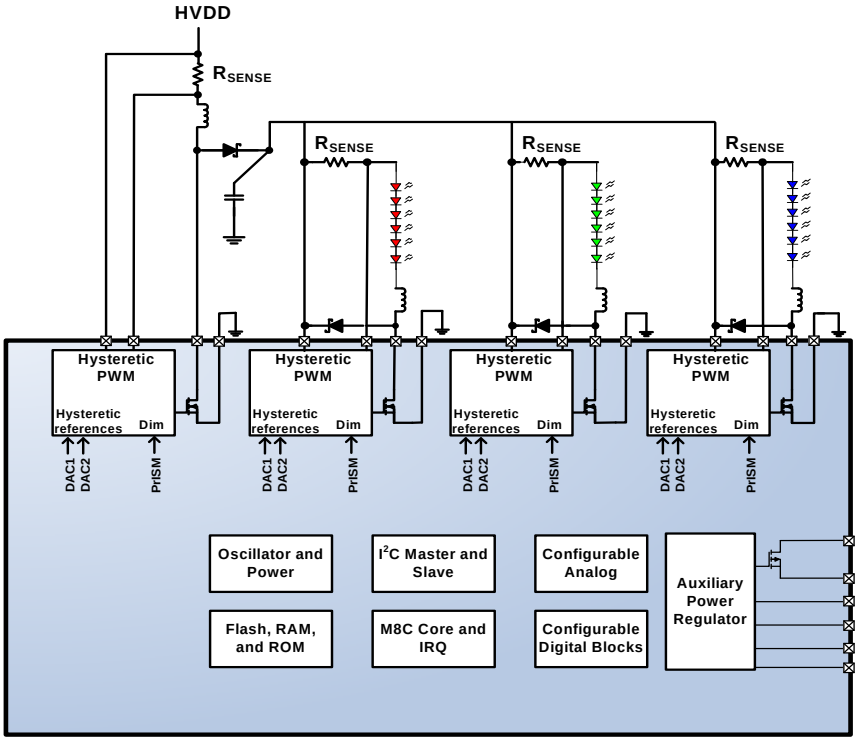


Figure 6-3. LED Lighting with a Single Channel Boost Driving Three Floating Load Buck Channels



7. PowerPSoC Device Characteristics

There are two major groups of devices in the PowerPSoC family. One group is a 4-channel 56-pin QFN and the other is a 3-channel 56-pin QFN. These are summarized in the following table.

Table 7-1. PowerPSoC Device Characteristics

Device Group	Internal Power FETs	External Gate Drivers	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Col-umns	Analog Blocks	SRAM Size	Flash Size
CY8CLED04D01-56LTXI	4X1.0A	4	14	2	8	14	2	2	6	1K	16K
CY8CLED04D02-56LTXI	4X0.5A	4	14	2	8	14	2	2	6	1K	16K
CY8CLED04G01-56LTXI	0	4	14	2	8	14	2	2	6	1K	16K
CY8CLED03D01-56LTXI	3X1.0A	3	14	2	8	14	2	2	6	1K	16K
CY8CLED03D02-56LTXI	3X0.5A	3	14	2	8	14	2	2	6	1K	16K
CY8CLED03G01-56LTXI	0	3	14	2	8	14	2	2	6	1K	16K
CY8CLED02D01-56LTXI	2X1.0A	2	14	2	8	14	2	2	6	1K	16K
CY8CLED01D01-56LTXI	1X1.0A	1	14	2	8	14	2	2	6	1K	16K

8. Getting Started

The quickest way to understand the PowerPSoC device is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PowerPSoC integrated circuit and presents specific pin, register, and electrical specifications. For in depth information, along with detailed programming information, refer to the *PowerPSoC Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PowerPSoC device data sheets on the web at www.cypress.com.

8.1 Application Notes

Application notes are an excellent introduction to a wide variety of possible PowerPSoC designs. Layout Guidelines, Thermal Management and Firmware Design Guidelines are some of the topics covered. To view the PowerPSoC application notes, go to http://www.cypress.com.

8.2 Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PowerPSoC development. Go to the Cypress Online Store web

site at http://www.cypress.com, click the Online Store shopping cart icon, and click *PowerPSoC (Power Programmable System-on-Chip)* to view a current list of available items.

8.3 Training

Free PowerPSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

8.4 CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PowerPSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

8.5 Technical Support

PowerPSoC application engineers take pride in fast and accurate response. They can be reached with a 24-hour guaranteed response at http://www.cypress.com/support/. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

9. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PowerPSoC family.

9.1 PSoC Designer Software Subsystems

9.1.1 System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PowerPSoC Intelligent LED Drivers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PowerPSoC device.

9.1.2 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PowerPSoC blocks. Examples of user modules are Current Sense Amplifiers, PrISM, PWM, DMM, Floating Load Buck, and Boost. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

9.1.3 Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

9.1.4 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PowerPSoC family of devices. The products allow you to create complete C programs for the PowerPSoC family of devices.

The optimizing C compilers provide all the features of C tailored to the PowerPSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

9.1.5 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PowerPSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

9.1.6 Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

9.2 In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PowerPSoC devices.

10. Designing with User Modules

The development process for the PowerPSoC device differs from that of a traditional fixed function microprocessor. The configurable power, analog, and digital hardware blocks give the PowerPSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PowerPSoC Blocks, have the ability to implement a wide variety of user selectable functions. The PowerPSOC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify and Debug

Select Components. In the chip-level view the components are called “user modules”. User modules make selecting and implementing peripheral devices simple and come in power, analog, digital, and mixed signal varieties. The standard user module library contains over 50 common peripherals such as Current Sense Amplifiers, PrISM, PWM, DMM, Floating Buck, Boost, ADCs, DACs, Timers, Counters, UARTs, and other not so common peripherals such as DTMF generators and Bi-Quad analog filter sections.

Configure Components. Each of the components selected establishes the basic register settings that implement the selected function. They also provide parameters allowing precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

The chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter and other information needed to successfully implement your design.

Organize and Connect. Signal chains can be built at the chip level by interconnecting user modules to each other and the IO pins. In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug. When ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high level user module API functions.

The chip-level designs generate software based on your design. The chip-level view provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows development and customization of your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

11. Document Conventions

11.1 Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	Alternating Current
ADC	Analog-to-Digital Converter
API	Application Programming Interface
CPU	Central Processing Unit
CSA	Current Sense Amplifier
CT	Continuous Time
DAC	Digital-to-Analog Converter
DALI	Digital Addressable Lighting Interface
DC	Direct Current
DMM	Delta Sigma Modulation Mode
DMX	Digital Multiplexing
DSM	Delta Sigma Modulator
DTMF	Dual-Tone Multi Frequency
ECO	External Crystal Oscillator
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
FAQ	Frequently Asked Questions
FET	Field Effect Transistor
FSR	Full Scale Range
GPIO	General Purpose IO
GUI	Graphical User Interface
HBM	Human Body Model
IC	Integrated Circuit
ICE	In-Circuit Emulator
IDE	Integrated Development Environment
ILO	Internal Low-speed Oscillator
IMO	Internal Main Oscillator
ISSP	In-System Serial Programming
I/O	Input/Output
IPOR	Imprecise Power On Reset
LED	Light Emitting Diode

Acronym	Description
LSB	Least-Significant bit
LVD	Low Voltage Detect
MCU	Microcontroller
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MSB	Most-Significant bit
OCD	On Chip Debugger
PC	Program Counter
POR	Power On Reset
PPOR	Precision Power On Reset
PowerPSoC	Power Programmable System-on-Chip™
PrISM	Precise Intensity Signal Modulation
PSoC	Programmable System-on-Chip™
PWM	Pulse Width Modulator
QFN	Quad Flat no leads Package
RGBA	Red, Green, Blue, Amber
RGGB	Red, Green, Green, Blue
SC	Switched Capacitor
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TRM	Technical Reference Manual
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watch Dog Timer

11.2 Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 14-1 on page 29 lists all the abbreviations used to measure the PowerPSoC devices.

11.3 Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.

12. Pin Information

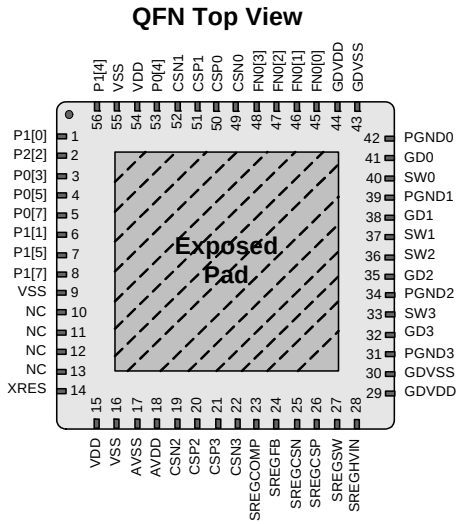
12.1 CY8CLED04D0x 56-Pin Part Pinout (without OCD)

The CY8CLED04D01 and CY8CLED04D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-1. CY8CLED04D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (secondary), ISSP primary
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Ainput(col0) Aoutput (col0)
4	I/O	I/O		P0[5]	GPIO/Ainput(col0) Aoutput (col1) Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Connects to Analog Column Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (secondary) ISSP primary
7	I/O	I		P1[5]	GPIO/I2C SDATA (Primary)
8	I/O	I		P1[7]	GPIO/ I2C SCLK (Primary)
9				VSS	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				VDD	Digital Power Supply
16				VSS	Digital Ground
17				AVSS	Analog Ground
18				AVDD	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDVDD	Gate Driver Power Supply
30				GDVSS	Gate Driver Ground
31				PGND3	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				SW3	Power Switch 3
34				PGND2	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0	Power FETGround 0
43				GDVSS	Gate Driver Ground

Figure 12-1. CY8CLED04D0x 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

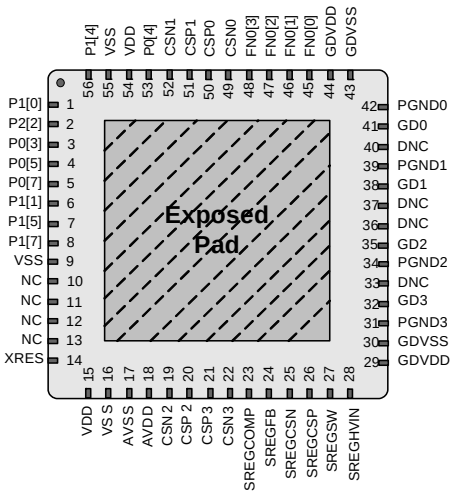
12.2 CY8CLED04G01 56-Pin Part Pinout (without OCD)

The CY8CLED04G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-2. CY8CLED04G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (secondary), ISSP primary
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Ainput(col0) Aoutput (col0)
4	I/O	I/O		P0[5]	GPIO/Ainput(col0) Aoutput (col1) Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Connects to Analog Column Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (secondary) ISSP primary
7	I/O	I		P1[5]	GPIO/I2C SDATA (Primary)
8	I/O	I		P1[7]	GPIO/ I2C SCLK (Primary)
9				VSS	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				VDD	Digital Power Supply
16				VSS	Digital Ground
17				AVSS	Analog Ground
18				AVDD	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDVDD	Gate Driver Power Supply
30				GDVSS	Gate Driver Ground
31				PGND3	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				DNC[1]	Do Not Connect
34				PGND2	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[1]	Do Not Connect
37				DNC[1]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1	Power FET Ground 1
40				DNC[1]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0	Power FET Ground 0
43				GDVSS	Gate Driver Ground

Figure 12-2. CY8CLED04G01 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDVDD	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Connects to Analog Column (1), connects to bandgap output
54				VDD	Digital Power Supply
55				VSS	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

12.3 CY8CLED04DOCD1 56-Pin Part Pinout (with OCD)

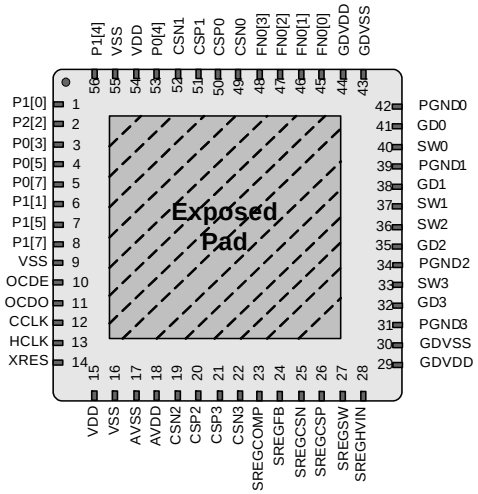
The CY8CLED04DOCD1 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-3. CY8CLED04DOCD1 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDATA (secondary) ISSP primary
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Ainput (coIO) Aoutput (coIO)
4	I/O	I/O		P0[5]	GPIO/Ainput (coIO) Aoutput (coIO) / Capsense Ref Cap
5	I/O	I		P0[7]	GPIO, connects to Analog Column Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (secondary) ISSP primary
7	I/O	I		P1[5]	GPIO/I2C SDATA (Primary)
8	I/O	I		P1[7]	GPIO/ I2C SCLK (Primary)
9				VSS	Digital Ground
10	I/O			OCDE	On Chip Debugger Port
11	I/O			OCDO	On Chip Debugger Port
12	I/O			CCLK	On Chip Debugger Port
13	I/O			HCLK	On Chip Debugger Port
14	I			XRES	External Reset
15				VDD	Digital Power Supply
16				VSS	Digital Ground
17				AVSS	Analog Ground
18				AVDD	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				CSP3	Current Sense Positive Input and Power Supply - CSA3
22			I	CSN3	Current Sense Negative Input 3
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDVDD	Gate Driver Power Supply
30				GDVSS	Gate Driver Ground
31				PGND3	Power FET Ground 3
32			O	GD3	External Low Side Gate Driver 3
33				SW3	Power Switch 3
34				PGND2	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0	Power FET Ground 0
43				GDVSS	Gate Driver Ground

Figure 12-3. CY8CLED04DOCD1 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDVDD	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Connects to Analog Column (1), bandgap output
54				VDD	Digital Power Supply
55				VSS	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

12.4 CY8CLED03D0x 56-Pin Part Pinout (without OCD)

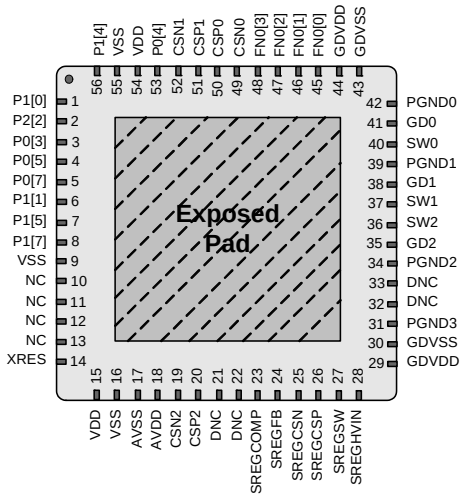
The CY8CLED03D01 and CY8CLED03D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-4. CY8CLED03D0x 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/ I2C SDA (secondary), ISSP primary
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Ainput(coI0) Aoutput (coI0)
4	I/O	I/O		P0[5]	GPIO/Ainput(coI0) Aoutput (coI1) Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Connects to Analog Column Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (secondary) ISSP primary
7	I/O	I		P1[5]	GPIO/I2C SDATA (Primary)
8	I/O	I		P1[7]	GPIO/ I2C SCLK (Primary)
9				VSS	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				VDD	Digital Power Supply
16				VSS	Digital Ground
17				AVSS	Analog Ground
18				AVDD	Analog Power Supply
19			I	CSN2	Current Sense Negative Input - CSA2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[1]	Do Not Connect
22				DNC[1]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDVDD	Gate Driver Power Supply
30				GDVSS	Gate Driver Ground
31				PGND3	Power FET Ground 3
32				DNC[1]	Do Not Connect
33				DNC[1]	Do Not Connect
34				PGND2	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				SW2	Power Switch 2
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0	Power FETGround 0
43				GDVSS	Gate Driver Ground
44				GDVDD	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Connects to Analog Column (1), connects to bandgap output
54				VDD	Digital Power Supply
55				VSS	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-4. CY8CLED03D0x 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

12.5 CY8CLED03G01 56-Pin Part Pinout (without OCD)

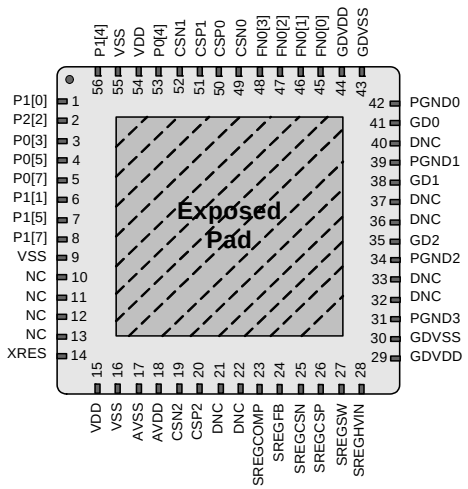
The CY8CLED03G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-5. CY8CLED03G01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (secondary), ISSP primary
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Ainput(col0) Aoutput (col0)
4	I/O	I/O		P0[5]	GPIO/Ainput(col0) Aoutput (col1) Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Connects to Analog Column Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (secondary) ISSP primary
7	I/O	I		P1[5]	GPIO/I2C SDATA (Primary)
8	I/O	I		P1[7]	GPIO/ I2C SCLK (Primary)
9				VSS	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				VDD	Digital Power Supply
16				VSS	Digital Ground
17				AVSS	Analog Ground
18				AVDD	Analog Power Supply
19			I	CSN2	Current Sense Negative Input 2
20				CSP2	Current Sense Positive Input and Power Supply - CSA2
21				DNC[1]	Do Not Connect
22				DNC[1]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDVDD	Gate Driver Power Supply
30				GDVSS	Gate Driver Ground
31				PGND3	Power FET Ground 3
32				DNC[1]	Do Not Connect
33				DNC[1]	Do Not Connect
34				PGND2	Power FET Ground 2
35			O	GD2	External Low Side Gate Driver 2
36				DNC[1]	Do Not Connect
37				DNC[1]	Do Not Connect
38			O	GD1	External Low Side Gate Driver 1
39				PGND1	Power FET Ground 1
40				DNC[1]	Do Not Connect
41			O	GD0	External Low Side Gate Driver 0
42				PGND0	Power FET Ground 0
43				GDVSS	Gate Driver Ground

Figure 12-5. CY8CLED03G01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDVDD	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Connects to Analog Column (1), connects to bandgap output
54				VDD	Digital Power Supply
55				VSS	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

12.6 CY8CLED02D01 56-Pin Part Pinout (without OCD)

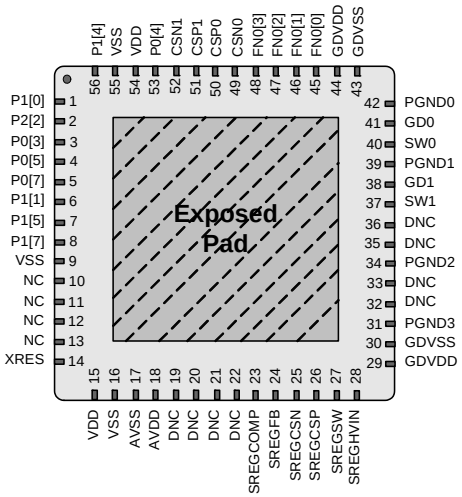
The CY8CLED02D01 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-6. CY8CLED02D01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/ I2C SDA (secondary), ISSP primary
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Ainput(coI0) Aoutput (coI0)
4	I/O	I/O		P0[5]	GPIO/Ainput(coI0) Aoutput (coI1) Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Connects to Analog Column Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (secondary) ISSP primary
7	I/O	I		P1[5]	GPIO/I2C SDATA (Primary)
8	I/O	I		P1[7]	GPIO/ I2C SCLK (Primary)
9				VSS	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				VDD	Digital Power Supply
16				VSS	Digital Ground
17				AVSS	Analog Ground
18				AVDD	Analog Power Supply
19				DNC[1]	Do Not Connect
20				DNC[1]	Do Not Connect
21				DNC[1]	Do Not Connect
22				DNC[1]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDVDD	Gate Driver Power Supply
30				GDVSS	Gate Driver Ground
31				PGND3	Power FET Ground 3
32				DNC[1]	Do Not Connect
33				DNC[1]	Do Not Connect
34				PGND2	Power FET Ground 2
35				DNC[1]	Do Not Connect
36				DNC[1]	Do Not Connect
37				SW1	Power Switch 1
38			O	GD1	External Low Side Gate Driver 1
39				PGND1	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0	Power FETGround 0
43				GDVSS	Gate Driver Ground
44				GDVDD	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				CSP1	Current Sense Positive Input and Power Supply - CSA1
52			I	CSN1	Current Sense Negative Input 1
53	I/O	I		P0[4]	GPIO/Connects to Analog Column (1), connects to bandgap output
54				VDD	Digital Power Supply
55				VSS	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Figure 12-6. CY8CLED02D01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

12.7 CY8CLED01D01 56-Pin Part Pinout (without OCD)

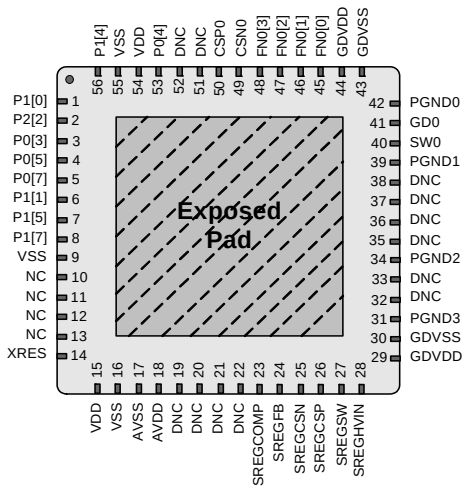
The CY8CLED01D01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-7. CY8CLED01D01 56-Pin Part Pinout (QFN)

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
1	I/O	I		P1[0]	GPIO/I2C SDA (secondary), ISSP primary
2	I/O	I		P2[2]	GPIO/Direct Switch Cap connection
3	I/O	I/O		P0[3]	GPIO/Ainput(col0) Aoutput (col0)
4	I/O	I/O		P0[5]	GPIO/Ainput(col0) Aoutput (col1) Capsense Ref Cap
5	I/O	I		P0[7]	GPIO/Connects to Analog Column Capsense Ref Cap
6	I/O	I		P1[1]	GPIO/I2C SCLK (secondary) ISSP primary
7	I/O	I		P1[5]	GPIO/I2C SDATA (Primary)
8	I/O	I		P1[7]	GPIO/ I2C SCLK (Primary)
9				VSS	Digital Ground
10				NC	No Connect
11				NC	No Connect
12				NC	No Connect
13				NC	No Connect
14	I			XRES	External Reset
15				VDD	Digital Power Supply
16				VSS	Digital Ground
17				AVSS	Analog Ground
18				AVDD	Analog Power Supply
19				DNC[1]	Do Not Connect
20				DNC[1]	Do Not Connect
21				DNC[1]	Do Not Connect
22				DNC[1]	Do Not Connect
23				SREGCOMP	Voltage Regulator Error Amp Comp
24			I	SREGFB	Regulator Voltage Mode Feedback Node
25			I	SREGCSN	Current Mode Feedback Negative
26			I	SREGCSP	Current Mode Feedback Positive
27			O	SREGSW	Switch Mode Regulator OUT
28				SREGHVIN	Switch Mode Regulator IN
29				GDVDD	Gate Driver Power Supply
30				GDVSS	Gate Driver Ground
31				PGND3	Power FET Ground 3
32				DNC[1]	Do Not Connect
33				DNC[1]	Do Not Connect
34				PGND2	Power FET Ground 2
35				DNC[1]	Do Not Connect
36				DNC[1]	Do Not Connect
37				DNC[1]	Do Not Connect
38				DNC[1]	Do Not Connect
39				PGND1	Power FET Ground 1
40				SW0	Power Switch 0
41			O	GD0	External Low Side Gate Driver 0
42				PGND0	Power FET Ground 0
43				GDVSS	Gate Driver Ground

Figure 12-7. CY8CLED01D01 56-Pin PowerPSoC Device

QFN Top View



*** Connect Exposed Pad to PGNDx**

Pin No.	Type			Name	Description
	Digital Rows	Analog Columns	Power Peripherals		
44				GDVDD	Gate Driver Power Supply
45			I/O	FN0[0]	Function I/O
46			I/O	FN0[1]	Function I/O
47			I/O	FN0[2]	Function I/O
48			I/O	FN0[3]	Function I/O
49			I	CSN0	Current Sense Negative Input 0
50				CSP0	Current Sense Positive Input and Power Supply - CSA0
51				DNC[1]	Do Not Connect
52				DNC[1]	Do Not Connect
53	I/O	I		P0[4]	GPIO/Connects to Analog Column (1), connects to bandgap output
54				VDD	Digital Power Supply
55				VSS	Digital Ground
56	I/O	I		P1[4]	GPIO / External Clock Input

Note
1. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.

13. Register General Conventions

13.1 Abbreviations Used

The register conventions specific to this section are listed in Table 13-1.

Table 13-1. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

13.2 Register Naming Conventions

The register naming convention specific to the PSoC core section of PowerPSoC blocks and their registers is:

<Prefix>mn<Suffix>
where m = row index, n = column index

Therefore, ASD13CR3 is a register for an analog PowerPSoC block in row 1 column 3.

The register naming convention specific to the power peripheral section of PowerPSoC blocks and their registers is:

<Prefix>x<Suffix>
where x = number of channel

Therefore, CSA0_CR is a register for a power peripheral PowerPSoC block in for Current Sense Amplifier, channel 0.

13.3 Register Mapping Tables

The PowerPSoC device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

More detailed description of the Registers are found in the PowerPSoC TRM.

13.4 Register Map Bank 0 Table

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DPWM0PCF	40	RW	ASC10CR0	80	RW	VDAC0_CR	C0	RW
PRT0IE	01	RW	DPWM0PDH	41	RW	ASC10CR1	81	RW	VDAC0_DR0	C1	RW
PRT0GS	02	RW	DPWM0PDL	42	RW	ASC10CR2	82	RW	VDAC0_DR1	C2	RW
PRT0DM2	03	RW	DPWM0PWH	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	DPWM0PWL	44	RW	ASD11CR0	84	RW	VDAC1_CR	C4	RW
PRT1IE	05	RW	DPWM0PCH	45	RW	ASD11CR1	85	RW	VDAC1_DR0	C5	RW
PRT1GS	06	RW	DPWM0PCL	46	RW	ASD11CR2	86	RW	VDAC1_DR1	C6	RW
PRT1DM2	07	RW	DPWM0GCFG	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DPWM1PCF	48	RW		88		VDAC2_CR	C8	RW
PRT2IE	09	RW	DPWM1PDH	49	RW		89		VDAC2_DR0	C9	RW
PRT2GS	0A	RW	DPWM1PDL	4A	RW		8A		VDAC2_DR1	CA	RW
PRT2DM2	0B	RW	DPWM1PWH	4B	RW		8B			CB	
FN0DR	0C	RW	DPWM1PWL	4C	RW		8C		VDAC3_CR	CC	RW
FN0IE	0D	RW	DPWM1PCH	4D	RW		8D		VDAC3_DR0	CD	RW
FN0GS	0E	RW	DPWM1PCL	4E	RW		8E		VDAC3_DR1	CE	RW
FN0DM2	0F	RW	DPWM1GCFG	4F	RW		8F			CF	
	10		DPWM2PCF	50	RW	ASD20CR0	90	RW	CUR_PP	D0	RW
	11		DPWM2PDH	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
	12		DPWM2PDL	52	RW	ASD20CR2	92	RW		D2	
	13		DPWM2PWH	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
	14		DPWM2PWL	54	RW	ASC21CR0	94	RW	MVR_PP	D4	RW
	15		DPWM2PCH	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
	16		DPWM2PCL	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
	17		DPWM2GCFG	57	RW	ASC21CR3	97	RW	I2C_SCR	D7	#
PDMUX_S1	18	RW	DPWM3PCF	58	RW		98		I2C_DR	D8	RW
PDMUX_S2	19	RW	DPWM3PDH	59	RW		99		I2C_MSCR	D9	#
PDMUX_S3	1A	RW	DPWM3PDL	5A	RW		9A		INT_CLR0	DA	RW
PDMUX_S4	1B	RW	DPWM3PWH	5B	RW		9B		INT_CLR1	DB	RW
PDMUX_S5	1C	RW	DPWM3PWL	5C	RW	VDAC6_CR	9C	RW	INT_CLR2	DC	RW
PDMUX_S6	1D	RW	DPWM3PCH	5D	RW	VDAC6_DR0	9D	RW	INT_CLR3	DD	RW
	1E		DPWM3PCL	5E	RW	VDAC6_DR1	9E	RW	INT_MSK3	DE	RW
CHBOND_CR	1F	RW	DPWM3GCFG	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW	VDAC4_CR	A0	RW	INT_MSK0	E0	RW
DBB00DR1	21	W	AMUX_CFG	61	RW	VDAC4_DR0	A1	RW	INT_MSK1	E1	RW
DBB00DR2	22	RW		62		VDAC4_DR1	A2	RW	INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#	VDAC5_CR	A4	RW	DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#	VDAC5_DR0	A5	RW	DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW	VDAC5_DR1	A6	RW	DEC_CR0	E6	RW
DBB01CR0	27	#	PAMUX_S1	67	RW		A7		DEC_CR1	E7	RW
DCB02DR0	28	#	PAMUX_S2	68	RW	MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W	PAMUX_S3	69	RW	MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW	PAMUX_S4	6A	RW	MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	DPWM0PCFG	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	DPWM1PCFG	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	DPWM2PCFG	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	DPWM3PCFG	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	DPWMINTFLG	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	DPWMINTMSK	7D	RW	RDI1RO0	BD	RW	DAC_D	FD	RW
DCB13DR2	3E	RW	DPWMSYNC	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#		7F			BF		CPU_SCR0	FF	#

13.5 Register Map Bank 1 Table: User Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	CSA0_CR	40	RW	ASC10CR0	80	RW	CMPCH0_CR	C0	RW
PRT0DM1	01	RW		41		ASC10CR1	81	RW	CMPCH2_CR	C1	RW
PRT0IC0	02	RW		42		ASC10CR2	82	RW	CMPCH4_CR	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	CMPCH6_CR	C3	RW
PRT1DM0	04	RW	CSA1_CR	44	RW	ASD11CR0	84	RW	CMPBNK8_CR	C4	RW
PRT1DM1	05	RW		45		ASD11CR1	85	RW	CMPBNK9_CR	C5	RW
PRT1IC0	06	RW		46		ASD11CR2	86	RW	CMPBNK10_CR	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW	CMPBNK11_CR	C7	RW
PRT2DM0	08	RW	CSA2_CR	48	RW		88		CMPBNK12_CR	C8	RW
PRT2DM1	09	RW		49			89		CMPBNK13_CR	C9	RW
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
FN0DM0	0C	RW	CSA3_CR	4C	RW		8C			CC	
FN0DM1	0D	RW		4D			8D			CD	
FN0IC0	0E	RW		4E			8E			CE	
FN0IC1	0F	RW		4F			8F			CF	
	10			50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
	11			51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
	12			52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
	13			53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
	14			54		ASC21CR0	94	RW	HYSCTLR0CR	D4	RW
	15			55		ASC21CR1	95	RW	HYSCTLR1CR	D5	RW
	16			56		ASC21CR2	96	RW	HYSCTLR2CR	D6	RW
	17			57		ASC21CR3	97	RW	HYSCTLR3CR	D7	RW
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B			DB	
	1C			5C			9C		SREG_TST	DC	RW
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7		DEC_CR2	E7	RW
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	RW
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	RW
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB			EB	
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW	AMUX_CLK	AF	RW		EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB01IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB01OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW		78		RDI1RI	B8	RW		F8	
DCB12IN	39	RW	GDRV0_CR	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW		7A		RDI1IS	BA	RW		FA	
	3B		GDRV1_CR	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW		7C		RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	GDRV2_CR	7D	RW	RDI1RO0	BD	RW	DAC_CR	FD	RW
DCB13OU	3E	RW		7E		RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		GDRV3_CR	7F	RW		BF		CPU_SCR0	FF	#

14. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 of the PowerPSoC device family. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc. Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 115°C, except where noted. Table 14-1 lists the units of measure that are used in this section.

Table 14-1. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	Kbit	1024 bits	mA	milliampere
dB	decibels	KHz	kilohertz	ms	millisecond
Hz	Hertz	KΩ	kilohms	mV	millivolts
pp	peak-to-peak	MHz	megahertz	mW	milliwatts
σ	sigma:one standard deviation	MΩ	megaohms	nA	nanoamperes
V	volts	µA	microamperes	ns	nanoseconds
Ω	ohms	µF	microfarads	nV	nanovolts
KB	1024 bytes	µH	microhenrys	pA	picoamperes
ppm	parts per million	µs	microseconds	pF	picofarads
sps	samples per second	µV	microvolts	ps	picoseconds
W	watts	µVrms	microvolts root-mean-square	fF	femtofarads
A	amperes	µW	microwatts		

14.1 Absolute Maximum Ratings

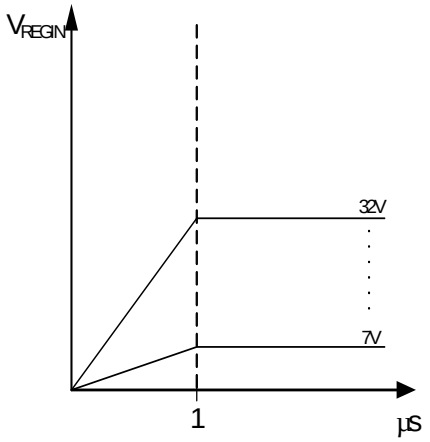
Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested.

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	–	+115	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is 0°C to 50°C.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	T_J ≤ 115°C
VDD, AVDD, GDVDD	Supply Voltage on VDD, AVDD, GDVDD	-0.5	–	+6.0	V	Relative to VSS, AVSS, and GDVSS respectively
V_{IO}	DC Input Voltage	VSS - 0.5	–	VDD + 0.5	V	Applies only to GPIO and FN0 pins
V_{IO2}	DC Voltage Applied to Tri-state	VSS - 0.5	–	VDD + 0.5	V	
V_{FET}	Maximum Voltage from Power Switch (SWx) to Power FET Ground (PGNDx)	–	–	36 [2]	V	PGNDx is connected to GDVSS
V_{CSP},V_{CSN}	Maximum Voltage applied to CSA pins	-0.5	–	36 [2]	V	
V_{SENSE}	Maximum Input Differential Voltage across CSA input	-1.0	–	1.0	V	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
I_{MIO}	Maximum Current into any Port and Function Pin	-25	–	+50	mA	

Note
2. Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. The system designer must ensure that the Absolute Maximum Ratings are NEVER exceeded. Functional operation is not implied under any conditions beyond the “Electrical Characteristics”, listed page 27 onwards. Extended exposure to “Absolute Maximum Ratings” may affect device reliability.

Symbol	Description	Min	Typ	Max	Units	Notes
LU	Latch Up current	200	–	–	mA	JESD78A Conformal
ESD	Electrostatic Discharge Voltage	2000	–	–	V	Human Body Model ESD.
t_{REGIN}	High Voltage Supply Ramp Time (SREGHVIN pin)	1	–	–	µs	
t_{HVDD}	High Voltage Supply Ramp Time (CSPx pins)	150	–	–	ns	

Figure 14-1. High Voltage Supply Ramp Time (SREGHVIN pin)



14.2 Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	$T_J \leq 115°C$
T_J	Junction Temperature	-40	–	+115	°C	

15. Electrical Characteristics

15.1 System Level

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115^oC$. These are for design guidance only.

Table 15-1. System Level Operating Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{SW}	Circuit Switching Frequency Range for Hysteretic Control Loop	0.02	–	2	MHz	
$t_{D,MAX}$	Maximum Delay Time from CSA Input to FET State Change	–	–	100	ns	HVDD = 24V, I_D = 1A, f_{SW} = 2 MHz
D	Output Duty Cycle for Hysteretic Controllers	5	–	95	%	f_{SW} < 0.25 MHz
E	Power Converter Efficiency	90	95	–	%	HVDD = 24V, I_D = 1A, f_{SW} = 2 MHz

15.2 Chip Level

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Note See the *PowerPSoC Technical Reference Manual* for more information on the DPWMxPCF register

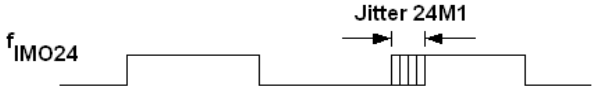
Table 15-2. Chip Level DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
VDD, AVDD, GDVDD	Digital, Analog, and Gate Driver Supply Voltage Range	4.75	–	5.25	V	All should be powered from the same source.
HVDD	High Voltage Supply Voltage Range	7	–	32	V	Applies to High Voltage pins CSPx and SREGHVIN. Not all pins need to be at the same voltage level.
I_{VDD}	Supply Current (VDD pins), IMO = 24 MHz	–	16	50	mA	Conditions are VDD = 5V, T_J = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{AVDD}	Supply Current(AVDD pin)	–	–	25	mA	Conditions are VDD = 5V, T_J = 25°C,
I_{GDVDD}	Supply Current Per Channel(GDVDD pins)	– –	– –	25 100	mA mA	Internal Power FET at 2 MHz External Gate Driver at 1 MHz, C_L = 4 nF at VDD = 5V
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.	– –	18 30	25 550	µA µA	T_J = 25°C, Built-in Switching Regulator disabled, DPWMxPCF = 0, Power Peripherals disabled, analog power = off T_J = 115°C, Built-in Switching Regulator disabled, DPWMxPCF = 0, Power Peripherals disabled, analog power = off

Table 15-3. Chip Level AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.04	24	24.96	MHz	
f_{CPU1}	CPU Frequency	0.093	24	24.96	MHz	
f_{BLK}	Digital PSoC Block Frequency	0	48	49.92[3]	MHz	Refer to "PSoC Core Digital Block Specifications" on page 47.
f_{32K1}	Internal Low-Speed Oscillator Frequency	15	32	64	kHz	
Jitter32k	32 kHz Period Jitter	–	100	–	ns	
Jitter24M1	24 MHz Period Jitter (IMO) Peak-to-Peak	–	600	–	ps	

Figure 15-1. 24 MHz Period Jitter (IMO) Timing Diagram



15.3 Power Peripheral Low Side N-Channel FET

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-4. Low Side N-Channel FET DC Specifications

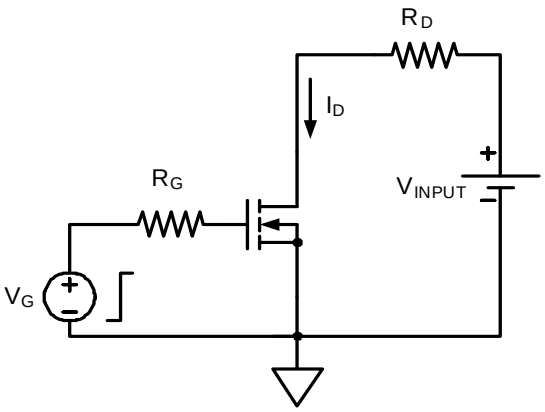
Symbol	Description	Min	Typ	Max	Units	Notes
V_{DS}	Operating Drain to Source Voltage	–	–	32	V	
$V_{DS,INST}$	Instantaneous Drain Source Voltage	–	–	36	V	
I_D	Average Drain Current	– –	– –	1 0.5	A A	CY8CLED04/3/2/1D01 devices CY8CLED04/3D02 devices
I_{DMAX}	Maximum Instantaneous Repetitive Pulsed Current	– –	– –	3 1.5	A A	Less than 33% duty cycle for an average current of 1A, f_{SW} = 0.1MHz. CY8CLED04/3/2/1D01 devices Less than 33% duty cycle for an average current of 0.5A, f_{SW} = 0.1MHz. CY8CLED04/3D02 devices
$R_{DS(ON)}$	Drain to Source ON resistance	– –	– –	0.5 1	Ω Ω	I_D = 1A, GDVDD = 5V, T_J = 25°C CY8CLED04/3/2/1D01 devices I_D = 0.5A, GDVDD = 5V, T_J = 25°C CY8CLED04/3D02 devices
I_{DSS}	Switching Node to PGND Leakage	– –	– –	10 250	µA µA	T_J = 25°C T_J = 115°C
I_{SFET}	Supply Current Per Channel - FET (Internal Gate Driver)	–	–	6.25	mA	f_{SW} = 2 MHz

Table 15-5. Low Side N-Channel FET AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_R	Rise Time	–	–	20	ns	I_D = 1A, R_D = 32Ω
t_F	Fall Time	–	–	20	ns	I_D = 1A, R_D = 32Ω

Note
3. See the individual user module data sheets for information on maximum frequencies for user modules.

Figure 15-2. Low Side N-Channel FET Test Circuit for I_{DSS}, $t_{R, and}$ t_F



15.4 Power Peripheral External Power FET Driver

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115^oC$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-6. Power FET Driver DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OHN}	N-Channel FET Driver Output Voltage -Drive High	VDD - 0.45 VDD - 0.1	– –	– –	V V	I_{OH} =100 mA I_{OH} =10 mA
V_{OLN}	N-Channel FET Driver Output Voltage -Drive Low	– –	– –	0.45 0.1	V V	I_{OL} =100 mA I_{OL} =10 mA
$I_{SFETDRV}$	Supply Current Per Channel - External FET Driver	–	–	25	mA	C_L = 4nF at GDVDD = 5V, F_{SW} = 1 MHz

Table 15-7. Power FET Driver AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_r	Rise Time	–	45	55	ns	C_L = 4nF at GDVDD = 5V
t_f	Fall Time	–	45	55	ns	
tp(LH)	Propagation Delay (Low-to-High)	–	–	10	ns	
tp(HL)	Propagation Delay (High-to-Low))	–	–	10	ns	

15.5 Power Peripheral Hysteretic Controller

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-8. Hysteretic Controller DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IO}	Comparator Input Offset Voltage	– –	– –	7.5 15	mV mV	$1V \leq V_{ICM} \leq 3V$ $0V \leq V_{ICM} \leq VDD$
V_{ICM}	Input Common Mode Voltage Range	0	–	VDD	V	
V_H	Hysteresis Voltage	4.5	–	11	mV	Comparator Internal Hysteresis V_{ICM} = 1.5V - 2.5V
I_{SHYST}	Supply Current - Hysteretic Controller	–	2	–	mA	Includes two Power Peripheral Comparators and one Reference DAC, f_{SW} = 2 MHz

Table 15-9. Hysteretic Controller AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ON} / t_{OFF}	Minimum ON/OFF timer					
	MONOSHOT<1:0> = 00	10	–	30	ns	
	MONOSHOT<1:0> = 01	20	–	60	ns	
	MONOSHOT<1:0> = 10	40	–	110	ns	
	MONOSHOT<1:0> = 11	–	–	–	ns	Timers Disabled

15.6 Power Peripheral Comparator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

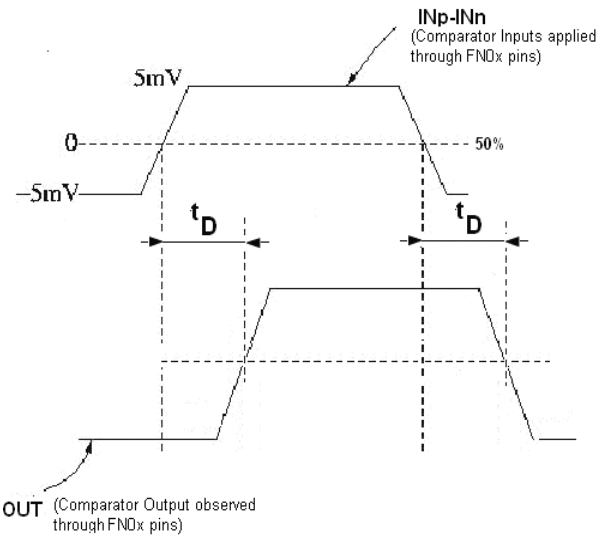
Table 15-10. Comparator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IN}	Input Voltage Range	0	–	VDD	V	
V_{IO}	Comparator Input Offset Voltage	– –	– –	7.5 15	mV mV	$1V \leq V_{ICM} \leq 3V$ $0V \leq V_{ICM} \leq VDD$
V_{HYS}	Hysteresis Voltage	2.5 4.5	– –	30 11	mV mV	$2.5V < V_{ICM} < 1.5V$ $1.5V \leq V_{ICM} \leq 2.5V$
V_{OVDRV}	Overdrive Voltage	5	–	–	mV	
I_{SCOMP}	Supply Current - Comparator	–	–	650	µA	
$V_{ICM,COMP}$	Comparator Input Common Mode Voltage Range	0	–	VDD	V	

Table 15-11. Comparator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_D	Comparator Delay Time (FN0x pin to FN0x pin)	–	150	–	ns	V_{OVDRV} = 5mV, C_L = 10pF at VDD = 5V

Figure 15-3. Comparator Timing Diagram



15.7 Power Peripheral Current Sense Amplifier

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115^oC$. Typical parameters apply to VDD of 5V and HVDD of 32V at 25°C. These are for design guidance only.

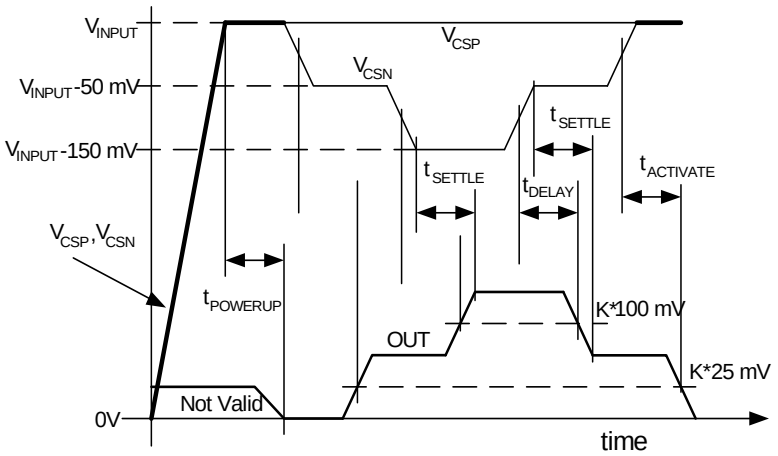
Table 15-12. Current Sense Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ICM}	Input Common Mode Voltage Operating Range	7	–	32	V	Either terminal of the amplifier must not exceed this range for functionality
$V_{ICM(Tolerant)}$	Non Functional Operating Range	0	–	32		Absolute Maximum Rating for V_{SENSE} should never be exceeded. See Absolute Maximum Ratings on page 29
V_{SENSE}	Input Differential Voltage Range	0	–	150	mV	
$I_{S,CSA}$	Supply Current - CSA	–	–	1	mA	Enabling CSA causes an incremental draw of 1 mA on the AVDD rail.
I_{BIASP}	Input Bias Current (+)	–	–	600	µA	
I_{BIASN}	Input Bias Current (-)	–	–	1	µA	
PSR_{HV}	Power Supply Rejection (CSP pin)	–	–	-25	dB	f_{SW} < 2 MHz
K	Gain	19.7	20	20.3	V/V	V_{SENSE} = 50 mV to 130 mV
V_{IOS}	Input Offset	–	–	2	mV	V_{SENSE} = 50 mV to 130 mV
C_{IN_CSP}	CSP Input Capacitance	–	–	5	pF	
C_{IN_CSN}	CSN Input Capacitance	–	–	2	pF	

Table 15-13. Current Sense Amplifier AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{SETTLE}	Output Settling Time to 1% of Final Value	–	–	5	µs	
$t_{POWERUP}$	Power Up Time to 1% of Final Value	–	–	5	µs	

Figure 15-4. Current Sense Amplifier Timing Diagram



15.8 Power Peripheral PWM/PrISM/DMM Specification Table

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115^oC$. Typical parameters apply to 5V at 25°C. These are for design guidance only. See the *PowerPSoC Technical Reference Manual* for more information on PWM/PrISM/DMM.

Table 15-14. PWM/PrISM/DMM DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$I_{S,Modulation}$	Supply Current - PWM, PrISM, or DMM	–	–	5	mA	

Table 15-15. PWM/PrISM/DMM AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
PWM Mode						
$f_{RANGE16}$	PWM Output Frequency Range 16-bit period	24,000,000/(256*2^{16})	–	48,000,000/2^{16}	Hz	Period Value = 2^{16} -1, Min: N = 255, Max: N = 0
f_{RANGE8}	PWM Output Frequency Range 8-bit period	24,000,000/(256*2^8)	–	48,000,000/2^8	Hz	Period Value = 2^8 -1, Min: N = 255, Max: N = 0
PrISM Mode						
f_{RANGE}	PrISM Output Frequency Range	24,000,000/(256*(2^M-1)	–	48,000,000/2	Hz	Min: N = 255, Maqx: N = 0, M = 2 to 16
DMM Mode						
$f_{RANGE,Dimming}$	DMM Dimming Frequency Range	24,000,000/ (256*Max DMM Period)	–	48,000,000/(Min DMM Period)	Hz	Min DMM Period: 2 (Right Aligned), 3 (Center Aligned), 4(Left Aligned) Max DMM Period: 2^{12} (Right Aligned), 8190 (Center Aligned), 2^{12} (Left Aligned)
$f_{RANGE,Dither}$	DMM Dither Frequency Range	(1/16)*(Min $f_{RANGE,Dimming}$)	–	(15/16)*(Max $f_{RANGE,Dimming}$)	Hz	

15.9 Power Peripheral Reference DAC Specification

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115^oC$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-16. Reference DAC DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{SDAC}	Supply Current - Reference DAC	–	–	600	µA	Mode 0 and Mode1
INL	Integral Non Linearity	-1 -1.5	– –	1 1.5	LSB LSB	Mode 0 Mode 1
DNL	Differential Non Linearity	-0.5	–	0.5	LSB	Mode 0 and Mode1
A_{ERROR}	Gain Error	-5 -7	– –	5 7	LSB LSB	Mode 0 Mode 1
OS_{ERROR}	Offset Error	–	–	1	LSB	Mode 0 and Mode1
V_{DACFS}	Fullscale Voltage - Reference DAC	– –	– –	2.6 1.3	LSB LSB	Mode 0 Mode 1
V_{DACMM}	Fullscale Voltage Mismatch (Pair of Reference DACs - Even and Odd)	– –	– –	7 12	LSB LSB	Mode 0 Mode 1

Table 15-17. Reference DAC AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{SETTLE}	Output settling time to 0.5 LSB of final value	–	–	10	µs	Mode 0 and Mode1
$t_{STARTUP}$	Startup time to within 0.5 LSB of final value	–	–	10.5	µs	Mode 0 and Mode1

15.10 Power Peripheral Built-in Switching Regulator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115^oC$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-18. Built-in Switching Regulator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REGIN}	Input Supply Voltage Range	7	–	32	V	See Absolute Maximum Ratings on page 29
V_{REGOUT}	Output Voltage Range	4.8	5.0	5.2	V	Does not include V_{RIPPLE}
V_{RIPPLE}	Output Ripple	–	–	100	mV	
V_{UVLO}	Under Voltage Lockout Voltage	5.5	–	6.5	V	$V_{REGIN} < V_{UVLO}$: Power Down Mode $V_{REGIN} > V_{UVLO}$: Active Mode
I_{LOAD}	DC Output Current -Active Mode	0.01	–	250	mA	
$I_{S,BSR}$	Supply Current - Built-in Switching Regulator	–	–	4	mA	
$I_{SB,HV}$	Standby Current (High Voltage)	–	–	250	µA	
I_{INRUSH}	Inrush Current	–	–	1.2	A	
$R_{DS(ON),PFET}$	PFET Drain to Source ON resistance	–	2.5	–	Ω	
$Line_{REG}$	Line Regulation	–	1	–	mV	I_{LOAD} = 250 mA, V_{REGIN} = 7V to 32V
$Load_{REG}$	Load Regulation	–	1	–	mV	V_{REGIN} = 24V, I_{LOAD} = 2.5 mA to 250 mA
PSRR	Power Supply Rejection Ratio	–	-60	–	dB	$V_{RIPPLE} = 0.2*V_{REGIN}$, f_{RIPPLE} = 1 kHz to 10 kHz
E_{BSR}	Built-in Switching Regulator Efficiency	80	–	–	%	V_{REGIN} = 24 V, I_{LOAD} = 250 mA

Table 15-19. Built-in Switching Regulator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{SW}	Switching Frequency	0.956	1	1.04	MHz	
t_{RESP}	Response time to within 0.5% of final value	–	10	–	µs	
t_{SU}	Startup Time	–	–	1	ms	
t_{PD}	Power Down Time	–	–	100	µs	
t_{REGIN}	High Voltage Supply Ramp Time (SREGHVIN pin)	1	–	–	µs	See Absolute Maximum Ratings on page 29
t_{PD_ACT}	Time from Power Down to Active Mode	–	–	1	ms	
t_{ACT_PD}	Time from Active Mode to Power Down Mode	–	–	50	µs	

Table 15-20. Built-in Switching Regulator Recommended Components

Component Name	Value	Unit	Notes
R_{fb1}	2	kΩ	Tolerance 1% or better
R_{fb2}	0.698	kΩ	Tolerance 1% or better
C_{comp}	2200	pF	Tolerance 20% or better
R_{comp}	20	kΩ	Tolerance 5% or better
L	47	µH	Tolerance 20% or better, Saturation current rating of 1.5 A or higher
R_{sense}	0.5	Ω	Tolerance 1% or better
C_1	10	µF	Ceramic, X7R grade, Minimum ESR of 0.1Ω
C_{in}	1	µF	Ceramic, X7R grade

Figure 15-5. Built-in Switching Regulator Timing Diagram

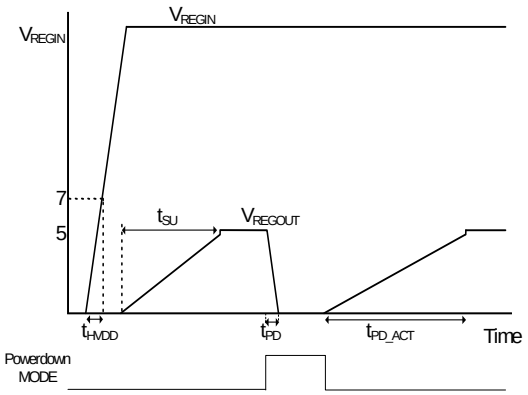
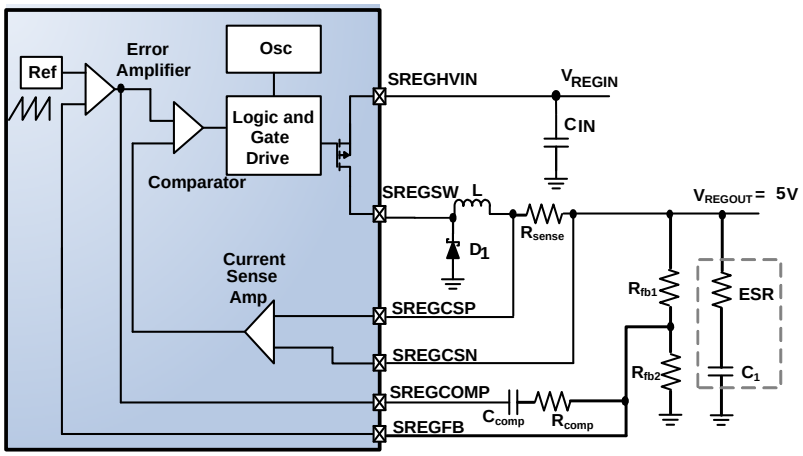


Figure 15-6. Built-in Switching Regulator



15.11 General Purpose IO/Function Pin IO

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

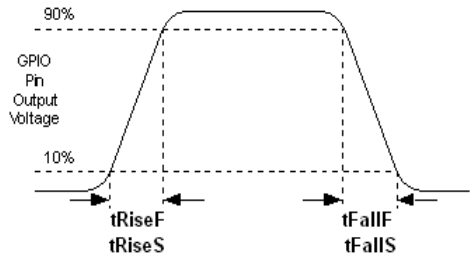
Table 15-21. GPIO/FN0 Pin IO DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	VDD - 1.0	–	–	V	IOH = 10 mA, 80 mA maximum combined IOH budget
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, 200 mA maximum combined IOL budget
V_{IL}	Input Low Level	–	–	0.8	V	
V_{IH}	Input High Level	2.1	–		V	
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	T_J = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	T_J = 25°C.

Table 15-22. GPIO/FN0 Pin IO AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
f_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
tRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	10% - 90%
tFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	
tRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	
tFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	

Figure 15-7. GPIO/Function IO Timing Diagram



15.12 PSoC Core Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 15-23. Operational Amplifier DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 analog pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 analog pins)	–	4.5	9.5	pF	T_J = 25°C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	VDD VDD - 0.5	V V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 60 60 80	 – – –	 – – –	 dB dB dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 VDD - 0.2 VDD - 0.2 VDD - 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated Analog Output Buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	52	80	–	dB	VSS ≤ VIN ≤ (VDD - 2.25) or (VDD - 1.25V) ≤ VIN ≤ VDD.

Table 15-24. Operational Amplifier AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	
t_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%) (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	

15.13 PSoC Core Low Power Comparator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-25. Low Power Comparator DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	VDD - 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	40	mV	

Table 15-26. Low Power Comparator AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

15.14 PSoC Core Analog Output Buffer

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-27. Analog Output Buffer DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	VDD - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 0.6 0.6	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to VDD/2) Power = Low Power = High	0.5 x VDD + 1.1 0.5 x VDD + 1.1	– –	– –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to VDD/2) Power = Low Power = High	– –	– –	0.5 x VDD - 1.3 0.5 x VDD - 1.3	V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	52	64	–	dB	(0.5 x VDD - 1.3) ≤ V_{OUT} ≤ (VDD - 2.3).

Table 15-28. Analog Output Buffer AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 2.5 2.5	 µs µs	
t_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 2.2 2.2	 µs µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/µs V/µs	
BW_{OBSS}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100 pF Load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100 pF Load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz	

15.15 PSoC Core Analog Reference

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 15-29. Analog Reference DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V	
–	AGND = VDD/2[4]	VDD/2 - 0.04	VDD/2 - 0.01	VDD/2 + 0.007	V	
–	AGND = 2 x BandGap[4]	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V	
–	AGND = BandGap[4]	BG - 0.009	BG + 0.008	BG + 0.016	V	
–	AGND = 1.6 x BandGap[4]	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V	
–	AGND Block to Block Variation (AGND = VDD/2)[4]	-0.034	0.000	0.034	V	
–	RefHi = VDD/2 + BandGap	VDD/2 + BG - 0.10	VDD/2 + BG	VDD/2 + BG + 0.10	V	
–	RefHi = 3 x BandGap	3 x BG - 0.06	3 x BG	3 x BG + 0.06	V	
–	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V	
–	RefLo = VDD/2 – BandGap	VDD/2 - BG - 0.04	VDD/2 - BG + 0.024	VDD/2 - BG + 0.04	V	
–	RefLo = BandGap	BG - 0.06	BG	BG + 0.06	V	

15.16 PSoC Core Analog Block

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-30. Analog Block DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

15.17 PSoC Core POR and LVD

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PowerPSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 15-31. POR and LVD DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	VDD Value for PPOR Trip					VDD must be greater than or equal to 2.5V during startup or reset from Watchdog
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.70	V	
	VDD Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[5]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[6]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	

Notes
4. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.
5. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
6. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

15.18 PSoC Core Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-32. Programming DC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	15	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.1	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	VSS + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	VDD - 1.0	–	VDD	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[7]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention[8]	10	–	–	Years	

Table 15-33. Programming AC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
t_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
f_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
t_{WRITE}	Flash Block Write Time	–	30	–	ms	
t_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	

Notes

7. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles)
   For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
8. Guaranteed for $-40°C \leq T_A \leq 85°C$

15.19 PSoC Core Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-34. Digital Block AC Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50[9]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.92	MHz	
	Maximum Frequency, With Capture	–	–	24.96	MHz	
Counter	Enable Pulse Width	50[9]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.92	MHz	
	Maximum Frequency, Enable Input	–	–	24.96	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[9]	–	–	ns	
	Disable Mode	50[9]	–	–	ns	
	Maximum Frequency	–	–	49.92	MHz	
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.92	MHz	
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.96	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.32	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.16	MHz	
	Width of SS_ Negated Between Transmissions	50[9]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.96	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with VDD ≥ 4.75V, 2 Stop Bits	–	–	49.92	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.96	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with VDD ≥ 4.75V, 2 Stop Bits	–	–	49.92	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

Note
9. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

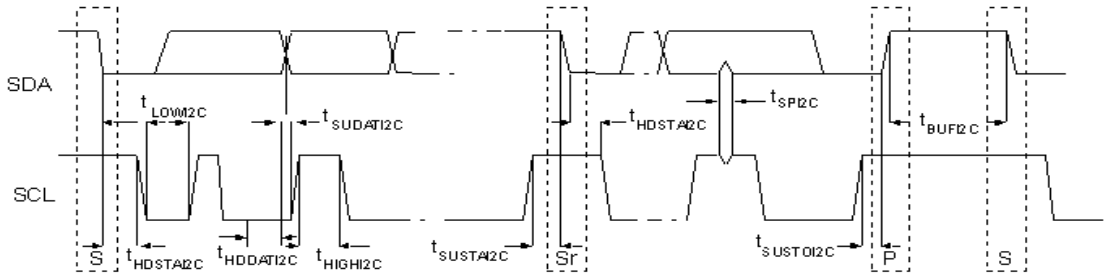
15.20 PSoC Core I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $T_J \leq 115°C$. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 15-35. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
f_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$t_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
t_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$t_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$t_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$t_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$t_{SUDATI2C}$	Data Setup Time	250	–	100[10]	–	ns	
$t_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs	
t_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
t_{SPI2C}	Pulse Width of Spikes are Suppressed by the Input Filter.	–	–	0	50	ns	

Figure 15-8. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

10. A fast mode I2C bus device can be used in a standard mode I2C bus system, but the requirement $t_{SUDATI2} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + $t_{SUDATI2}$ = 1000 + 250 = 1250 ns (according to the standard mode I2C bus specification) before the SCL line is released.

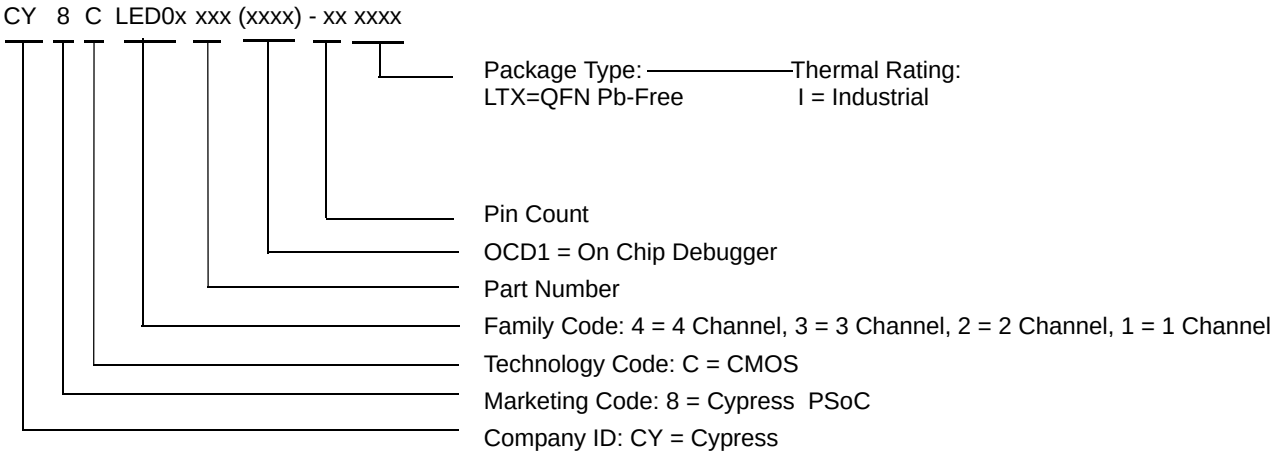
16. Ordering Information

16.1 Key Device Features

Table 16-1. Device Key Features and Ordering Information

PowerPSoC Part Number	No. of Pins	Package	Channels	Voltage	Internal FETs	Gate Drivers for External Low Side N-FETs
CY8CLED04D01-56LTXI	56 QFN	8 mm X 8 mm	4	32V	4 X 1.0A	4
CY8CLED04D02-56LTXI	56 QFN	8 mm X 8 mm	4	32V	4 X 0.5A	4
CY8CLED04G01-56LTXI	56 QFN	8 mm X 8 mm	4	32V	0	4
CY8CLED04DOCD1-56LTXI	56 QFN	8 mm X 8 mm	4	32V	4 X 1.0A	4
CY8CLED03D01-56LTXI	56 QFN	8 mm X 8 mm	3	32V	3 X 1.0A	3
CY8CLED03D02-56LTXI	56 QFN	8 mm X 8 mm	3	32V	3 X 0.5A	3
CY8CLED03G01-56LTXI	56 QFN	8 mm X 8 mm	3	32V	0	3
CY8CLED02D01-56LTXI	56 QFN	8 mm X 8 mm	2	32V	2 X 1.0A	2
CY8CLED01D01-56LTXI	56 QFN	8 mm X 8 mm	1	32V	1 X 1.0A	1

17. Ordering Code Definitions



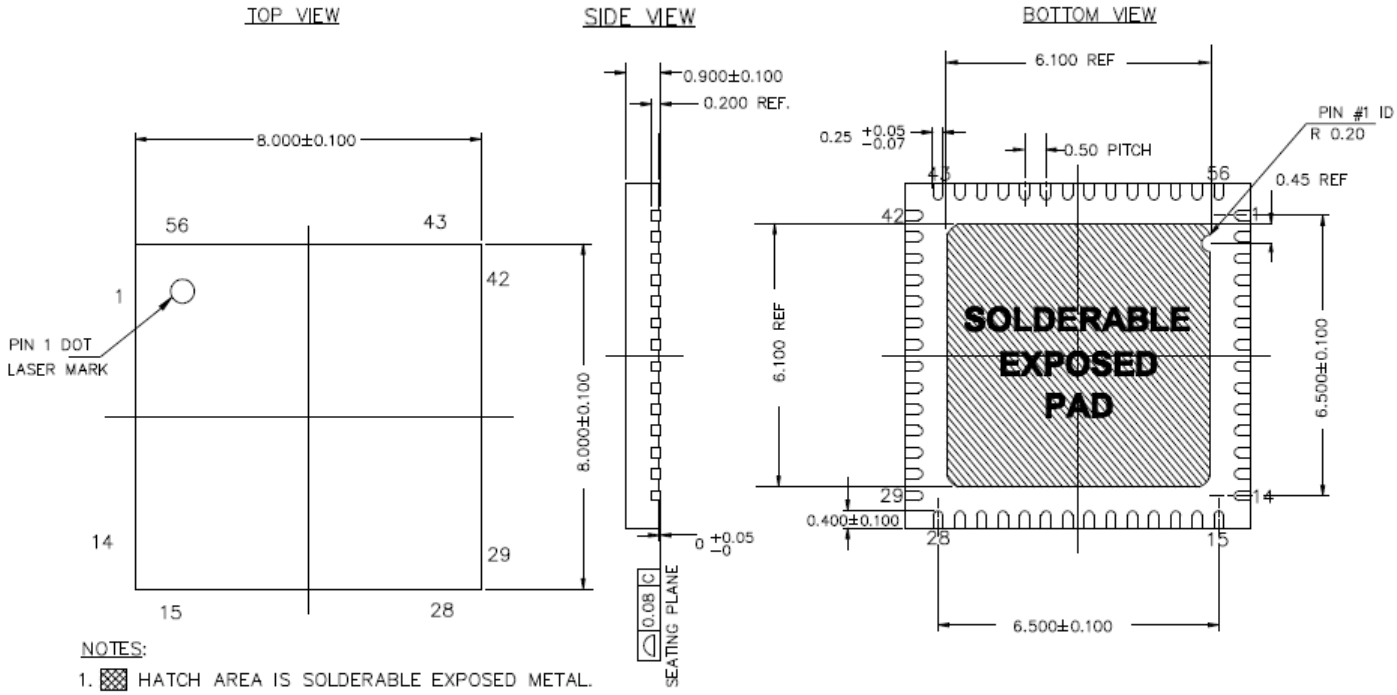
18. Packaging Information

Packaging Dimensions

This section illustrates the package specification for the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 along with the thermal impedance for the package and solder reflow peak temperatures.

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Figure 18-1. 56-Pin (8x8 mm) QFN



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18.1 Thermal Impedance

Package	Typical θ_{JA} [11]
56 QFN[12]	16.6 °C/W

18.2 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Package	Minimum Peak Temperature[13]	Maximum Peak Temperature
56 QFN	240°C	260°C

Notes
11. $T_J = T_A + POWER \times \theta_{JA}$
12. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.
13. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste Refer to the solder manufacturer specifications.

19. Development Tools

19.1 Software

This section presents the development tools available for all current PowerPSoC device families including the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01.

19.1.1 PSoC Designer 5.0™

At the core of the PSoC development software suite is PSoC Designer. Used by thousands of PSoC developers, this robust software has been facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at under Design Resources > Software and Drivers.

19.1.2 PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer 5.0. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

19.2 Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PowerPSoC device, see AN2323, *Debugging - Build a PSoC Emulator into Your Board.*

20. Document History Page

Document Title: CY8CLED04D01, CY8CLED04D02, CY8CLED04G01, CY8CLED03D01, CY8CLED03D02, CY8CLED03G01, CY8CLED02D01, CY8CLED01D01 PowerPSoC® Intelligent LED Driver Document Number: 001-46319				
Revision	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2506500	ANWA/ DSG	05/20/08	New data sheet.
*A	2575708	ANWA/ AESA	10/01/08	1) Updated Logic Block Diagram with AINX label and SREGFB pin. 2) Updated Current Sense Amplifier Specification Table. 3) Updated External Gate Driver Specification Table. 4) Updated Register Table.
*B	2662774	KJV	02/19/09	Extensive changes made to content and electrical specifications.
*C	2665155	KJV/PYRS	02/25/09	Updated Notes in electrical specifications.
*D	2671254	KJV/PYRS	03/10/09	Updated sections 8, 9, and 10 on pages 14, 15, and 16.
*E	2683506	VED	04/03/09	Release to the external web site
*F	2698529	KJV/PYRS	04/27/09	Updated Figure 14-1, Figure 15-2, and Figure 15-4.
*G	2735072	KJV	07/10/09	Added 1 and 2 channel part information

21. Sales, Solutions, and Legal Information

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