

Typical Applications

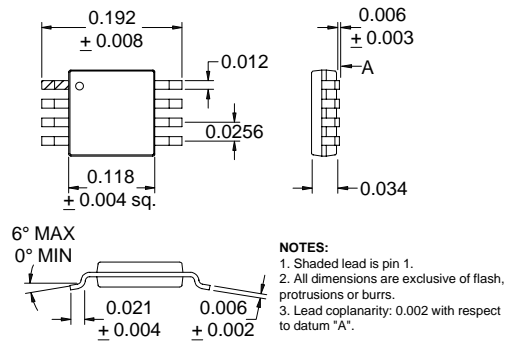
- Low Voltage
- Wireless LANs
- IF LO for 2.45GHz ISM Band Systems
- Wireless Local Loop
- Digital Cordless Phones

Product Description

The RF2506 is an integrated oscillator and buffer amplifier chain designed to achieve low sensitivity to fluctuations in load impedance and power supply noise, while maintaining superior phase noise performance. The IC offers great flexibility, yet is easy to use. This product was designed for use in applications with low supply voltages. It has a power-down feature and is designed to operate from 10MHz to 1000MHz with the help of an external resonator. Frequency control is achieved with an external varactor diode. The IC's ease of use, reduced load pulling, small size, and low cost make it an ideal LO (Local Oscillator) for wireless applications in the VHF/UHF range. The RF2506 was designed to operate with the 2.4GHz chipset; specifically with the IF portion of the RF2518 PLL/synthesizer.

Optimum Technology Matching® Applied

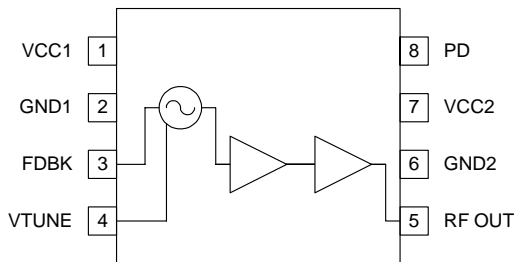
- | | | |
|--|-----------------------------------|--------------------------------------|
| <input type="checkbox"/> Si BJT | <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> GaAs MESFET |
| <input checked="" type="checkbox"/> Si Bi-CMOS | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si CMOS |



Package Style: MSOP-8

Features

- High-Isolation/Reduced Load Pulling
- Low Current Consumption
- -7dBm Output Power
- Digitally Controlled Power Down Mode
- 10MHz to 1GHz Operating Range
- Single 2.7V to 3.6V Supply



Functional Block Diagram

Ordering Information

RF2506	VHF/UHF VCO/High-Isolation Buffer Amplifier
RF2506 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.8	V _{DC}
Power Down Voltage (V _{PD})	-0.5 to +5.8	V _{DC}
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-55 to +150	°C



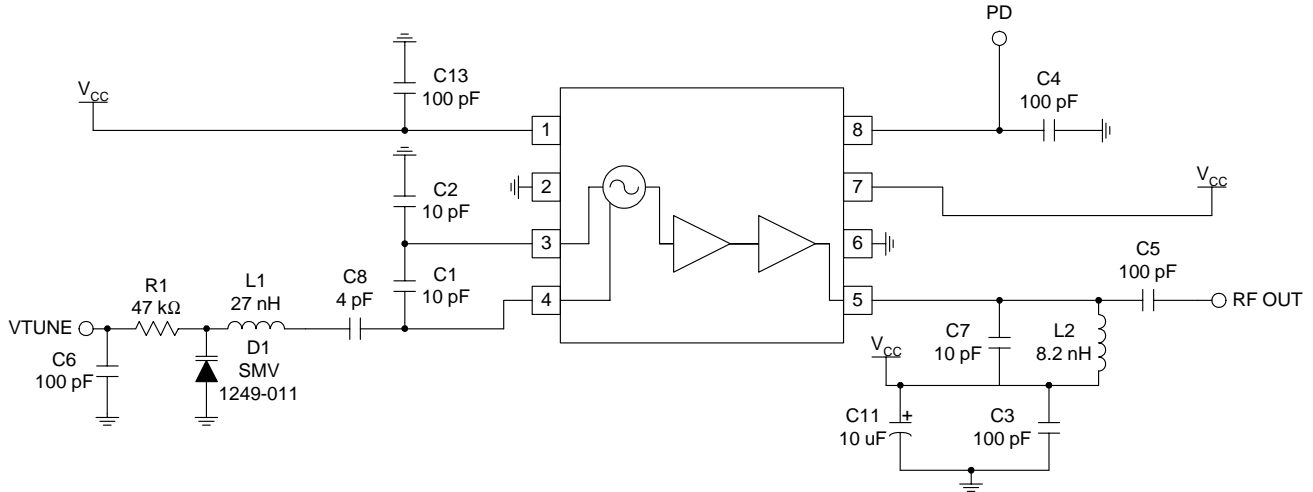
Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall Operating Frequency		10 to 1000		MHz	
560MHz Operation Output Power 2nd Harmonic 3rd Harmonic Load Pulling V _{CC} Pushing Phase Noise		-3 -27 -35 50 190 -110 -90		dBm dBc dBc kHz _{P-P} kHz/V dBc dBc	T=25 °C, V _{CC} =2.7V, Z _{LOAD} =50Ω, V _{PD} =2.7V, O/P terminated into LC. Characterized @ 560MHz as per eval board. Data will change depending on frequency of operation and resonant tank network. Into 1.75 VSWR Load Supply sweep from 2.7V to 3.2V 100kHz Offset. Better phase noise is achievable by increasing the loaded Q of the resonator circuit. 10kHz Offset
560MHz Operation Output Power 2nd Harmonic 3rd Harmonic Load Pulling V _{CC} Pushing Phase Noise		-7 -11.5 -15.5 35 160 -107 -88		dBm dBc dBc kHz _{P-P} kHz/V dBc dBc	T=25 °C, V _{CC} =2.7V, Z _{LOAD} =50Ω, V _{PD} =2.7V, O/P terminated in 50Ω. Characterized @ 560MHz as per eval board. Data will change depending on frequency of operation and resonant tank network. Into 1.75 VSWR Load Supply sweep from 2.7V to 3.2V 100kHz Offset. Better phase noise is achievable by increasing the loaded Q of the resonator circuit. 10kHz Offset
Power Supply Operating Voltage Supply Current		2.7 to 3.6 9		V _{DC} mA	At 2.2V and -40°C, output power will be reduced to typically -11 dBm.

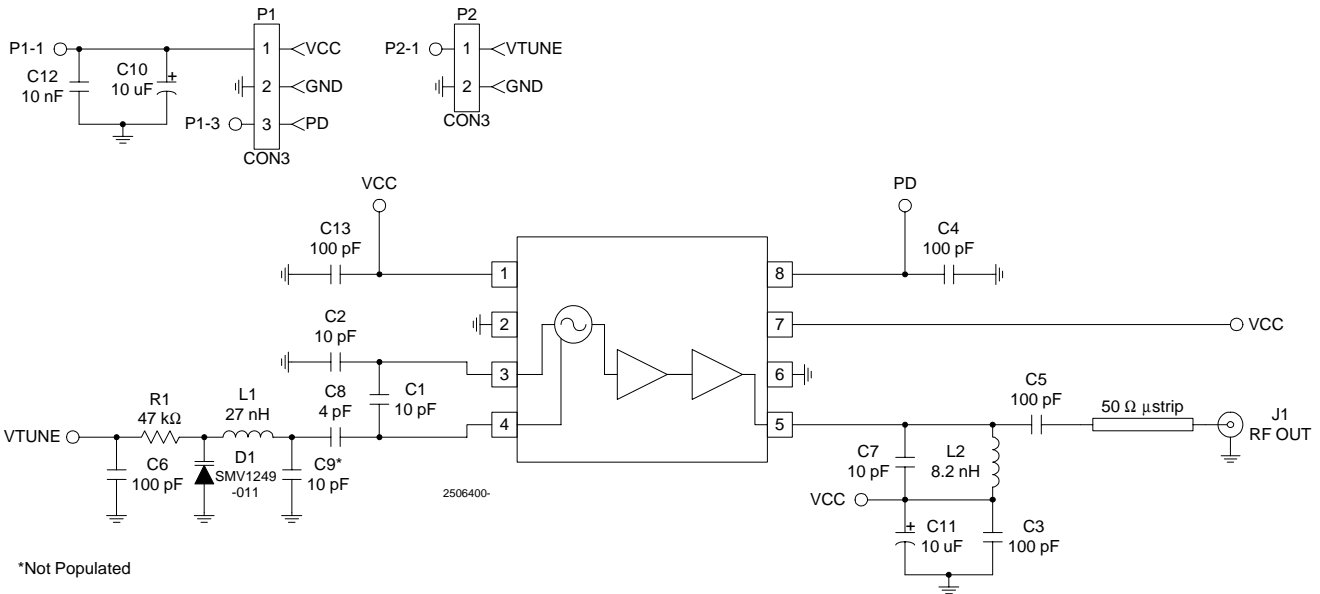
Pin	Function	Description	Interface Schematic
1	VCC1	Power supply connection for the VCO. This pin should be well bypassed close to the package with a capacitor suitable for the frequency of operation as well as a capacitor to minimize low frequency noise from the voltage supply. The ground side of the capacitors should connect immediately to ground plane.	
2	GND1	Ground connection for the VCO. Keep traces physically short and connect immediately to ground plane for best performance. In order to minimize load pulling, it is recommended that pin 2 has a different return path to ground than pin 6 (i.e., separate vias to a common ground plane).	See pin 2.
3	FDBK	Feedback output to resonant circuit. A Colpitts oscillator is formed by placing a capacitor from this pin to pin 4 and from this pin to ground. A DC blocking capacitor, suitable for the frequency of operation, should be used if the external circuitry has DC present or presents a DC path to ground. See the application schematic of this data sheet for design details.	See pin 4.
4	VTUNE	Tank circuit input. A resonant circuit is placed from this pin to ground. The capacitive side is tapped to the FDBK point and the inductive side includes a varactor for voltage tuning to provide the VCO function. A DC blocking capacitor, suitable for the frequency of operation, should be used if the external circuitry has DC present or presents a DC path to ground. See the application schematic of this data sheet for design details.	<p>The schematic shows a varactor connected between the VTUNE pin and the FDBK pin. A DC blocking capacitor is connected between the FDBK pin and GND1. A bias network is connected to the VTUNE pin, consisting of a resistor and a capacitor, labeled 'To Bias Ckts.'. The output of the varactor is labeled 'To Buffer Amps and Bias Ckts.'.</p>
5	RF OUT	RF output pin. This is an open-collector output and must be biased externally. A shunt bias/matching inductor to V_{CC} and a series blocking/matching capacitor are recommended. See Application Example Schematic.	
6	GND2	Ground connection for the buffer amplifiers. Keep traces physically short and connect immediately to ground plane for best performance. In order to minimize load pulling, it is recommended that pin 2 has a different return path to ground than pin 6 (i.e., separate vias to a common ground plane).	
7	VCC2	Power supply connection for the buffer amplifiers. This pin should be well bypassed close to the package with a capacitor suitable for the frequency of operation. The ground side of the capacitor should connect immediately to ground plane.	
8	PD	Power Down pin for the VCO and buffer amplifiers. A logic "low" (0.0 to 0.7V) turns the entire device off and supply current drops to less than $1\mu\text{A}$. A logic "high" ($\geq 3.0\text{V}$) turns the device on. Note that the voltage on this pin should never exceed $5.5V_{DC}$.	

Application Schematic



Evaluation Board Schematic

(Download [Bill of Materials](http://www.rfmd.com) from www.rfmd.com.)



*Not Populated

Evaluation Board Layout 900MHz
Board Size 1.404" x 0.986"
Board Thickness 0.031", Board Material FR-4

