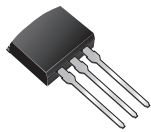




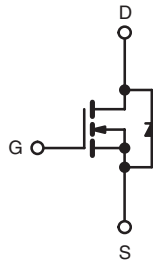
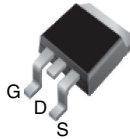
Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	500
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.85
Q_g (Max.) (nC)	38
Q_{gs} (nC)	9.0
Q_{gd} (nC)	18
Configuration	Single

I²PAK (TO-262)



D²PAK (TO-263)



N-Channel MOSFET

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{OSS} Specified
- Lead (Pb)-free Available



RoHS* COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half Bridge
- Full Bridge

ORDERING INFORMATION				
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free	IRF840ASPbF	IRF840ASTRLPbF ^a	IRF840ASTRRPbF ^a	IRF840ALPbF
	SiHF840AS-E3	SiHF840ASTL-E3 ^a	SiHF840ASTR-E3 ^a	SiHF840AL-E3
SnPb	IRF840AS	IRF840ASTL ^a	IRF840ASTRR ^a	IRF840AL
	SiHF840AS	SiHF840ASTL ^a	SiHF840ASTR ^a	SiHF840AL

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V_{DS}		500	V
Gate-Source Voltage	V_{GS}		± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	8.0	A
		$T_C = 100\text{ }^\circ\text{C}$	5.1	
Pulsed Drain Current ^a	I_{DM}		32	
Linear Derating Factor			1.0	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}		510	mJ
Repetitive Avalanche Current ^a	I_{AR}		8.0	A
Repetitive Avalanche Energy ^a	E_{AR}		13	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		125	W
	$T_A = 25\text{ }^\circ\text{C}$		3.1	
Peak Diode Recovery dV/dt ^{c, e}	dV/dt		5.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}		- 55 to + 150	$^\circ\text{C}$
Soldering Temperature	for 10 s		300 ^d	

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 16\text{ mH}$, $R_G = 25\text{ }^\circ\Omega$, $I_{AS} = 8.0\text{ A}$ (see fig. 12).
- $I_{SD} \leq 8.0\text{ A}$, $dI/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- Uses IRF840A/SiH840A data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^d$		-	0.58	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 4.8\text{ A}^b$	-	-	0.85	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 4.8\text{ A}$		3.7	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	1018	-	pF
Output Capacitance	C_{oss}			-	155	-	
Reverse Transfer Capacitance	C_{rss}			-	8.0	-	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	1490	-	-	
Output Capacitance	C_{oss}		$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	42	-	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 0\text{ V to } 480\text{ V}^{c, d}$	56	-	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 8.0\text{ A}, V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^{b, d}	-	-	38	nC
Gate-Source Charge	Q_{gs}			-	-	9.0	
Gate-Drain Charge	Q_{gd}			-	-	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 8.0\text{ A}, R_G = 9.1\text{ }\Omega, R_D = 31\text{ }\Omega$, see fig. 10 ^{b, d}		-	11	-	ns
Rise Time	t_r			-	23	-	
Turn-Off Delay Time	$t_{d(off)}$			-	26	-	
Fall Time	t_f			-	19	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p-n junction diode 		-	-	8.0	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	32	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 8.0\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 8.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	422	633	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	2.0	3.0	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS} .
- Uses IRF840A/SiHF840A data and test conditions

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

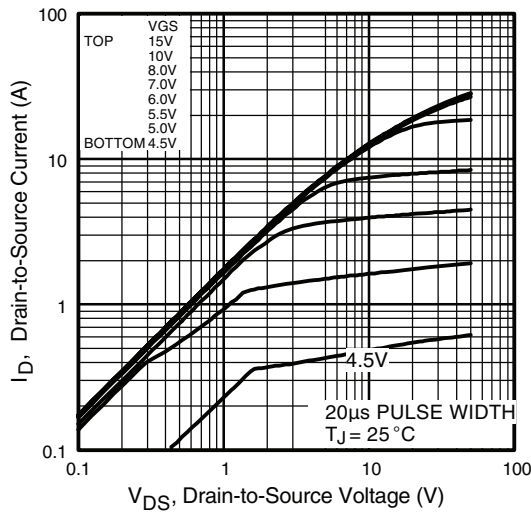


Fig. 1 - Typical Output Characteristics

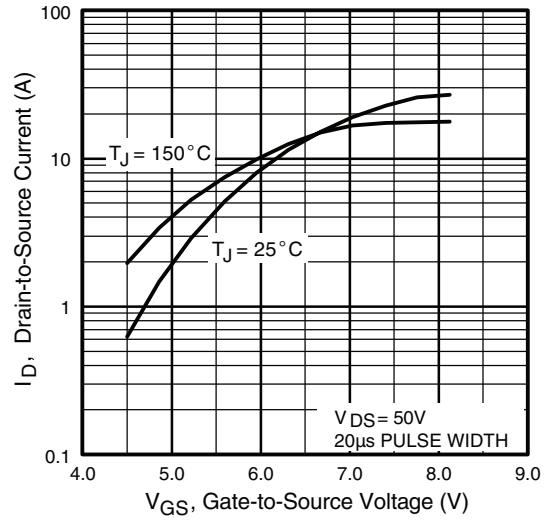


Fig. 3 - Typical Transfer Characteristics

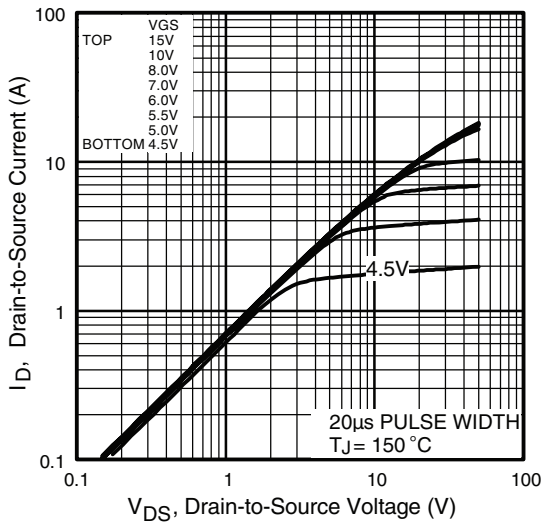


Fig. 2 - Typical Output Characteristics

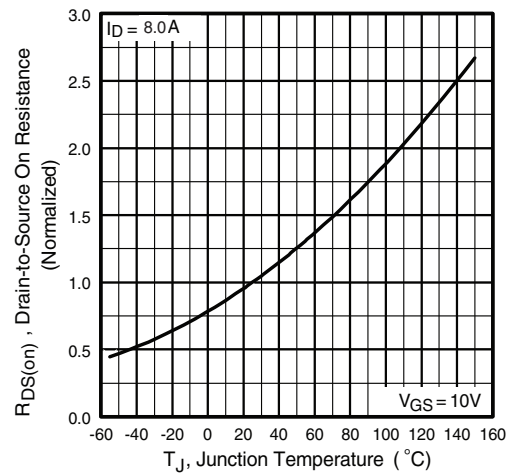


Fig. 4 - Normalized On-Resistance vs. Temperature

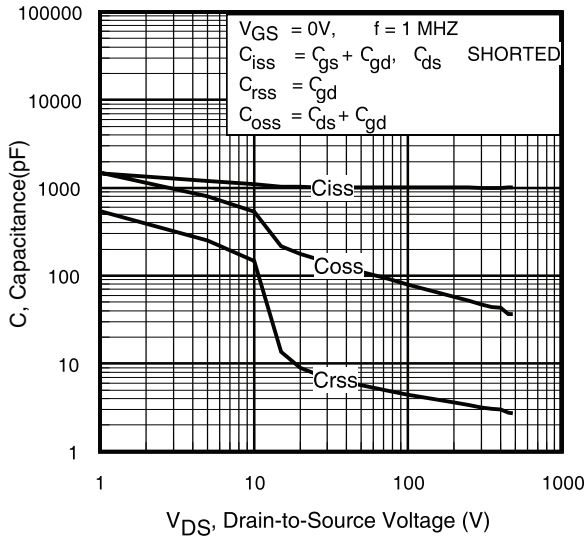


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

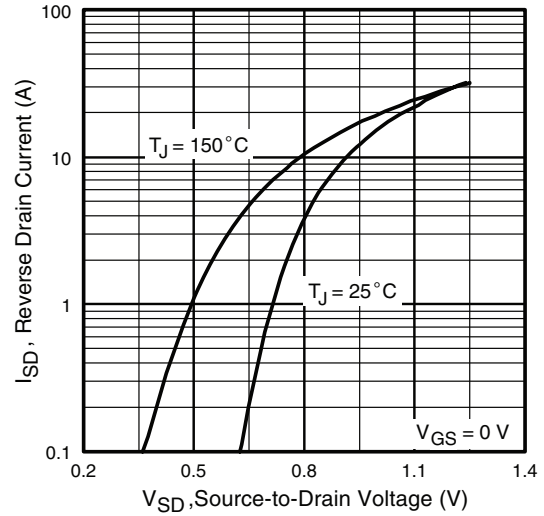


Fig. 7 - Typical Source-Drain Diode Forward Voltage

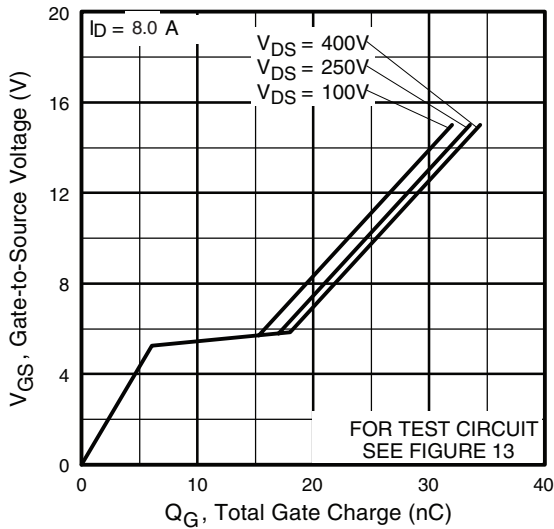


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

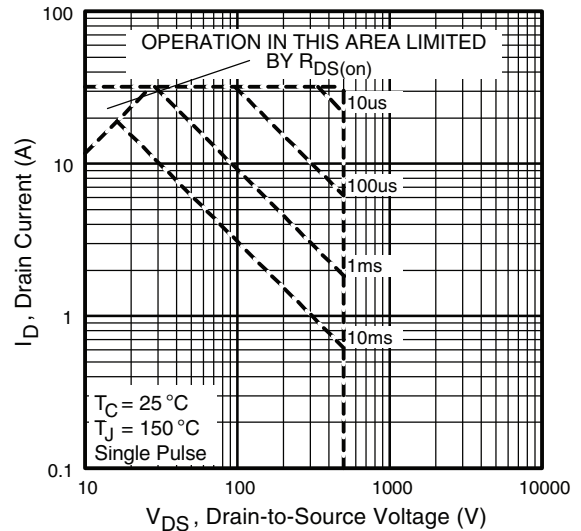


Fig. 8 - Maximum Safe Operating Area

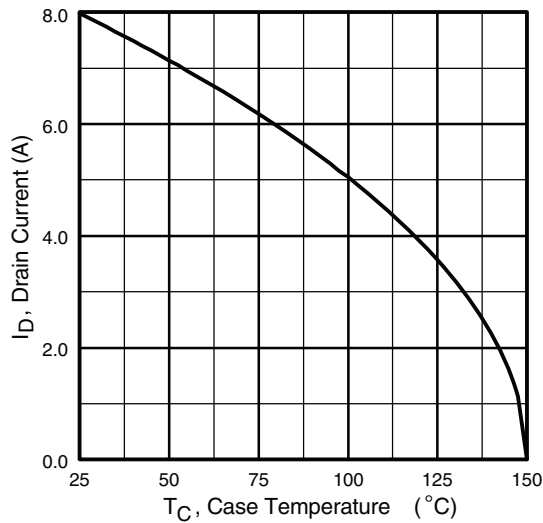


Fig. 9 - Maximum Drain Current vs. Case Temperature

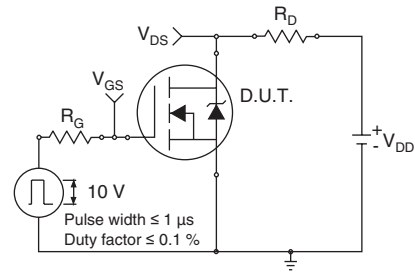


Fig. 10a - Switching Time Test Circuit

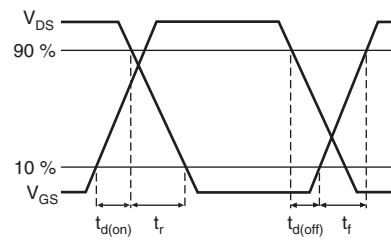


Fig. 10b - Switching Time Waveforms

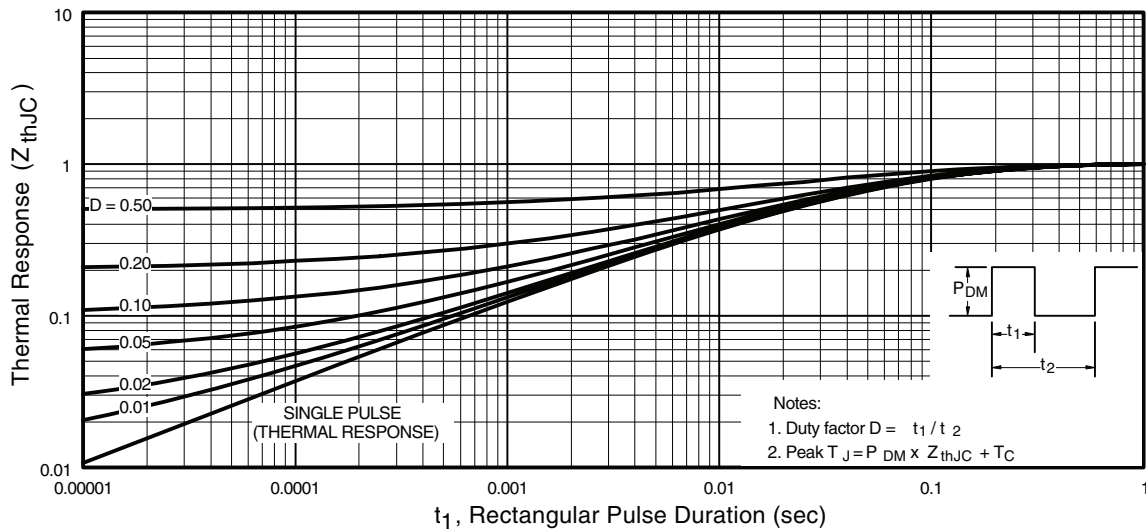


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

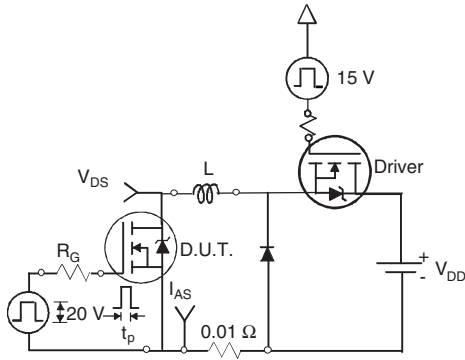


Fig. 12a - Unclamped Inductive Test Circuit

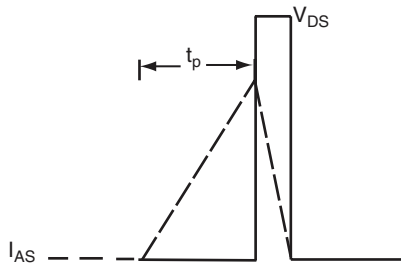


Fig. 12b - Unclamped Inductive Waveforms

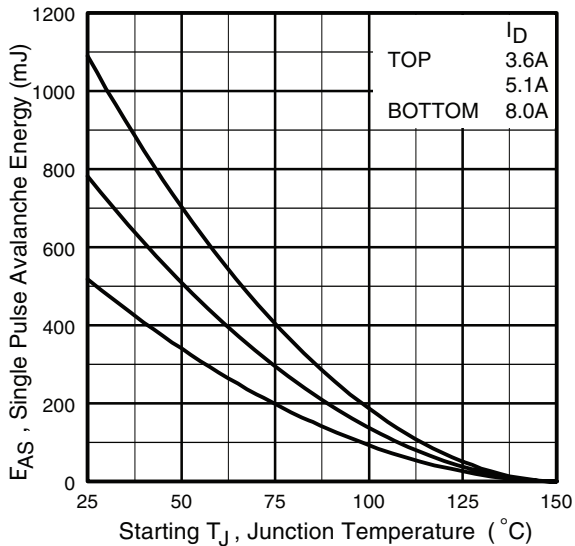


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

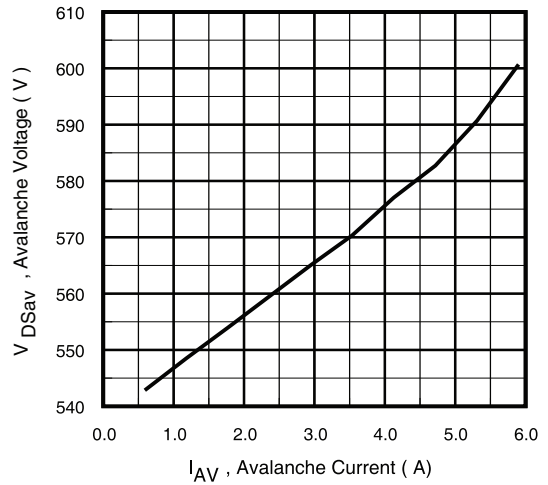


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

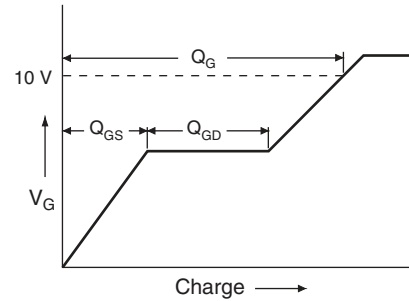


Fig. 13a - Basic Gate Charge Waveform

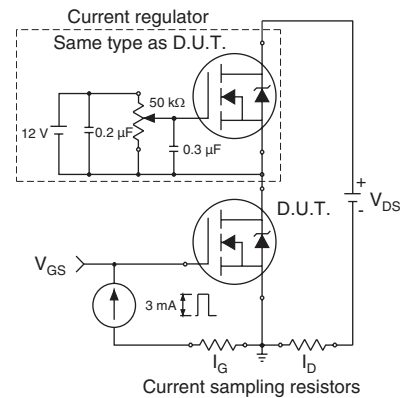
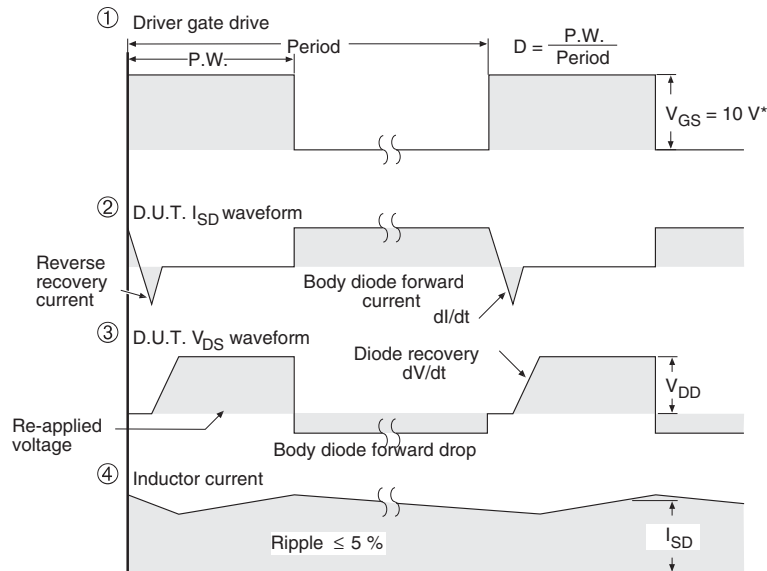
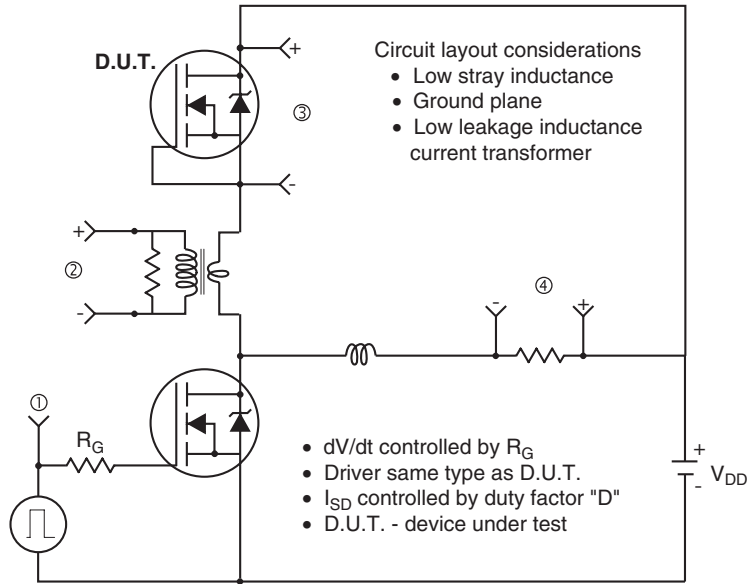


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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